The Fabrication of Highly Conducting and Thermo-mechanically Robust Metal Thin Films

A thesis presented to Trinity College Dublin, the University of Dublin for the degree of

Doctor of Philosophy in Chemistry

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DECLARATION

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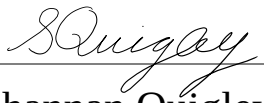

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SUMMARY

Nanocrystalline materials have made their way into a variety of applications as a result of their desirable properties compared to their coarse-grained counterparts. Such properties include; increased strength, enhanced diffusivity, and improved ductility[1]. Nanocrystalline copper, in particular, has found use in the microelectronics industry as interconnects[2]. With each new generation, interconnect structures decrease in dimension. In doing so, the role of surface/interface scattering as well as grain boundary scattering in resistance becomes more prominent[3]. This causes the resistivity of wires to increase with each new generation, making the interconnect, a bottleneck for overall circuit performance. Likewise, surfaces/ interfaces and grain boundaries have been found to be fast diffusion paths for material[4]. As a result, both pathways influence the rate of electromigration[4] and stress voiding[5] within interconnects. Therefore, influencing circuit reliability.

Research on interfaces has been undertaken to find material combinations that minimise resistivity and material diffusion, taking into consideration properties such as adhesion[6], interface/surface roughness[7] and the interfacial density of states[8]. Alternatively, most studies that minimise the impact that grain boundaries have on resistivity and interconnect stability rely on minimising the number of grains within interconnects[9] as well as the width of the grain size distribution[10] or trading improved stability with decreased conductivity by grain boundary doping[11].

Recent research from high-resolution surface probe microscopy and atomic simulation have identified that grain boundaries in [111] FCC copper thin films can restructure in a region immediately below the surface[12]. The restructured boundaries are known as core shifted boundaries (CSBs). CSBs can extend to a depth of approximately 10 nm depending on the in-plane misorientation angle of the boundary[13]. These length scales are the same used for current interconnect technology[14]. DFT quantum transport calculations indicate that the transmission capability of the restructured boundaries versus [111] boundaries at elevated temperatures are improved. Likewise, electromigration mean time to failure calculations show [112] boundaries have enhanced electromigration resistance compared to their [111] counterparts.

This thesis aims to produce a thin film sample predominantly consisting of restructured grain boundaries throughout the entire depth of the film. The starting material for this research were 50 – 60 nm copper (111) thin films. Four etchants were considered to thin these films to the appropriate thickness range. These are citric acid, phosphoric acid,

formic acid, and acetic acid. Electrochemical etching with phosphoric acid produced the fastest etch rate of 4.8 ± 0.4 nm/ second. The speed of this etch made control of sample thickness challenging. Likewise, the etch rate varied over the sample surface. Such variation was not ideal for creating samples with a well-defined thickness. Submersion in aqueous citric acid was the second etchant in terms of speed with an etch rate of 8.2 ± 0.7 nm/ min.

Formic acid etching separated the oxidation step of the sample from the material removal step. Oxidation was completed by exposure of the copper to an oxygen plasma. The subsequent oxide was removed via submersion in formic acid. The etch rate for this sample was 4.5 ± 0.2 nm/ round. This etch was slower than phosphoric acid but had the advantage of a minimal variation in etch rate. The same process was repeated using acetic acid. The etch rate was determined to be 3.4 ± 0.1 nm/round. Like formic acid, the acetic acid etch showed a very small variation in etch rate and has the bonus of etching in smaller steps, allowing for better control of the remaining sample thickness.

Roughness comparisons for all three methods show that the two-step; oxidation – formic acid etch process provided the lowest RMS roughness at each depth point, while submersion in citric acid and electrochemical etching in phosphoric acid behaved in a similar fashion. Analysis of the ACL revealed citric acid as the etch with the lowest spatial roughness. This was attributed to the influence of hole features that the citric acid etch process left on the surface. The fractal dimension was employed to combine vertical and lateral roughness into a single parameter. At all equivalent thickness points, the fractal dimension for the formic acid etch are closer to a two-dimensional surface compared to both the citric acid and phosphoric acid etch methods. The strong controllability of the formic acid etch rate combined with the RMS and fractal dimension performance indicates that formic acid provides both strong control of the etch rate and a relatively smooth surface compared to citric acid submersion and phosphoric acid electrochemical etching. Further comparison of the oxidation-formic acid etch with the oxidation – acetic acid etch revealed the oxidation-formic acid etching provided a smoother finish on the surface. However, the oxidation-acetic acid etch surfaces showed fewer pore features. With smaller etch steps and a slight increase in roughness, the plasma oxidation- acetic acid etch was chosen for producing copper thin films.

An annealing step was added between oxidation-etch rounds to try and further reduce sample roughness. When the metal films are annealed, step density on the surface can decrease and grains can grow. Both processes lead to a smoother film. Alternatively,

grooving at grain boundaries and grain boundary triple points can also occur. These processes increase the roughness of the film. Annealing at 350 °C in an inert atmosphere for 120 minutes did induce grain growth but also promoted surface roughening. STM analysis of films that have undergone seven rounds of etching with eight anneals had significant grain boundary damage, making atomic studies of the grain boundaries challenging.

Initial investigations into inducing grain boundary reconstructions in 60 nm copper films on C-plane sapphire revealed the boundaries in these films were within valleys with depths in the nanometre range prior to any processing. Sputter- annealing rounds roughened the surface according to the root mean square roughness. This was contrasted with the film becoming smoother laterally according to the autocorrelation length. Further anneals at low temperatures are required to allow the large step densities imaged on the cleaned surface to decrease making grain boundaries accessible to be evaluated at the atomic scale.

The resistivity measured for 50 nm copper films on 7 nm of tantalum, which, in turn, is deposited onto a doped silicon wafer, had an average resistivity lower than that expected for bulk pure copper. The thin layer of tantalum used as an adhesion layer was insufficient to divert electrons from crossing into the doped silicon, making electrical characterisation of these films impossible. Alternatively, the measured resistivity of 60 nm copper films on C-plane sapphire at various points of the etch-anneal process could be modelled via a combination of surface scattering and grain boundary scattering models. The change in resistivity as a function of process time was best modelled when the reflectivity parameter for the grain boundaries was allowed to vary for each step of sample processing. The results of the electrical characterisation support the interpretation that the processing employed to thin these samples damages grain boundaries. That being said, the ability of electrical modelling to detect the state of the boundaries provides support that the four-point probe technique can be used to evaluate the electrical resistivity changes that reconstructed boundaries have on a thin film.

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LIST OF ABBREVIATIONS

ACL	Autocorrelation Length
AFM	Atomic Force Microscopy
CMP	Chemical Mechanical Polishing
CSB	Core Shifted Boundary
CSL	Coincident Site Lattice
CVD	Chemical Vapour Deposition
DFT	Density Functional Theory
DI	Deionised
ECD	Electrochemical Deposition
EM	Electromigration
FCC	Face Centred Cubic
FS	Fuchs-Sondheimer
HR	High Resolution
IC	Integrated Circuit
IPA	Isopropyl Alcohol
LAGB	Low Angle Grain Boundary
MD	Molecular Dynamics
MIM	Metal Insulator Metal
MS	Molecular Statistics
MS	Mayadas – Shatzkes
MTTF	Mean time to Failure
PVD	Physical Vapour Deposition
RC	Resistance- Capacitance
RIE	Reactive Ion Etch
RPM	Rotations per Minute
SCCM	Standard Cubic Centimetre per minute
SPM	Surface Probe Microscopy
STM	Scanning Tunnelling Microscopy
TEM	Transmission Electron Microscopy
UHV	Ultra-high Vacuum
WKB	Wentzel-Kramers Brillion

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PUBLICATIONS & PRESENTATIONS

Oral Presentations

"Fabrication of Highly Conducting Thermo-mechanically robust metal films."

Trinity College & University College Dublin DubChem 3rd Year Postgraduate Talk

(Dublin, Ireland, 9th June 2022)

1 INTRODUCTION

The field of microelectronics was kickstarted in 1948 by the unveiling of the transistor by Bell labs[15]. The transistor was originally designed with the intent to be a smaller, more efficient version of its predecessor, the vacuum tube[16]. However, the impact of the transistor extended beyond this, as it inspired both Kilby[17] and Noyce[18] to produce entire circuits with devices made of semiconductor material. These solid-state circuits are now infamous as the world's first integrated circuits (IC)[15]. In modern electronics, an integrated circuit or chip, is a set of electronic components built into planar silicon substrates.[19]

Since the inception of integrated circuits, the semiconductor industry has focused primarily on enhancing functionality and speed within semiconductor devices.[20] Device scaling theory states that if a device's area decreases by half, then the density of devices that can be incorporated onto a chip doubles. At the same time, device performance improves with decreasing dimensions as the gate delay decreases with decreasing device dimensions.[21], [22] The result of such a trend is captured formally as Moore's law, which shows transistor density doubling approximately every 18 months.[23] The systematic increase in devices per unit area along with the increasing performance of individual devices means higher performing chips with each new generation.

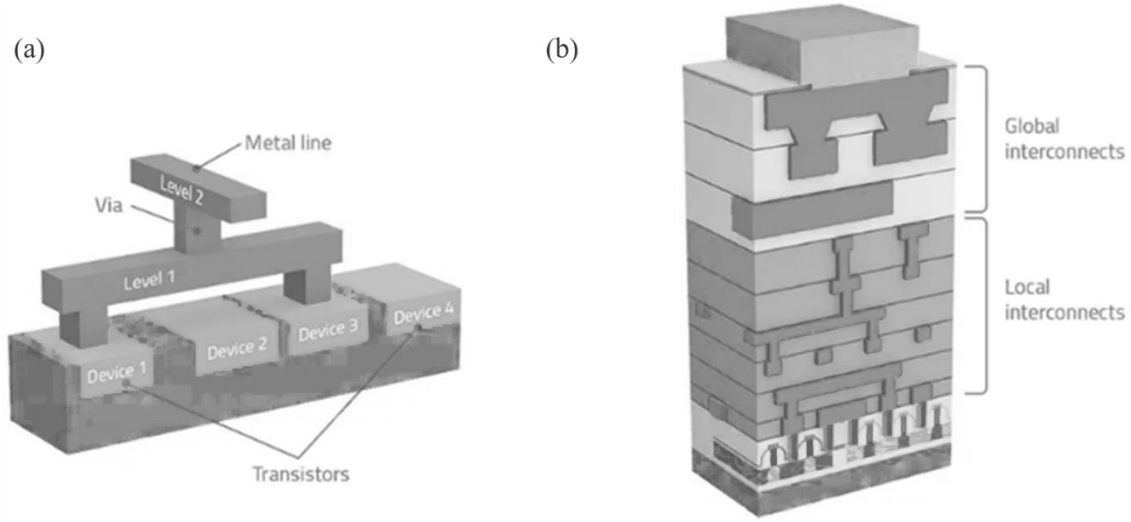

Figure 1.1: Schematic of an integrated circuit. Displaying (a) transistors with a connecting copper interconnect structure containing horizontal lines and vertical vias (b) a hierarchical structure of interconnect types within an integrated circuit.[26]

The same trend, however, does not apply to all elements of the integrated circuit. The most pressing example of this is the performance trends seen in interconnects. Interconnects are the small metal lines used to connect individual components and circuits together. Interconnects, therefore, are the backbone of both power and signal transmission within integrated circuits[24]. As a result, the performance and reliability of interconnects contribute to the performance and reliability of the overall chip. A modern chip surface is so densely packed with devices that the number of interconnects required to connect everything cannot be deposited as a single layer.[24] Instead, modern manufacturers build interconnect structures over several levels. An example of a modern interconnect structure can be seen in ***Figure 1.1***.

The left-hand side of ***Figure 1.1*** shows the subsections of a typical interconnect. The horizontal sections of an interconnect are referred to as lines. Meanwhile, the vertical connections are called vias[25]. On the right-hand side, the various levels of interconnects that are available within an integrated circuit structure are displayed. At the upper levels, there are global interconnects. These interconnects join different circuits within a chip [26]. At the global scale, wire lengths tend to increase with each generation [21]. On the opposite end of the scale, there are local wires. These are the wires that connect individual devices [26]. As such, they decrease in size alongside the devices within each generation [21].

1.1 THE SIZE EFFECT

In contrast to device performance, downsizing interconnect features has had an adverse effect on both their performance and their reliability [27]. The source of these effects is an increase in electrical resistivity. The increasing resistance is the result of the grain boundary and side wall scattering mechanisms that become prominent when dimensions near the mean free path of electron scattering (λ), as seen in ***Figure 1.2***. Since then, size dependence has become a prominent roadblock for creating more power-efficient and reliable nanoscale

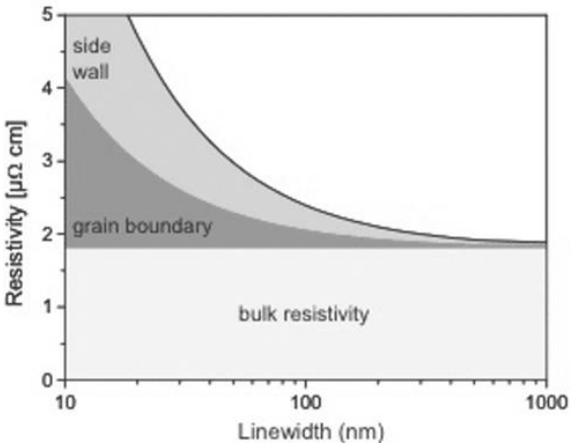

Figure 1.2: Resistivity contributions from different sources as a function of line width. Bulk resistivity is a constant at all linewidths. As the linewidth decreases, grain boundary and surface/interface contributions are responsible for the increasing resistivity[27].

interconnects. For example, 10 nm wide copper interconnects have a resistivity approximately one order of magnitude larger than bulk copper. [2], [28]

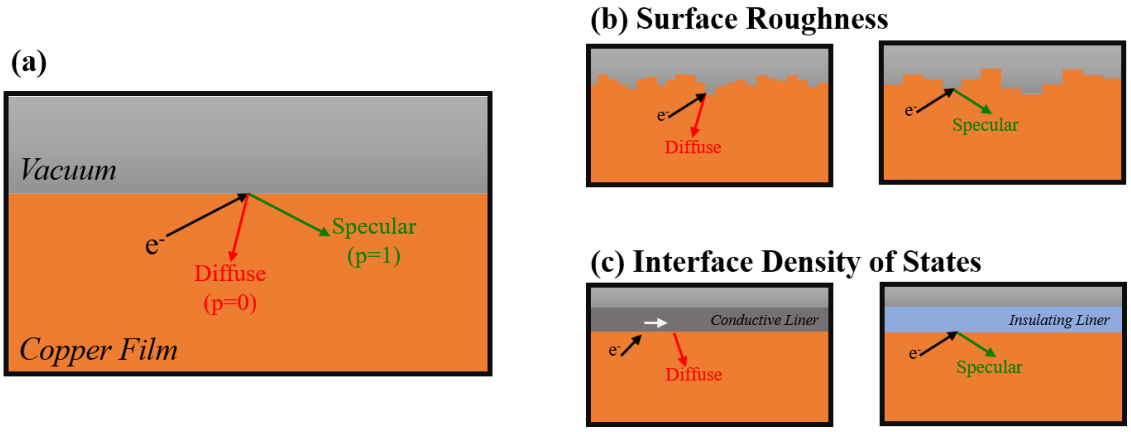

Figure 1.3: (a) Schematic of the surface contribution to resistivity. When an electron scatters at a surface, the reflected electron can either continue in the direction of electron flow (Specular, p=0) or the electron's trajectory no longer moves in the direction of electron flow (Diffuse, p=1). (b) Schematic of the influence of roughness on surface scattering. The smoother the surface is at the atomic scale, the more likely a specular scattering event is to occur. (c) The influence of the density of states at the scattering interface. If an electron can enter an interface material, it is more likely to return metal conductor as a diffusely scattered electron. [31]

Fuchs made the first attempt to explain the size effect in thin films. Fuchs' model[29] was further refined for nanoscale wires by Sondheimer [30]. As a result, the theory is now referred to as the Fuchs-Sondheimer (FS) theory. [31] In this model, Fuchs and Sondheimer attributed the increase in resistivity to an increase in surface scattering. As a piece of material is thinned from bulk to a value in the nanometre regime, the percentage of atoms located at its surfaces or interfaces make up a larger fraction of the overall atoms within the material. Consequently, the surface effect, which was once negligible in the bulk, becomes very influential at the nanoscale. This, combined with the ordinary scattering mechanisms found in bulk (ρ_0), create a thickness (h) dependent total resistivity. The Fuchs-Sondheimer equation of interconnect resistivity (ρ_T) for a square cross-section wire is given by ***Equation 1.1*** [32].

$$\rho_T = \rho_0 + \rho_0 \lambda (1 - p) \left[\frac{3}{8}\left(\frac{1}{w} + \frac{1}{h}\right)\right] \qquad 1.1$$

The wire's dimensions are accounted for via the width (w) and height (h) terms in ***Equation 1.1***. In the Fuchs-Sondheimer theory, electrons are scattered due to interactions with surfaces or interfaces. This process is shown schematically in ***Figure 1.3(a)***. During this process, electrons can undergo two types of scattering. If the electron's momentum changes

entirely, a diffuse scattering event has occurred. Diffuse scattering events are the events which contribute to the increase in resistance seen in thin films and interconnects. Alternatively, the electron could maintain its momentum component parallel to the surface. This type of scattering is referred to as specular scattering. Unlike diffuse scattering, specular scattering does not contribute to a resistivity increase. The likelihood of having either diffuse or specular scattering is encapsulated by the parameter, p, known as the specularity parameter. If p=0, all scattering events are diffuse. Likewise, if p=1, all scattering events are specular [31].

Two factors which can influence the specularity coefficient at a surface or an interface are the roughness of the surface (***Figure 1.3(b)***) and the interfacial density of states. (***Figure 1.3(c)***). Over short lateral distances, a high degree of roughness increases the chance that reflected electron waves at the surface, destructively interfere[28]. This increases the chance of diffuse scattering events. As a result, the specularity coefficient increases. Likewise, if there are localised states at the interface between the metal line and a capping material, electrons can scatter into these localised states and return to the metal line with random momentum, increasing the number of diffuse scattering events. This occurs when the capping material is conductive[8].

The Fuchs-Sondheimer model works well for single crystal films or interconnects but fails to adequately model the changes in resistivity for polycrystalline samples. The deposition techniques used to create thin films and interconnects tend to create workpieces which are polycrystalline in nature. Therefore, a further expansion to the size effect is required. Mayadas and Shatzkes proposed a secondary source of scattering for the size effect. This contribution comes from the grain boundaries. The contribution of grain boundary scattering to resistivity is given by ***Equation 1.2*** [32].

$$\rho_{GB} = \rho_0 \left(\frac{1}{1 - \frac{3}{2}\alpha + 3\alpha^2 - 3\alpha^3 ln\left(1 + \frac{1}{\alpha}\right)} \right) - \rho_0 \qquad 1.2$$

where

$$\alpha = \frac{\lambda}{g}\left(\frac{R}{1-R}\right) \qquad 1.3$$

In ***Equation 1.3*** [32], g is the average grain diameter. Grain size scales with conductor size for microscopic conductors. As such, narrower interconnects and thinner films will have smaller grains and, therefore, larger grain boundary densities compared to their wider or

thicker counterparts. [31] More grain boundaries mean more sites for potential scattering events. As such, the resistivity contribution from grain boundaries is inversely proportional to the grain size. To minimise the contribution of grain boundaries, grain size can be increased. [31]

Like the FS model, the Mayadas and Shatzkes (MS) model contains a phenomenological parameter (R) called the electron reflection parameter. The electron reflection parameter expresses the probability that an electron will be backscattered by grain boundaries. This is shown schematically in ***Figure 1.4***. Therefore, minimising the electron reflection coefficient minimises the resistivity contributions of grain boundaries. In experiment, the reflection coefficient is determined by varying the average grain size on a sample and measuring resistivity. For copper, the average reflection coefficient lies between 0.1 and 0.8[33].

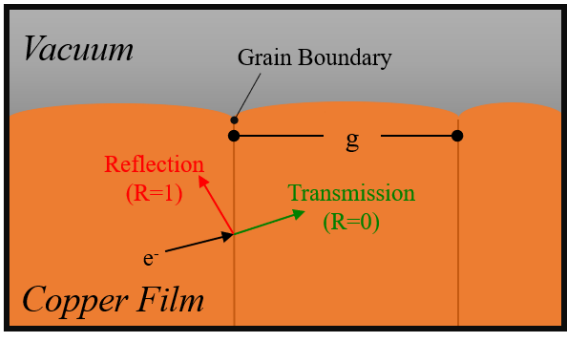

Figure 1.4: Schematic of the influence grain boundary scattering has on resistivity in a metal interconnect. The boundary acts as an internal surface. The electron can pass through the boundary. In this instance the reflectivity coefficient of the boundary is 0. Alternatively, the electron can be reflected, making the reflectivity coefficient of the boundary 1.[31]

The parameter, R, has a distinct limitation in that it is an average over all grain boundaries. Conductive scanning probe measures have been used to measure the specific resistivity of individual grain boundaries[34]. The most conductive grain boundaries are found to be coincident site boundaries Σ3 or twin boundaries[35]. Meanwhile, random grain boundaries have the highest resistivity[35]. The variability of grain boundary resistances can add a challenge to minimising overall sample resistance, as high resistance boundary structures could exacerbate the overall resistance in thin films or interconnects. Alternatively, the variability presents an opportunity to minimise overall resistivity by minimising the grain boundary contribution to resistivity. For example, one method to reduce R is to adjust metal processing to favour the formation of low-energy boundaries.

Another influence on grain boundary resistance is the match between electron states near the Fermi surface in the two adjacent grains. An electron impinging on a grain boundary with energy E and momentum p can traverse the boundary without scattering if there exists and empty state with the same E and p in the new grain. The copper Fermi

surface is approximately spherical. A comparison of copper grain boundaries with tungsten, which has a more anisotropic Fermi surface, via first principle calculations on coherent Σ5, Σ9, Σ11, and Σ17 boundaries predicts that the specific resistances for copper is an order of magnitude lower than that of tungsten. [31]

1.2 RC DELAY

The influence of the size effect on interconnect performance is measured via Resistance -Capacitance (RC) delay. RC delay is the time it takes to transmit an accurate signal across an interconnect. Since resistance is defined as the opposition to the flow of electrons. Increases in resistance for an interconnect result in longer RC delay times. In a similar vein, capacitance is the ability of a material to hold charge. In integrated circuits, two neighbouring lines can act as a parallel plate capacitor. When electrons flow through an active line, a parasitic capacitance can exist allowing the signal to couple to the neighbouring metal line, reducing the signal in the original active line. The product of the resistance and capacitance determines the time delay to transmit accurate signals[14]. To optimise an integrated circuit, both resistance and capacitance must be as low as possible. [2]

The key control parameter of RC delay depends on the type of interconnect under consideration. For example, at the global level of the interconnect structure, lines are extremely long and well separated. Combining this with a narrow cross-section creates wires with high resistance. Therefore, at the global scale, resistance is the controlling parameter for interconnect speed. Alternatively, local interconnects are shorter but more densely packed. The increase in density leads to a decrease in distance between individual lines, which causes an increase in coupling capacitance between interconnects. This creates cross-talk noise and signal delay. [24] As a result, both resistance and capacitance must be considered when thinking about decreasing interconnect dimensions.

1.3 ELECTROMIGRATION

Alongside performance concerns, the size effect also brings about reliability concerns. The first reliability concern for interconnects was noted during the 1960's and is known as electromigration (EM). Electromigration is the biased mass transport of atoms within a thin film or interconnect in the direction of current flow due to momentum transfer during electron-atom collisions. The momentum transfer model was first proposed

independently by both Fiks and Huntington [36]. The semi-ballistic model[37] starts with a conceptual "average" electron within a metal. As there is no current flowing within the metal, the average electron is at rest. In reality, electrons are never at rest. However, the momentums of electrons within a metal are equally distributed in all directions. The average of all electron momentums is zero. Hence, the average electron is said to be at rest. [38]

When an electric field is applied to a metal, the average electron accelerates in the direction applied by the electric field. This continues until the electron collides with a defect. During this collision, the electron's momentum is transferred to the defect. The momentum gained is equal to [38]

$$Momentum\ Transferred = Ez^{*}el \tag{1.4}$$

In ***Equation 1.4***, l is the mean free path of the electron, E is the applied electric field, e is the charge of the electron and z^{*} is a quantity that expresses the effectiveness of momentum exchange. In order for an atom to move within a metal, it needs a place to move to. This means that the motion of atoms within a metal is accompanied by the movement of a vacancy in the opposite direction. As such, the driving force can be expressed as acting on either the atoms or the vacancies. [38]

There are three potential diffusion pathways that atoms can move through; the lattice, the grain boundaries, or the interfaces/free surfaces. Electron scattering at a vacancy is dependent on the defect's configuration. As a result, the driving force for each diffusion path is different. Therefore, the dominant diffusion mechanism is a function of the material, the temperature, and the microstructure of the conductor. At high temperatures, lattice self-diffusion will dominate. Whereas, at lower temperatures, the activation energy is a function of the geometry and the microstructure of the conductor [38]. Copper is the chosen material for interconnects as it has a high conductivity and a rather low self-diffusion, making it relatively resistant to electromigration compared to other metals.[39] The activation energy for grain boundary diffusion is between 0.8 and 1.0 eV. Meanwhile, for interfacial diffusion, the activation energy is between 0.8 and 1.1 eV. Depending on how the interconnect is designed, either pathway is viable for electromigration. [21]

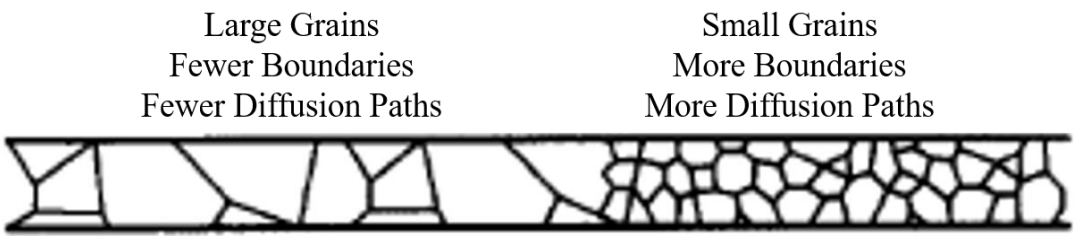

Figure 1.5: Schematic of grain size variation within a copper interconnect line [39].

The movement of atoms in the direction of electron flow causes voids/holes or hillock features to form. Voids form in regions where the flux of vacancies changes, allowing individual vacancies to pile up.[40] Some sources of flux divergence are diffusion barriers, thermal gradients, grain boundary tiple point intersections, or, the most common source in fine-grained interconnects, changes in grain size. [41] For example, in ***Figure 1.5***, the left-hand side of the film has larger grains compared to the right-hand side. The right-hand side has fewer grain boundaries for mass transport compared to the left-hand side. If a current is applied from left to right, a void forms in the middle of the section as more material leaves this section on the left than enters from the right. Subsequent void growth can then occur, provided there is a sustained vacancy flux divergence. The void eventually reaches a critical size in which the current density and the temperature distribution near the void increase, accelerating the rate of damage. These features grow until the interconnect or film is unable to pass current. [41]

Alternatively, if a current is applied from right to left, a pile-up of material occurs in the centre region as more material is entering the centre region from the right than is leaving at the left. This creates a hillock feature. Hillocks can grow and extend out from the interconnect. These can connect to adjacent lines making short-circuit failures. Hillock damage formation occurs in a similar manner to voids. However, this time there is an accumulation of atoms. Void-induced failures typically appear earlier than hillock-induced failures. [41]

In order to reduce electromigration damage, either the magnitude of the atomic flux must be reduced or the inhomogeneity in the parameters controlling the mass transport must be reduced. In early interconnect research, the current passed through an interconnect was limited to minimise the potential for electromigration. This, however, was not a tenable solution as device performance was reduced meaning processing speed was sacrificed for reliable function.

One of the most widely used methods to improve electromigration resistance in interconnects is interfacial engineering.[42] The copper line is usually encapsulated by a barrier. The barrier is designed to stop copper migration into the dielectric. Another advantage of encapsulating copper is the prevention of copper oxidation. Copper is incapable of producing a stable native oxide. The copper oxide interface allows for significant mass diffusion. Evidence suggests this can be a primary path for material diffusion in electromigration. [42] By mitigating the formation of copper oxide interfaces, interconnect reliability is improved. Additionally, mitigating the formation of copper oxide minimises the resistance of the copper line as copper oxide roughens the conducting copper surface, producing more diffuse scattering events[31].

Studies of different encapsulating materials, such as CoW_xP_y [43], [44], $CoSn_xP_y$ [43], $CoW_xB_yP_z$ [45], Pd [43], Ta/TaN_x [44], [46], W[47], Ir[2] and Ru[48] have been conducted. Ta/TaN systems are the most frequently used as barrier layers. All studies show a strong correlation between adhesion to the copper surface and the electromigration behaviour of copper. However, even in the presence of an encapsulating layer, void formation can still occur. Although the voids are across grain boundaries, the presence of these "slit-like" voids indicates grain boundary diffusion contributes to electromigration, especially in strongly encapsulated interconnects. [49]

Flux inhomogeneities within the copper can be reduced by modifying a conductor's microstructure. Larger grains lead to fewer grain boundary triple points, giving fewer sites of flux inhomogeneity. Likewise narrow grain size distributions reduce the chances of having regions of varying grain size within a copper line. Microstructure optimisation starts with choosing the deposition method. Methods such as physical vapour deposition (PVD)[50], [51], [52], chemical vapour deposition (CVD)[51], [52], [53] and electrochemical deposition (ECD)[52], [53] have been used to form copper interconnects. ECD has been found to provide the largest average grain sizes compared to CVD[52], [53] and PVD[50], [52].

An increase in average grain size can be further promoted by thermal annealing post-deposition. For ECD and some conditions of PVD, copper lines have an unstable microstructure. As a result, even leaving the lines at room temperature for a time allows for grain growth[54], [55], [56]. This process is called self-annealing. Hu et al. [57] studied the change in microstructure due to the inclusion of an annealing step between deposition and

CMP removal of material. Annealing at elevated temperatures created larger grains than seen in the as-deposited lines. However, no difference in microstructure was noted between samples annealed at 100 °C and 250 °C. EM median lifetime tests showed that samples with no anneal had the lowest lifetimes. Meanwhile, the samples annealed at 100 °C and 250 °C provided similar median lifetimes for each linewidth tested.

The presence of the overburden, which was initially kept for pre-CMP annealing as it minimised the chance of obtaining either void or hillock features at the trench surface, was found to impact the microstructural evolution of copper during annealing. Carreau et al. [58] studied the interplay between line width and anneal temperature for samples with and without an overburden. For a 150 °C anneal, the presence of the overburden provided lines of lower resistivity for all line widths (30 nm to 30 μm). Alternatively, at 400 °C, the presence of the overburden did not seem to affect the resistivity measurements for any linewidths.

Brandstetter et al. [59] performed a similar study. Here, the influence of overburden was found to depend on the trench width. In relatively wide trenches (~3 μm), the overburden was found to have a strong effect. Grains were able to extend from the overburden to the bottom of the interconnect trench. However, there were still several grains spanning the width of the interconnect in these structures. As such, the longitudinal grain boundaries still acted as potential pathways for mass transport. Alternatively, for thinner interconnect widths, the overburden is unable to aid in the modification of the microstructure within the trench. At widths below 250 nm, there is little effect, and at 80 nm or less, there is practically no effect [59]. A more detailed study of overburden thickness and microstructure development was done by Dubreuil et al.[60] For narrow interconnects thinner overburdens were found to promote grain growth more than thicker overburdens.

The texture of the copper line can also influence electromigration behaviour[61]. The most characteristic texture in both as-deposited and annealed copper interconnects is the (111)[53], [62], [63] orientation, though contributions from (200) [53], [63] and random orientations[52] have also been observed. In copper thin films, the interface and the free surface contribute a large fraction to the total free energy of the film. As such, the texture of the film that provides the lowest surface and interface energy is preferred to minimise the total film free energy. For FCC metals, the orientation with the lowest surface energy is the (111)[63]. This is the origin of the (111) texture seen in copper interconnects.

In opposition to this, deposition and annealing conditions can introduce stress into the film via grain growth and by the mismatch in thermal expansion between the film and substrate. To combat this, films can preference the growth of grains, which have orientations that minimise the strain energy of the film. The lowest strain energy density orientation for copper is (100)[63]. These two driving forces compete with one another. For each thickness, there is a threshold biaxial stress where strain energy minimisation dominates. This gives rise to the (200) texture. Below this stress, surface/interface energy minimisation drives texture creating (111) films[63]. The texture of copper in trenches can be controlled via the choice of barrier and seed layer[53], deposition method conditions[61], [64], [65], the subsequent processing conditions[66], [67] and the line characteristics [61], [62], [66], [68], [69].

Ryu et al. [53] studied the difference in the electromigration performance with differing copper texture using CVD copper films. It was found that films with a majority (111) orientation had better electromigration performance compared to (200) oriented test lines. The test lines were polygranular with similar grain size distributions. The difference in performance was attributed to a narrower tilt distribution of grains in the (111) interconnects compared to the (200) interconnects. Here, the tighter tilt distribution means a lower flux deviation between different boundaries, reducing void nucleation. That being said, the electromigration experiments were completed on unpassivated copper. As such, the difference in electromigration behaviour could also be the result of surface diffusion along the differently oriented grains as opposed to variation in grain boundary behaviour.

Abe et al. [61] noted a similar correlation between the strength of the (111) orientation and EM resistance. However, the difference in textures between samples was due to different barrier layers. The improved EM resistance was reported to be a mix of suppression of copper diffusion at both grain boundaries and the copper-barrier interface. Ji et al. [66] also noted improved electromigration resistance in post-anneal samples. The samples had larger grain sizes and stronger (111) texture. This improvement was attributed to the reduction in grain boundaries and the minimisation of high-angle grain boundaries (HAGB) in the annealed lines. Like Ryu et al. [53], no capping was added to the lines, allowing the free surface to act as a diffusion pathway.

Since grain boundary diffusion plays a role in the mass transport of copper, modification of boundary structure or chemistry can be used to decrease the rate of mass

transport. Not all grain boundaries provide sufficiently fast electromigration pathways. From aluminium studies, the (111) tilt grain boundaries with low misorientation angles (<11 or 15 °) are poor pathways for electromigration voids. Meanwhile, high-angle misorientation boundaries provide fast diffusion pathways except for coincident site lattice (CSL) boundaries. Since copper is an FCC metal, the behaviour of aluminium could be extended to copper [42]. In situ transition electron microscopy by Oh et al. [70] shows that the high angel grain boundaries exposed to the free surface are the most favoured path for electromigration in polycrystalline copper.

A second technique used routinely to inhibit the rate of transport along the grain boundaries is doping[11], [71], [72], [73], [74] the interconnect material with a solute. The downside of such a technique is the increase in resistivity of the interconnect. This becomes especially prominent as the dimensions of the interconnect decrease. Copper can be dopped with aluminium[11], [71], [72], [73], manganese[74], or tin[72], [73]. Dopants are typically introduced during the seed layer deposition. Subsequent annealing allows the atoms to move towards the grain boundaries and/or into the capping interface. Hu et al. [72] suggested that the improvement of electromigration with aluminium comes from arrested diffusion at the interface and is less effective in grain boundary electromigration. The CuMn [74] seed alloy has similar behaviour to aluminium. On the other hand, the tin[73] alloy seed layer is mobile in the grain boundaries and at the free surface, leading to an improved EM resistance.

1.4 STRESS VOIDING

Stress-induced voiding, also termed stress migration, is the process in which voids form within interconnects due to tensile stresses within the metal. Stress can be introduced into the metal via a mismatch of the thermal expansion coefficients between the metal and its surrounding material. This type of stress is known as thermal stress. Alternatively, stress can be introduced via grain growth within the metal. This is referred to as growth stress. To relieve stress within the metal, voids form. In order for the voids to cause interconnect failure, they must increase in size to cause either a significant increase in resistance or create an open circuit[75]. As such, the process of stress-induced voiding can be broken into two steps; void nucleation and void growth. [21]

Thermal stress is introduced to an interconnect during the fabrication process. For example, in copper interconnects, the deposition of the copper material is done at relatively

low temperatures. Alongside this, the top surfaces of copper lines are not constrained. This makes the thermal stress in the copper relatively low. However, to apply a capping layer and the interlevel dielectric, a relatively high temperature is required. During this process, the copper expands. Once the device cools, the copper tries to retract, but the presence of the capping layer constrains the copper, and the copper cannot move back to its original state. This introduces tensile stress into the interconnect. [5]

Grain growth can also contribute to tensile stress. Copper is usually deposited at low temperatures. This means the as-deposited film has a small grain size. Since subsequent depositions occur at much higher temperatures, grain growth occurs in the copper. The grain growth eliminates free space within the copper, creating excess vacancies and shrinkage in the metal lines. If grain growth occurs prior to the deposition of the capping layer, the vacancies can diffuse to the free surface and are annihilated. Alternatively, if the grain growth occurs post-capping layer deposition, the vacancies are trapped within the copper and shrinkage of the metal line results in tensile stress. [21]

To relieve the tensile stress, voids form within the line. In order to form a void, the strain energy released must exceed the change in energy at the interface, assuming that voids form at the interface. As such, there is a critical stress for void nucleation. Any stress above this value will produce a void that is thermodynamically stable. The critical stress is dependent on the adhesion between the copper and the surrounding material and on the modulus of the dielectric. The barrier to void formation can also be reduced if there are preexisting defects within the structure. Potential defects include undercut from the creation of vias or a poor fill of the trench during plating.

For thermal stress-induced voids, the maximum rate of void growth occurs at a temperature below the "stress-free" temperature. Where the "stress-free" temperature is related to the deposition of the capping layer and subsequent processes. When the temperature of the interconnect is close to the stress-free temperature, the tensile stress is low. As such, void growth is low. However, at low temperatures, the copper diffusivity is low, so void growth also occurs slowly. As such, void growth can only occur at temperatures where there is significant tensile stress and relatively high copper diffusivity. The rate of void growth is given as [21]

$$R = C(T_o - T)^N \exp\left(-Q/kT\right) \qquad 1.5$$

Where T_o is the stress-free temperature, N is the creep exponent, Q is the activation energy of copper diffusion, k is the Boltzmann constant, and C is a proportionality constant. The activation energy for bulk copper diffusion is 2.2 eV. For grain boundary diffusion, the activation energy is between 0.8 and 1.0 eV and for interface diffusion, the activation energy is between 0.8 and 1.1 eV. Therefore, the dominant diffusion mechanisms for stress-induced voiding are grain boundary and interfacial diffusion. [21]

Stress-induced voids in copper are typically seen at grain boundaries, under vias or inside vias. Voids that form at grain boundaries and at interfaces are a result of the fast diffusion paths compared to bulk diffusion. Meanwhile, the formation of voids under vias is a result of a stress gradient in the underlying copper line as well as the composition of the via-metal interface. Models of vias in a line show high tensile stress in the metal at the edge of the via. When the tensile stress exceeds the critical stress, voids form.

Since the kinetics of void growth is controlled by interface, void growth rate can be reduced by interface engineering. As with electromigration, a strongly adhering interface between the copper and the encapsulating layer can inhibit the use of the interface as a fast diffusion path. Another form of interface engineering is through the etch step used to remove copper over-fill. If the etch has poor selectivity and end-point detection, defects can be left in the copper. If a via of capping layer is then added atop this copper, the defects allow holes to form which attract vacancies to form a killer void. As such, any etch used should prioritise the minimisation of copper defects. [75]

As grain boundaries can also be sites of stress voiding, annealing processes have been used to minimise the formation of stress-induced voids [21]. Ogawa[76] et al. studied the effect that post-deposition annealing had on stress migration. They found the stress migration failure rate could be reduced by a factor of 10 with post-deposition annealing. Von Glasow et al. [75] studied the effects of insufficient annealing. In their study, grain growth occurred during stress, causing voids within and below the vias.

Harada et al. [77] studied the effect of two separate annealing processes on copper. The first anneal was at 150 °C prior to the CMP removal of the overfill. The second was a 400 °C anneal between the CMP and capping layer deposition. With or without the post CMP anneal, the interconnects were more resistant to stress-induced voiding with a resistance shift of no more than 5% after 2500 h of stress at 225 °C. The post CMP annealed samples with the most migration sensitive structures had a slightly larger resistance

increase. This could indicate that the pre-CMP anneal was incomplete. As such, grain growth occurred during the post CMP anneal, and vacancies were either trapped within the copper or diffused to the copper surface, creating an abnormal topography and weakening the copper-cap interface. After capping, the anneal temperatures should be limited as high-temperature annealing promotes stress-induced void formation.

In terms of both performance and reliability, the copper interface and grain boundaries have been identified as key locations of interest. Research on copper interfaces shows that both the chemical composition and structure of the interface can be manipulated to minimise the impact of the copper interface in both areas. Alternatively, for grain boundaries, most of the pursued work aims to minimise the number of grain boundaries without considering how promoting certain structures could also improve reliability and minimise resistance.

1.5 GRAIN BOUNDARIES

In the previous section, the role of grain boundaries in RC Delay and damage processes for interconnects was highlighted. However, this was done without a detailed description of what a grain boundary is and how it is structured. In nanocrystalline materials, such as interconnects, there is an aggregation of single crystals that are oriented differently from one another. In order for the films to be continuous, the grains bond together. The interfaces where two grains join are called grain boundaries. Grain boundaries are planar defects that are used to maintain continuity between two adjoining single crystals that are oriented differently to one another. [78] Initial observations of grain boundaries were performed using optical microscopy. An example of this is shown in ***Figure 1.6(a).***

The individual atoms within a boundary, referred to as the boundary core atoms, are displaced from their regular crystal positions, like those within the grain interior. If the atoms are not arranged by their regular crystallographic sites, how are they organised? In early models, it was assumed that grain boundaries were regions with an amorphous structure. Later, the grain boundary was considered to be made of regions of "good" material and "bad" material. This was developed from dislocation models of grain boundary structure. Both theoretical and experimental studies show the grain boundary has a crystal-like structure, but its structure differs from that of the adjoining grains on either side of it. [78]

In terms of atomic structure, grain boundaries can be divided into two groups; low-angle grain boundaries and high-angle grain boundaries. Low-angle grain boundaries have a small misorientation angle between the two grains that comprise them. For low-angle boundaries, the misorientation can be accommodated by an array of dislocations or by half-planes that are shoved in periodically between the grains to make up the grain boundary angle. The grain boundary can, therefore, be represented as a periodic row of discrete dislocations with their Burger vectors (*b*) having the same sign. The misorientation angle (θ) can be related to the size of the Burgers vector and the dislocation spacing (D) by ***Equation 1.6.*** [78]

$$\sin\frac{\theta}{2} = \frac{|b|}{2D} \qquad 1.6$$

For low misorientation angles, sin(θ/2) can be approximated by θ/2, making θ ≈ |b|/D. Tilt grain boundaries are formed by edge dislocations, while twist boundaries are made by an array of screw dislocations. An example of a low-angle tilt grain boundary is shown in ***Figure 1.6(b)***. [78], [79]

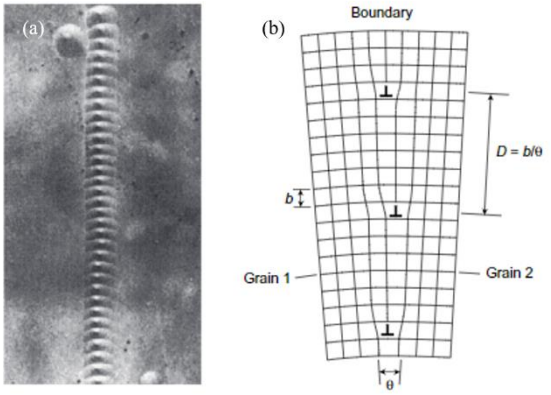

Figure 1.6: (a) An optical micrograph of a symmetrical pure tilt boundary between germanium crystals. An etchant has been used to form pits around the individual dislocations in the array. The etch pits are evenly spaced (b) A diagram of the arrangement of the dislocations in the boundary[79].

As the misorientation angle increases, the spacing between individual dislocations decreases. Eventually, the dislocations lose their character and dislocation theory cannot be used to describe the grain boundary structure. Generally, the limit for the successful application of the dislocation model is between 13° and 15°. This corresponds to a value of D ≈ 4|*b*|. The reason that the dislocation model fails is due to the fact the individual grains are no longer distinguishable and now overlap one another. [78]

Systematic computer modelling studies of FCC cubic crystals has given rise to a new model called the structural unit model. Within this model, high-angle grain boundaries are formed by repeat structural units that represent particular arrangements of limited numbers of atoms. There are a limited number of basic structural units. As a result, there is a limited number of grain boundaries that can be formed by single structural units. A

majority of high-angle grain boundaries consist of combinations of the simple structural units. [78]

Currently, the investigation of grain boundaries is undertaken by high-resolution TEM (HR TEM). HR TEM is capable of providing atomic scale resolution of thin films. Despite the high resolution this technique offers, TEM has innate disadvantages for imaging grain boundaries and dislocations. In order to produce TEM images, samples need to be thin enough to allow electrons to transmit through them. Oftentimes, this means samples must be thinned. The thinning of the samples introduces plastic deformation which results in a change in the dislocation concentration by dislocation emission at the film's surface. Grain boundary dynamics such as sliding and migration may also occur during the thinning process.[80] Likewise, atomic resolution on emerging grain boundaries in TEM is limited due to its sensitivity to any misalignments of the tilt axis from well-defined crystallographic orientations. Likewise, TEM's requirement for a capping layer also makes atomic resolution difficult. [80]

Another technique which has been utilised successfully to analyse the structure of grain boundaries at the surface is scanning tunnelling microscopy (STM). STM is capable of providing a three-dimensional map of the surface topography with atomic resolution, and unlike TEM, STM's high vertical resolution makes it capable of detecting slight changes in the boundary tilt axis due to grain rotation.

1.6 Discovery of Grain Boundary Reconstruction

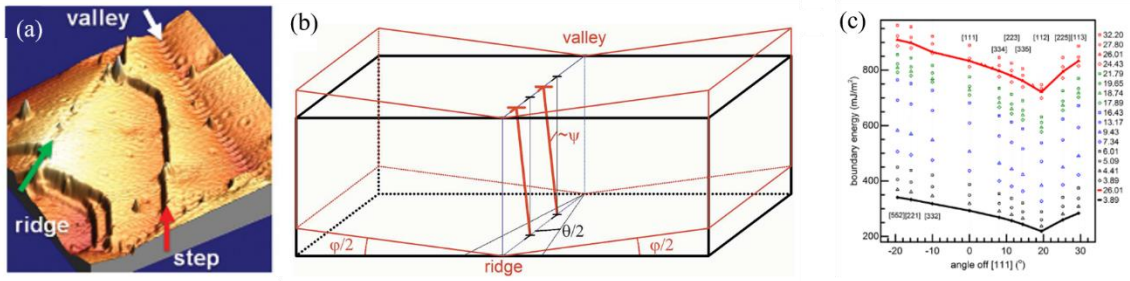

Figure 1.7: (a) A three-dimensional rendering of an STM topograph of a nanocrystalline copper film[12]. *(b) Representation of LAGB film tilting for in-plane angle θ and out-of-plane angle φ*[12]. *(c) Plot of calculated GB energy versus inclination angle ψ for grain boundaries of different misorientation angle. Each case boundary has a minimum at ψ =19.47°*[13].

A recent pioneering STM study of surface grain boundaries was conducted by Zhang et al.[12] In their study of 50 nm thick nanocrystalline copper (111), it was discovered that the copper surface consists of ridges and valleys that coincide with locations where grain boundaries (GB) meet the surface. A three-dimensional rendering of the

nanocrystalline copper film is shown in ***Figure 1.7(a).*** An out-of-plane rotation of neighbouring grains is responsible for the formation of ridges and valleys and is accompanied by a shifting of the tilt axis away from the (111) direction. From analysis of the corrugations within the boundaries, it was found that the GBs at valleys dissociated into two Shockley partials with a stacking fault sitting between them. Meanwhile, in ridges, the array of dislocations was not dissociated.

Molecular dynamic (MD) simulations were performed to understand why the out-of-plane rotation occurred. It was found that the grain boundaries "restructured" to allow the dislocation cores to shift away from the [111] direction by an angle ψ along the boundary. The shift occurs because it is energetically favourable for the dislocation cores to lie within a member of the close-packed family of {111} planes. The geometrical relationship between the in-plane misorientation angle (θ), the inclination angle of the grain boundary cores (ψ) and the out-of-plane rotation angle (φ) was found to be ***Equation 1.7***. The relationship between the three angles was also expressed schematically, as shown in ***Figure 1.7(b)***.

$$\tan\psi = \frac{\tan(\varphi/2)}{\sin(\theta/2)} \qquad 1.7$$

Molecular statics (MS) calculations of grain boundary energy versus inclination angle were undertaken for free-standing (111) films. In these calculations, the grain boundary energy always reached a minimum at an inclination angle of $\psi = 19.47\,°$ for all three tested misorientation angles (θ). At 19.47 °, the dislocation lines are parallel to the [112] so that the stacking fault ribbon that comprises the boundary cores all lie within the lower energy $(11\bar{1})$ planes, allowing for the overall dislocation line energy to be a minimum. The restructured boundaries are referred to as core shifted boundaries or CSBs. Further study showed CSBs are energetically preferred for all types of grain boundary misorientation angles [13] and for all types of face-centred cubic (FCC) metals[81]. This includes high-conductivity metals such as copper, aluminium and silver[81].

The driving force of the restructuring is the decrease in energy caused by the stabilisation of the cores. In copper, CSBs were found to be approximately 30% lower in energy compared to other tilt boundaries at low misorientation angles. This decreased to ~ 10% before increasing again to > 40% for the 60° misorientation twin boundaries.

[81]Similar trends are also found for other FCC metals.[81] In all cases, the energy stabilisation was particularly significant at low misorientation angles.[81] These [112] CSBs are always found to be present at the surface of FCC metals.

The decrease in grain boundary energy competes with an increase in the elastic stress caused by restructuring. The depth of a CSB is determined by balancing the energetic driving force and the elastic energy cost. This can be expressed mathematically as ***Equation 1.8***.

$$h = \frac{\Delta\gamma_{gb}}{2cG\varphi^2} \qquad 1.8$$

$-\Delta\gamma_{gb} \cdot h$ is the energetic driving force, and $c \cdot G\varphi^2 h^2$ is the elastic energy cost, where c is related to Poisson's ratio, and G is the shear modulus. The depth of the reconstruction (h) ranges from a few nanometres up to 10 nm, depending on the in-plane misorientation angle. The CSB depth as a function of the misorientation angle for copper is shown in ***Figure 1.8***. The depth is several nanometres for low-angle grain boundaries. The depth of low-angle CSBs is the same as the length scale for current interconnects technologies. The depth decreases as the misorientation angle increases until it is ultimately reduced to the thickness of an atomic layer at approximately 32.20°.[81] Misorientation angles above this show a modest increase in depth. However, the restructuring is still limited to several atomic layers, which creates a surface effect.

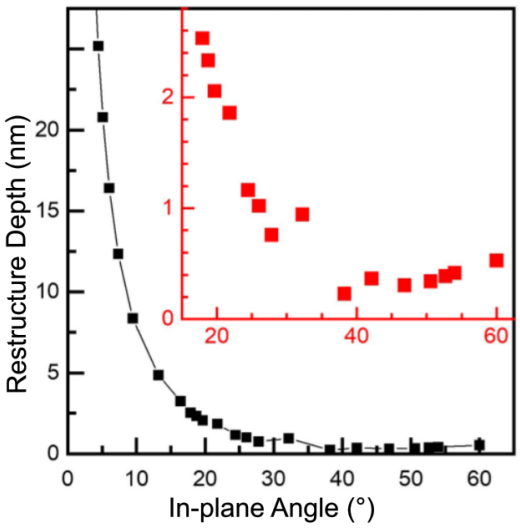

Figure 1.8: Misorientation angle versus reconstruction depth for copper. Insert is a close-up of the misorientation angles > 15 ° [81].

The Boland group are performing DFT quantum transport calculations for low-angle grain boundaries. The simulations are challenged by the size of the cell required to capture the enhanced core dislocations. Unpublished results of the specific resistivity in Σ21(θ = 21.79°) boundaries, comparing [112] boundaries with [111] boundaries in bulk copper, show the two boundaries have similar resistivities at zero Kelvin. At room

temperature, the resistivity of both boundaries increases by a factor of 5 or more and at higher temperatures, the [112] boundary is more conductive. The calculations show an enhanced cohesive energy for the atoms making up [112] boundaries and a blue shift in their phonon frequencies that is responsible for the improved transmission properties compared to the [111] boundaries.

The enhanced cohesive energy of the atoms in [112] boundaries and the blue shift in phonon frequencies also point to [112] boundaries having improved electromigration resistance. An estimate for the improvement in the mean-time to failure (MTTF) due to electromigration was estimated by the Boland group by comparing the difference in binding energies of the weakest bound atoms at [112] and [111] boundaries. The differences ranged from 0.15 eV in angles up to 30° to 0.08 eV in higher angles. If there is a significant conversion of [111] boundaries to [112] boundaries at 300 K, the Black equation provides a MTTF improvement of 400 for boundaries up to 30° and 30 for higher angles. At operation temperatures of 400 K, the improvement reduces to 70 and 10, respectively.

The Boland group has managed to simulate [112] CSBs and induce them to form on the surface of nanocrystalline copper under vacuum conditions. Simulations of these boundaries have provided support for their improved conductivity and thermomechanical stability. The next stage in the experimental focus is to find processing conditions that allow for the formation of [112] CSBs in atmospheric conditions. If these boundaries can be formed within interconnects, they may be a route to improving copper interconnect conductivity and thermostability. This research path would be a deviation from previous methods used to reduce electromigration and stress voiding as this path does not rely on either the minimisation in the number or boundaries or on dopants, which are known to increase the resistivity of interconnects.

1.7 AIMS OF THIS THESIS PROJECT

The aim of this project is to fabricate nanoscale films solely comprised of CSBs. The strategy involves the use of thicker 50 nm film whose grain structure can be optimised using post-deposition treatments such as sputtering and annealing. Once the grains are as flat and as large as possible, these films will be etched down to thicknesses where the restructured boundaries can dominate. From there, the films can be further annealed to ensure complete grain boundary relaxation. The predominance of reconstructed grain

boundaries within the film is expected to play a substantial role in improving the film's stability as well as enhancing its conductivity.

To this end, four methods by which copper can be controllably etched on a nanometre scale are compared. The etch methods are evaluated on both their ability to controllably etch copper and on the roughness of the remaining sample thickness. These results are presented in Chapters 3 and 4, respectively. Following on from this, Chapter 5 evaluates the effect of recovery annealing on the topography of etched samples via AFM and whether restructured grain boundaries can be identified in such films via STM. Finally, resistivity modelling is employed to determine if the etch-anneal process can produce copper films with grain boundaries of improved resistivity. Analysis in each chapter is completed for two samples. The first is a 50 nm nanocrystalline copper (111) on silicon. Zhang et al. induced and characterised the reconstruction on a similar sample. The second is a 60 nm copper (111) film that is deposited on C-plane sapphire. This sample was introduced to allow for resistivity measurements to be completed as the doped silicon required for STM samples makes resistance measurements on the 50 nm copper challenging.

Though an etch method to controllably thin copper films was produced, the etch and anneal process was not without its flaws. As a result, some of the aims of this thesis are left unfulfilled. For the 50 nm copper on tantalum on silicon, the etch resulted in films with considerable roughness in grain boundary regions. This roughness made procuring evidence of the grain boundary reconstruction at the surface via STM impossible. Likewise, the evidence of the presence of the grain boundary reconstruction was not found via the four-point probe. This was the result of a leakage current into the doped silicon.

As of the writing of this thesis, the as-deposited copper on sapphire samples is still in the cleaning stage within STM. As such, no evidence of the grain boundary reconstruction on the sample surface has been obtained. AFM analysis of the etched samples shows that the etch process had a strong preference for the grain boundary. However, analysis of the four-point probe data showed evidence that resistance measurements can be used to determine the state of the grain boundaries.

2 EXPERIMENTAL TECHNIQUES & METHODS

The key focus of this section is to describe in detail the equipment, techniques and procedures employed throughout the course of this project. This begins by detailing the essential characterisation equipment implemented within this thesis, from their principle of operation to the exact details of the systems used. Such pieces include scanning tunnelling microscopy (STM), atomic force microscopy (AFM) and four-point probe resistance measurements. Following this, the process by which the copper films are etched and annealed is described in detail. Finally, the metrics by which surface roughness can be evaluated are identified, and their significance is explained.

2.1 SCANNING TUNNELLING MICROSCOPY

2.1.1 Theoretical Background & Operating Principle

Scanning tunnelling microscopy is the inaugurate technique of the surface probe microscopy family. It was conceptualised in 1982 by Binning and Rohrer[82]. The power of STM lies in its ability to provide topographic information on conductive surfaces with atomic resolution. The basic operating principle of STM is illustrated in ***Figure 2.1***. In STM, an atomically sharp metallic tip and a conductive surface are brought within Ångströms of one another, just out of mechanical contact. Between the two lies a vacuum gap. A bias is then applied across the tip and sample. The bias causes current to flow between the tip and sample. Electrons are able to move through the vacuum gap as a result of quantum mechanical tunnelling. The tunnelling current can be used to either control the separation between the tip and the sample or probe the surface's local physical properties. If the current is kept constant, the separation between the tip and surface is also kept constant, to a first approximation. A constant current is achieved by means of a feedback loop. Since the distance between the tip and sample is kept constant, the contour of the surface is obtained by measuring the tip's vertical position (Z) as a function of lateral position (X, Y), producing a three-dimensional image as the tip is rastered over the surface by piezoelectric drives.[83]

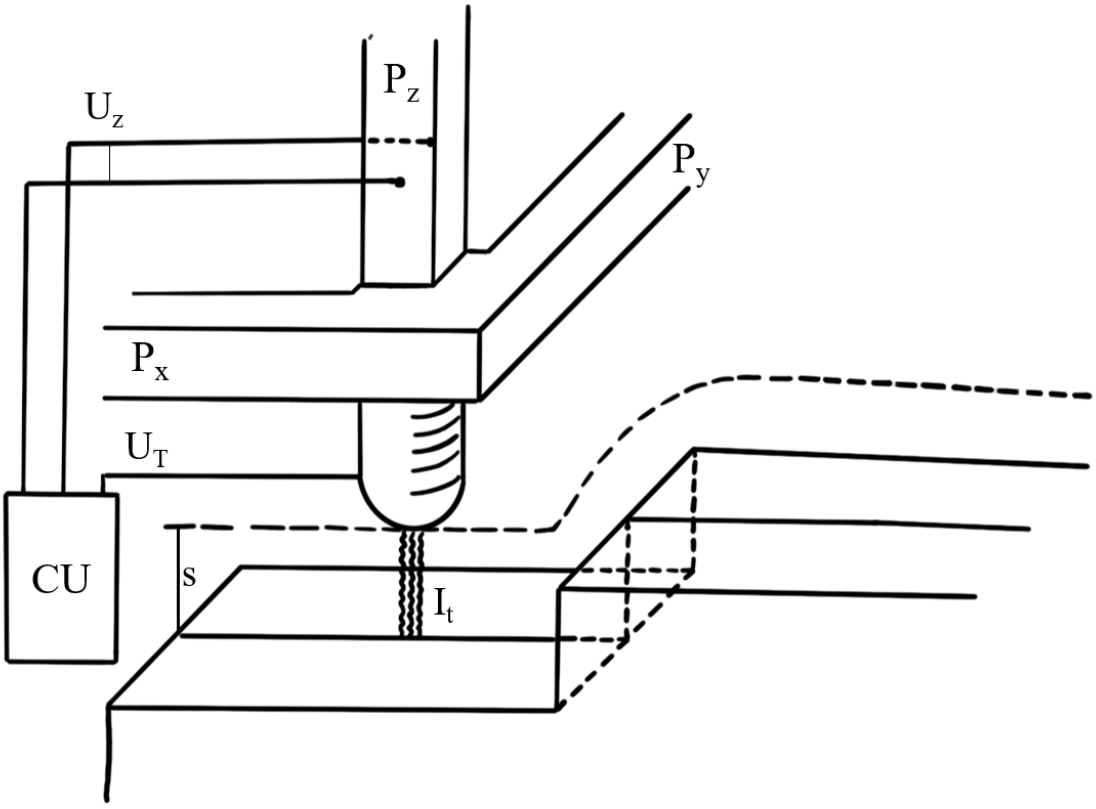

Figure 2.1: The principle of operation in STM. The piezo drives, P_x and P_y scan the metal tip over the surface. The control unit (CU) applies a voltage, U_z to the P_z piezo drive. The tunnelling current I_t is maintained using the voltage, U_t [83].

2.1.2 Elastic Tunnelling Through a One-Dimensional Rectangular Potential Barrier

The backbone theory behind STM is quantum mechanical tunnelling. In contrast to other transport mechanisms, such as diffusion or drift, quantum mechanical tunnelling cannot be explained via classical physics. For example, consider a microscopic particle like an electron trying to cross a one-dimensional potential barrier, as presented in ***Figure 2.2***. In classical physics, the electron is considered a particle. A particle would only be able to traverse the potential barrier by surmounting it. To do so, the electron would require energy greater than the barrier's height. However, in quantum mechanics, the electron can be treated as either a wave or a particle. When the electron's wave nature is accounted for, the electron is capable of crossing the barrier even when its energy is below that of the barrier. [83]

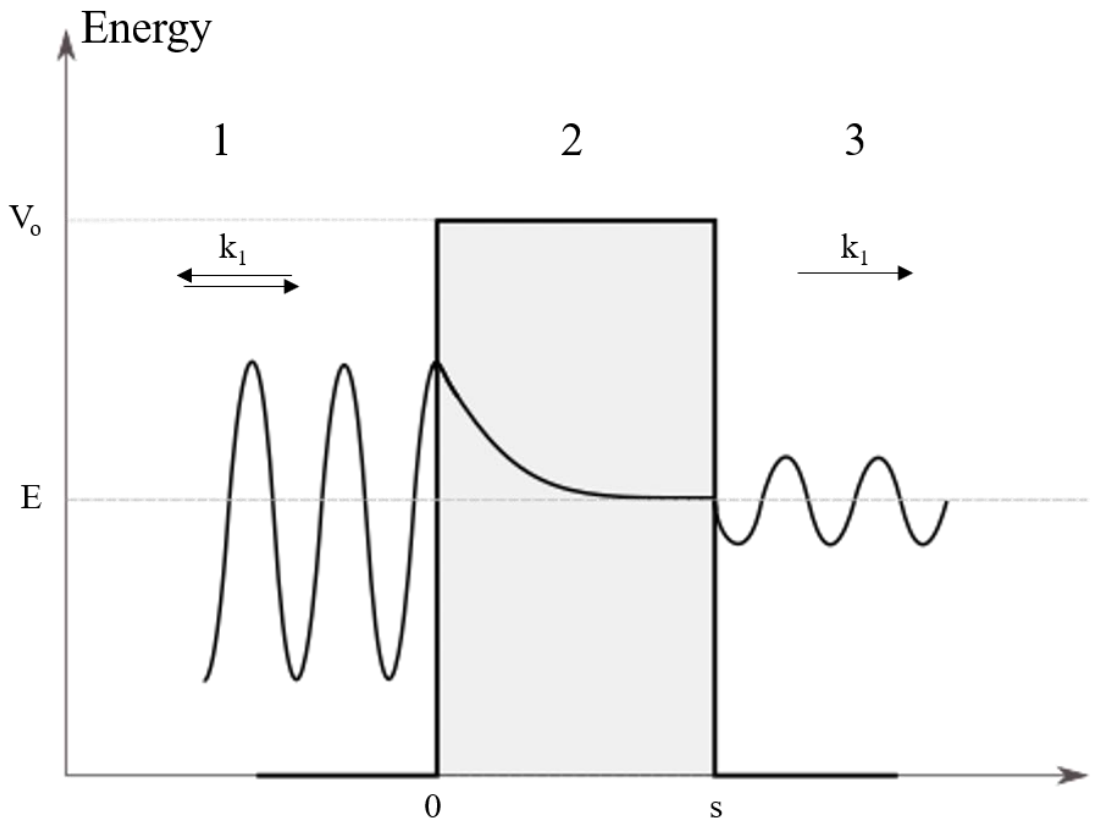

Figure 2.2: Schematic of a one-dimensional rectangular potential barrier with a height V_o and a width s. Region 1 and Region 3 represent the tip and the sample. Region 2, which contains the barrier, represents the vacuum gap between the two.

For an encroaching electron with energy (E) and mass (m), transmission across the barrier can be explained via the time-independent Schrödinger equation. Prior to encountering the barrier, the potential V(z) is 0, and the Schrödinger equation takes the form;

$$-\frac{\hbar^2}{2m}\frac{d^2\psi_1}{dz^2} = E\psi_1 \qquad 2.1$$

here $\hbar$ is the reduced Planck's constant, and ψ_1 is the wavefunction of the incident electron such that;

$$\psi_1 = Ae^{ikz} + Be^{-ikz} \qquad 2.2$$

where A and B are the amplitudes of the incident and reflected waves, respectively, and k is the wave vector.[83]

$$k^2 = \frac{2mE}{\hbar^2} \qquad 2.3$$

When the electron enters the barrier, the potential changes from 0 to V_0. The Schrödinger equation changes to;

$$-\frac{\hbar^2}{2m}\frac{d^2\psi_2}{dz^2} + V_0\psi_2 = E\psi_2 \quad 2.4$$

$$\psi_2 = C'e^{ik'z} + D'e^{-ik'z} = Ce^{-\varkappa z} + De^{\varkappa z} \quad 2.5$$

here, C and D are the amplitudes for the transmitted wavefunction and reflected wavefunction, and $\varkappa$ is the decay constant.[83]

$$\varkappa^2 = -k'^2 = \frac{2m(V_0 - E)}{\hbar^2} \quad 2.6$$

Finally, the electron exits the barrier and the potential reduces back to 0. This changes the Schrödinger equation again;

$$-\frac{\hbar^2}{2m}\frac{d^2\psi_3}{dz^2} = E\psi_3 \quad 2.7$$

$$\psi_3 = Fe^{ikz} \quad 2.8$$

here, F is the amplitude of the transmitted wavefunction. The relation between the incident wave and transmitted wave amplitudes can be found by matching the equations ψ_j and their first derivatives at the discontinuity points for the potential V(z), given at position z=0 and z=s. [83]

The transmission coefficient is the ratio of the transmitted current density and the incident current density, which is given by;

$$T = \left|\frac{F}{A}\right|^2 = \frac{4k^2\varkappa^2}{(k^2+\varkappa^2)^2 sinh^2(\varkappa s) + 4k^2x^2} \quad 2.9$$

For a strongly attenuating barrier ($\varkappa$s >> 1), the transmission barrier coefficient becomes;

$$T \approx \frac{16k^2\varkappa^2}{(k^2+\varkappa^2)^2} \cdot e^{-2\varkappa s} \quad 2.10$$

The transmission barrier coefficient shows a non-zero possibility that an electron will tunnel through the potential barrier when it has energy lower than the potential barrier. Meanwhile, the factor $e^{-2\varkappa s}$, expresses the strong dependence the transmission coefficient (T) has on the barrier width (s). It is this sensitivity that lends itself to STM's high spatial resolution. [83]

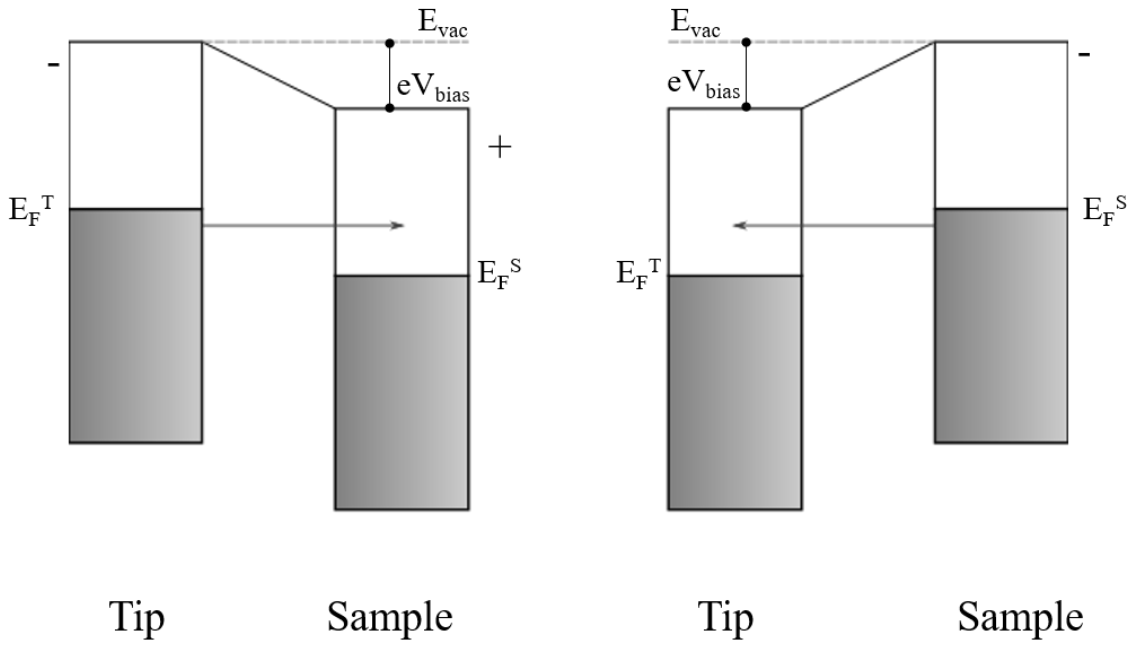

Figure 2.3: Energy window diagram for a tip and a sample. Tunnelling direction is dependent on the bias polarity. (a) The positive bias is applied to the sample. Electrons will tunnel from filled states (grey) of the tip to empty states (white) in the sample. (b) The positive bias is applied to the tip. Current moves from filled sample states (grey) to empty tip states (white).

When a bias voltage is applied between the tip and the sample, a tunnelling window is established. The tunnelling window determines what states are accessible in STM. The direction of the current depends on the polarity of the applied bias. This is represented in ***Figure 2.3***. If a positive bias is applied to the sample, E_F^S shifts by eV below the tip E_F^T level. From first-order perturbation theory, the tunnelling current can be expressed as

$$I = \frac{4\pi e}{\hbar}\sum_{\mu\nu}[f\left(E_\mu^T - E_F\right) - f(E_\nu^S - E_F)\left|M_{\mu\nu}\right|^2\delta\left(E_\nu^S - E_\mu^T - eV_{bias}\right) \quad 2.11$$

where $f\left(E_\mu^T - E_F\right)$ is the Fermi function of the tip. The density of states (DOS) is the number of electrons per unit volume per unit energy.

$$\rho(E) = \sum_n \delta(E - E_N) \rightarrow \int \rho(E)dE \quad 2.12$$

The net tunnelling in terms of the DOS of the tip and the sample is then:

$$I = \frac{4\pi e}{\hbar}\int_0^{eV} \rho_s\,(E_F + \epsilon)\rho_T(E_F + \epsilon - eV)|M(\epsilon)|^2 d\epsilon \qquad 2.13$$

where M(ϵ) is the energy-dependent tunnelling matrix element. The energy dependence comes from the wavefunctions via their decay constants.

Higher contributions to the transmission probability and the tunnelling current comes from the topmost states of the energy interval. In the case of a positive bias applied to the sample, the sample's Fermi level is lowered by eV with respect to the tip's Fermi level. Tunnelling is allowed from the filled states of the tip at E_F to the empty states at the sample E_F + eV. Similarly, if the sample is negatively biased, electrons will tunnel from the filled states of the sample near E_F to the empty states of the tip. Since the empty states of the tip contribute to the tunnelling current in determining the sample's DOS, the tip's DOS must be flat. [83]

2.1.3 System Overview

The STM system can be broken down into three main chambers; the load lock, the preparation chamber and the STM chamber. These are highlighted in ***Figure 2.4***. The load lock is the point of entry and exit for the UHV system. The load lock is connected to a HiPace 300 turbo molecular pump (TMP) to evacuate the chamber down to vacuum. The TMP is supported by the MD-4-NT Vaccuubrand diaphragm roughing pump. The chamber also contains a leak valve that allows a controlled amount of nitrogen gas to enter the chamber to vent it up to atmospheric pressure. A transfer arm, labelled in ***Figure 2.4***, is also contained within the load lock. The transfer arm moves samples from the load lock into the preparation chamber. The chamber is surrounded by heating tape and aluminium foil that allows the load lock to be baked independently from the rest of the system.

The preparation chamber is the main chamber used for sample preparation and sample storage. The preparation chamber contains a manipulator arm that manoeuvres samples around the preparation chamber and can transfer samples to the STM chamber. The manipulator arm is highlighted in ***Figure 2.4***. The manipulator bellows are connected back to the load lock so the arm's pressure can be maintained using the TMP and roughing pump. The manipulator arm also serves as a method of sample manipulation. The two stages present in the arm have electrical contacts, allowing for sample annealing. Other preparation methods attached to this chamber are two sputter guns, which allow for sample cleaning by ion bombardment and a thermal evaporator to decorate sample surfaces. In

conjunction with this, the preparation chamber also houses alternative methods for sample characterisation, such as low energy electron diffraction (LEED) apparatus from Specs. Samples that are not in the head can be stored in the sample storage unit. The storage unit contains five spaces that can hold samples or tips for the system. A wobble stick attached to the chamber is used to transfer samples to and from the storage stage and the manipulator arm. A hot filament or ion gauge measures the pressure in the chamber. This chamber's pressure is maintained by an ion pump and titanium sublimation pump (TSP) combination. During sample manipulation, the chamber can be pumped by a HiPace 80 TMP that is connected directly to the chamber and to the diaphragm pump.

The final chamber in the system is the STM chamber. This chamber is predominantly used to house the microscope assembly. A cryo-shield surrounds the assembly to maintain the temperature of the head. Resting above the chamber is a 28-litre bath cryostat. This is highlighted in ***Figure 2.4***. The cryostat is divided into two chambers. The cryostat can be filled with either liquid nitrogen or liquid helium for 77 K or 4 K experiments. Sitting outside the cyroshield is another sample storage unit with five additional spaces for further storage. This chamber also has a wobble stick to allow samples to be moved between the STM head, the storage unit, and the manipulator arm. This chamber's pressure is monitored by an ion gauge and is maintained by an ion pump–TSP combination.

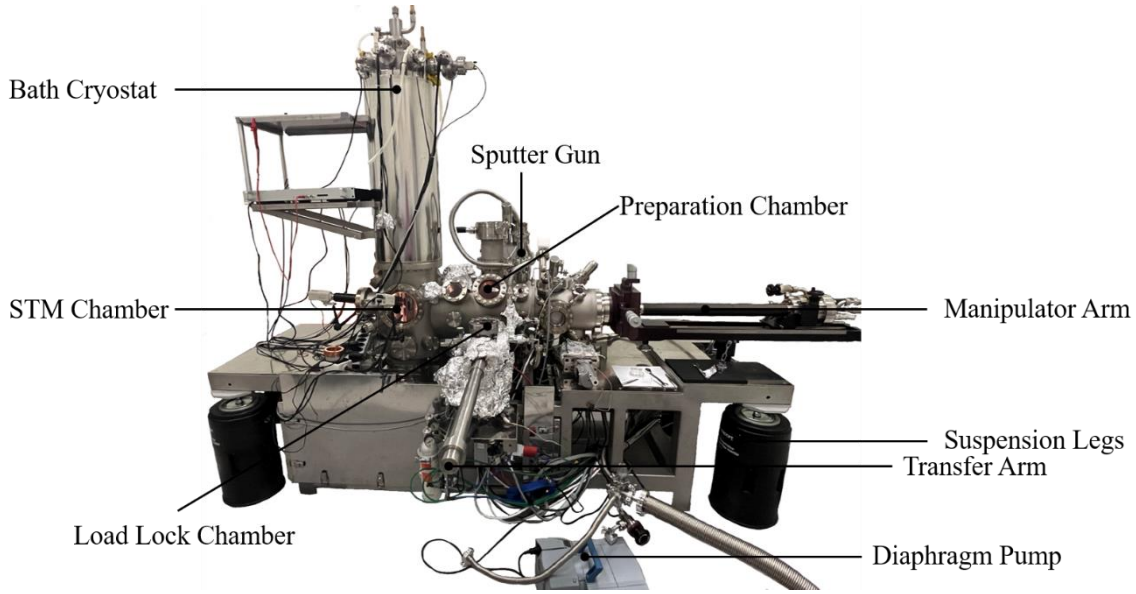

Figure 2.4: Image of the UHV LT-STM system. The UHV system contains three chambers; the load lock, the preparation chamber and the STM chamber. Sitting above the STM chamber is the bath cryostat which allows for LT measurements to be taken. The whole system is vibrationally isolated using four suspension legs. Sample movements between chambers are completed using the transfer arm and manipulator arm.

2.1.4 Creating a tip

STM tips were created using 0.25 mm diameter tungsten wire. A sharp point is created at the end of the wire by DC drop-off etching. In this method, a tungsten wire is partially submerged in a 2 M NaOH solution by a micrometre positioner. Surrounding the wire is a glass tube and a stainless-steel loop. A voltage is applied between the wire and the loop, creating an electrochemical circuit where the tip is the anode, and the loop is the cathode. The anodic reaction (Oxidation) is given as [84]

$$W + 8OH^- \rightarrow WO_4^{2-} + 4H_2O + 6e^- \quad 2.14$$

and the cathodic reaction (Reduction) is;

$$6H_2O + 6e^- \rightarrow 3H_2 + 6OH^- \quad 2.15$$

The glass tube surround is used to protect the meniscus at the wire from disturbances caused by the hydrogen gas bubbles that evolve at the stainless-steel loop. Further disturbances from vibration are mitigated using a vibration isolation table.

Initially, the full available length, approximately 8 mm, of the wire was submerged in the solution with a bias voltage of 10 V applied to remove the surface oxide. The wire was then removed from the solution, and only 3 mm of the wire was resubmerged into the solution with an applied bias of 5 V already employed. As the reaction occurs, WO_4^{2-} ions flow downwards along the length of the submerged section of wire. The flow of ions shields the lower section from being etched. As a result, the section just below the meniscus has the fastest etch rate, forming a neck at the point just below the meniscus. At a certain point, the neck becomes so narrow it can no longer support the weight of the lower section of wire, and it breaks off creating an extremely sharp tip that can be used for scanning. Any etching that occurs after drop-off causes the tip to blunt. A control circuit is used to stop the applied bias when a significantly sizeable current differential is detected. The newly formed tips were submerged in deionised (DI) water to remove residual hydroxide ions. The tips were then fitted to a tip holder and loaded into the STM system.

2.1.5 Preparing a sample

8 mm x 4 mm samples were cut from larger samples using a diamond-tipped scribe on the silicon or sapphire side. The samples were then cleaned by repeated wash cycles of isopropyl alcohol (2-Propanol for HPLC, 99.9%, Sigma Aldrich), followed by drying under nitrogen flow. The samples were installed into an STM sample holder, as seen in ***Figure 2.5***. The sample and the holder were cleaned by three cycles of IPA (2-Propanol for HPLC, 99.9%, Sigma Aldrich) rinsing followed by nitrogen drying. The sample holder and sample were submerged in acetic acid (Glacial, ReagentPlus®, ≥ 99%, Sigma-Aldrich, 1003545482) for 30 seconds to remove the sample's oxide layer. The sample was immediately transferred from the acetic acid into the transfer arm of the load lock chamber. The load lock was slightly over-pressured with nitrogen to keep the sample in an inert environment until the system is pumped down. The samples were then baked overnight at 100 °C. The sample was moved into the preparation chamber. All samples underwent a cleaning anneal at 2.0 - 2.2 A with 3.2 - 5.5 V for 20 minutes. Subsequent anneals to optimise the surface were done between 1.0 A and 2.2 A for 20 minutes. The samples were sputter cleaned between optimisation anneals using 1.4 x 10^{-7} to 1.1x10^{-7} mbar of argon. The energy of the bombardment was 1,000 kV for 5 minutes. The leakage current was 1.3 μA. The sputter was rastered over an eight-millimetre by eight-millimetre raster size.

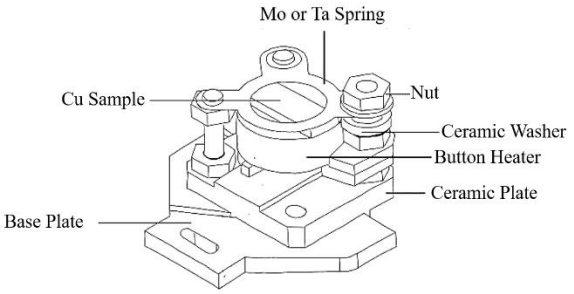

Figure 2.5: Schematic of the sample holder assembly used for experiments. The sample is placed on top of a button heater which makes an electrical connection with the sample holder on the manipulator arm. The button heater anneals samples in the system.

2.2 ATOMIC FORCE MICROSCOPY

2.2.1 Theoretical Background & Operating Principle

The concept of AFM was developed by Binning, Quate, and Gerber[85] during the creation of scanning tunnelling microscopy (STM). In STM, a variety of forces were found to influence the interactions between an atomically sharp probe and a conductive sample. Binning was the first to recognise that such forces could also give information regarding a sample surface. As such, a second form of SPM, known as atomic force microscopy or scanning force microscopy (SFM), was created in 1986. Atomic force microscopy utilises the repulsive and attractive forces between a probe and a sample surface to track surface

topography.[86] The operating principle behind AFM is a hybrid between two distinct characterisation techniques; surface force analysis and profilometry. [83]

When two electrically neutral and non-magnetic bodies are separated by a distance of a few nanometres, van der Waals (VDW) forces dominate the interaction force between them. Surface force analysis (SFA), invented by Tabor and Winterton[87], [88] in 1969, studies VDW forces over a range of separations, between 1 nm to greater than 100 nm, to study the force interaction between two surfaces. In SFA two surfaces are made to approach one another using piezoelectric crystals. The separation is controlled with sub-Ångström accuracy using an optical technique of multiple beam interference fringes.[83] The resulting force is measured by the deflection of a spring (Δz), which has a mica sheet mounted atop it. According to Hooke's law, if the spring constant is known, the force can be derived by ***Equation 2.16.***[83]

$$F = c \cdot \Delta z \qquad 2.16$$

In the surface force apparatus, the stiffness of the spring can be varied to allow for a wide range of forces to be detected. A force resolution of 10^{-8} N is achievable using a relatively soft spring.[83]

The second technique which inspired AFM is surface profilometry[89]. This technique was designed as a means to study the surface roughness of materials. In profilometry, a sharp stylus is rastered over a sample surface. The stylus tip is in mechanical contact with the surface. The tip position in Z is measured as a function of X and Y by maintaining a constant force, usually in the range of 10^{-4} N. Due to the loading force, profilometry tips are approximately 1 μm wide. Larger tips stop large local pressure, thereby minimising surface damage to the sample. However, larger tips also mean lower lateral resolution. As a result, reliability in the roughness values determined by topographic maps in surface profilometry is poor.[83]

Binning combined the sensitivity of surface force analysis with the spatial capabilities of surface profilometry to build atomic force microscopy[85]. In this system, a sharp surface probe is mounted on a cantilever-type spring. The tip is separated by a few nanometres from the surface. The force interaction between the tip and the sample deflect the cantilever according to Hooke's law ***Equation 2.16***.[83] The spring constant, c, in this context, is replaced by k, the cantilever force constant, which is analogous to the force constant. [86]

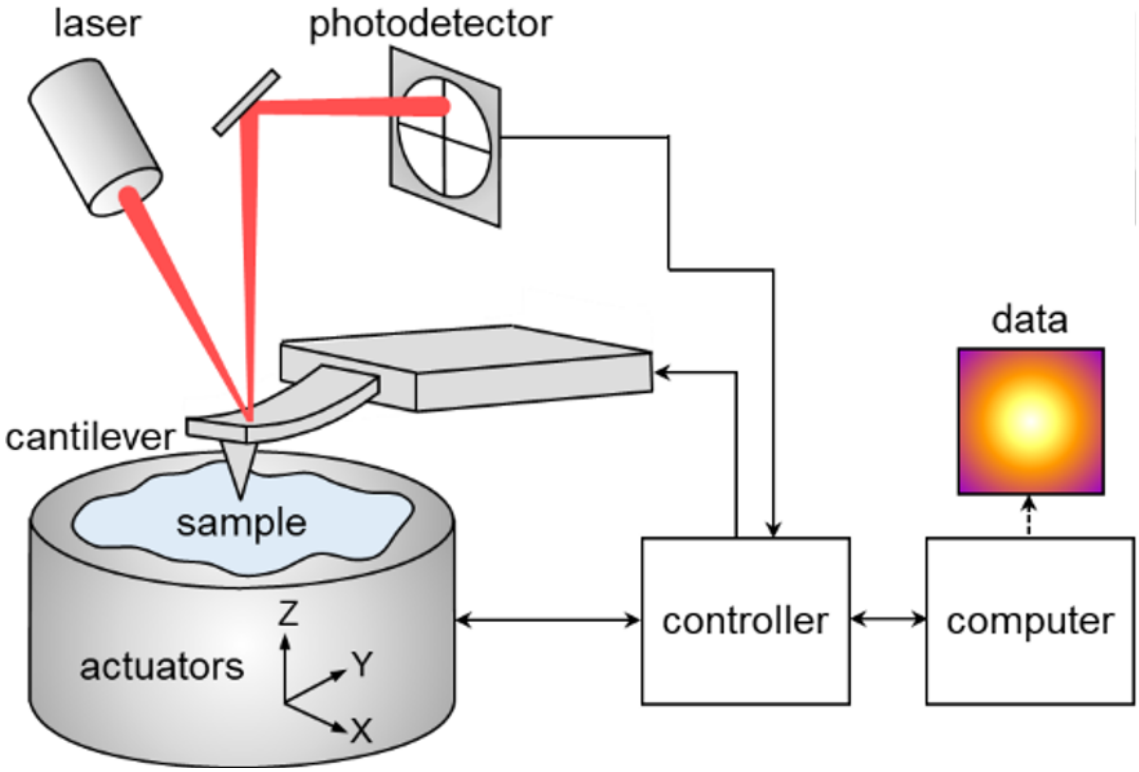

Figure 2.6: Illustration of atomic force microscopy. The deflection of the cantilever is recorded by a photodetector [90].

Deflection can be measured by either capacitance detection, optical detection via a laser-photodetector apparatus or an STM tunnelling setup. ***Figure 2.6*** [90] illustrates the optical detection method for deflection as this is the deflection measurement system utilised in the Asylum MFP-3D AFM employed within these studies. The laser deflection method requires an AFM tip with a reflective back surface. This can be achieved by coating the back of the tip with a thin metal film. In this method, a laser beam incident on the back of the tip is reflected onto a photodetector. A change in force causes the tip's deflection to change. As a result, the angle at which the incident beam hits the back of the tip changes. The change in the incident beam angle also causes the reflected beam angle to change. As a result, the position the reflected beam strikes the photodetector changes allowing for the change in force between the tip and sample to be measured.

A topographic map of a sample surface is obtained by maintaining the force between the tip and the sample as the tip is rastered over the sample surface. This mode is the simplest operation mode of AFM and is called contact mode or normal force mode. Here, the tip is in mechanical contact with the sample such that the repulsive forces between the tip and the sample cause the tip to deflect. The deflection is maintained throughout rastering by a feedback loop. If the deflection changes, a voltage is applied to the z-piezo. This changes the position of the tip or sample until the force setpoint (deflection) is reestablished. The change in the Z-position is recorded as a function of X and Y. In contact mode, AFM operates like the stylus profilometer. However, the forces used in the AFM are considerably smaller, usually between 10^{-6} to 10^{-10} N. Alternatively, the tip can also be kept a couple of nanometres above the surface, where attractive VDW forces can deflect the cantilever. This is known as the non-contact mode.[83]

The critical component in the AFM is the cantilever. In order for the system to have high sensitivity in Z, a large deflection for a given force is needed. As such, the spring should be as soft as possible. The resolution in X and Y is determined by the size and shape of the probe tip. Commercial probes are made using silicon or silicon nitride with tip radii as small as 10 nm. The most common radius being somewhere between 20 and 40 nm. In order to obtain atomic resolution, a radius of 20 nm or below is required. The tip also needs a high resonant frequency in order to minimise its sensitivity to mechanical vibrations during scanning. The resonant frequency of a spring is determined by ***Equation 2.17.***[83]

$$\omega_0 = \left(\frac{c}{m}\right)^{1/2} \qquad 2.17$$

Here, c is the spring constant, and m is the effective loading of the spring. From ***Equation 2.17***, it can be seen that a large value of ω_0 and low spring constant, or a soft cantilever, requires the mass and geometrical dimensions of the cantilever to be as small as possible.[83]

Since AFM relies on the forces between the tip and the sample, AFM is applicable to insulators as well as semiconductors and conductors. AFM is also versatile in terms of its operating environment. While STM requires a vacuum for operation, AFM can be performed in vacuum, atmosphere and in liquids. AFM probes a variety of forces, both attractive and repulsive. For example, AFM can probe VDW, ion-ion repulsion, electrostatic, capillary, adhesion, and frictional forces.[83] This variety has matured into a number of advanced techniques and operation modes for AFM.

Some of the most popular scanning modes involve oscillating the cantilever during scanning. One such example used in this project is tapping mode. In this mode, the tip is oscillated vertically with an amplitude of 50 to several hundred nanometres. During the oscillation, the tip contacts the sample on the down stroke. Feedback in this mode is slightly different from contact mode. In this mode, the photodetector monitors the oscillation amplitude. The amplitude changes depending on how close the tip is to the sample. The user inputs a setpoint for the oscillation amplitude. The feedback loop tries to maintain the setpoint oscillation amplitude by varying the tips' Z-position. The Z-position of the tip is plotted as the tip rasters across the surface. The generated topographic image, much like contact mode, is generated by displaying the Z-position as a function of X and Y. This mode has the benefit of mitigating the shear forces that are exerted on a sample when a tip is rastered over the sample in contact mode.

Tapping mode can also operate in the attractive force regime, known as non-contact tapping mode. In this mode, the tip is held in proximity to the sample's surface. The tip does not make contact with the sample at any point during its oscillation. Instead, the tip’s oscillation is altered by attractive force interactions with the surface. The change in the oscillation reveals information about the vertical height of the sample. In this mode, the user also defines the oscillation amplitude setpoint. As the tip moves across the sample, a change in the oscillation is compensated for with a change in Z-position. The Z-position is recorded as a function of the X and Y position. In either mode, atomic resolution can be achieved. The advantage of non-contact mode is the fact that non-contact mode can be used on soft samples such as biological specimens.

2.2.2 System Overview

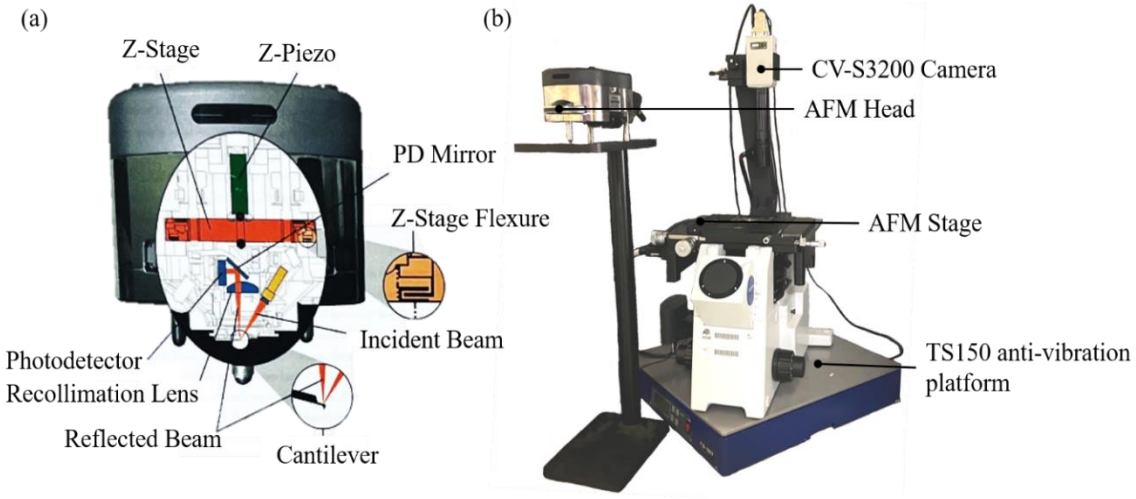

Figure 2.7: (a) Schematic of key components within the AFM head. Including the generation of the laser which is focused onto cantilever and reflected back to the photo-detector using a PD mirror [91]. *(b) The current configuration of the Asylum AFM MFP-3D.*

The system used for the AFM imaging of samples was the Asylum MFP-3D system. The system can be divided into two sections, the head and the stage, as shown in ***Figure 2.7(b)***. In the head of the system, there is a laser, an adjustable detector mirror, a photodetector, a Z-piezo tube, an X-Y piezo stage and a cantilever holder. These components are highlighted in ***Figure 2.7(a)***. The laser arrangement is made up of a laser diode to produce the beam, a collimator to shape the beam and limit the maximum field size of the beam, a focusing lens to focus the beam, and a base plate. There are also X and Y laser diode adjustment wheels that allow the beam to be positioned over the cantilever. The laser reflection and tip are viewed manually via the CV-S3200 Analog Colour Camera mounted above the AFM head. A PD mirror positions the reflected laser spot onto the four photodetector elements. This mirror is adjustable so the laser signal can be maximised, and the deflection of the laser on the PD can be minimised. The photodetector mirror is adjusted via a wheel located on the head.[91]

The photodetector assembly itself consists of four photo-detectors. Differing combinations of these quadrants provide different information about the sample, depending on the operating mode. In all modes, the four elements combine to form the SUM signal. The amplified difference signal between the top two and bottom two elements measures cantilever deflection. Meanwhile, the amplified difference signal between the sum of the two left and two right photodiodes provide a measure of the cantilever's torsion. [91]

The Z-piezo in the Asylum system is used to move the cantilever assembly up and down. The Z-piezo makes up one part of the Nano-Positioning System (NPS). In the NPS, a feedback loop is used to maintain the cantilever deflection. When the deflection changes the NPS system makes the Z-piezo expand or contract to counteract the change. Another sensor called the NPS sensor, measures the distance of the cantilever assembly from the sample, which is used to form AFM images. [91] To bring the head into contact with the sample, the head has three legs controlled via wheels located above each leg on the head.

Like the Z-piezo, the X-Y piezo stacks move the cantilever assembly in X and Y. The X and Y stacks vary from the Z stack in that they have a longer range, and they use flexure mechanics to amplify their motion. The final component of the AFM head is the cantilever holder. The main function of the cantilever holder is to clasp the cantilever in position for use. To do so, the holder uses a stainless-steel tongue assembly that is screw-tightened to hold the tip. The tip holder also includes the cantilever piezoelectric stack and the electrical contacts for the drive circuits used in tapping modes. [91]

The stage system in the Asylum allows for manual sample movement via screw gauges that control the sample stage's X and Y movement. Samples are held on the stage, by either a clip assembly or via magnets. If the sample is smaller than 4 cm on one edge, the sample must be mounted onto a glass slide in order to be held in place. AFM is exceptionally susceptible to vibration. As a result, the system is both acoustically and vibrationally isolated. The isolation system is comprised of a TS150 anti-vibration platform upon which the microscope rests. This is labelled in ***Figure 2.7(b)***. An Integrated Dynamics Engineering acoustic enclosure surrounds the AFM system and the air table. The acoustic enclosure door can be raised to access the instrument and lowered during operation. [91]

2.2.3 Sample & Tip Preparation

The samples used in these studies were 2 cm x 2 cm squares. As a result, they had to be mounted to hold them in place on the AFM stage. For the Asylum AFM, the samples were mounted onto the centre of a glass slide using carbon tabs (PELCO Tabs, Carbon Conductive Tabs, 12 mm OD). The glass slide was held in place on the sample stage by two magnets positioned at either end of the slide. The tips used for AFM imaging were Budget Sensors Tap150Al-G. The tips had a conical shape with a radius < 10 nm. The detector side of the probes were coated in 30 nm thick aluminium.

2.2.4 AFM Calibration

The AFM calibration was tested using a calibration sample from Digital Instruments (P/N 498-000-026). The reference sample is a series of square pits with a pitch of 10 µm and a depth of 200 nm. Analysis of the reference sample images using Igor Pro gave squares of width of 5 µm, spaced 5 µm apart with a 200 nm depth. As a result, no adjustment of the system was required.

2.2.5 Determining Grain Size Distribution

To determine the average grain diameter, line profiles were extracted from 2, 5 and 10 µm AFM images. The line profiles were used in conjunction with the image to measure the width of the individual grains in the x direction. Each grain measured was labelled with the image, line profile number and order number in which it was measured. The measured diameters of the grains were used to determine the mean grain diameter and the standard deviation of grain diameters. The grain diameters were also used to create the histograms shown in ***Chapter 5***.

2.3 FOUR POINT PROBE

2.3.1 Theoretical Background & Operating Principle

The specific electrical resistance, also called resistivity (ρ) of a solid, is a fundamental physical property of a material. It is used to classify a material as a conductor, semiconductor or insulator and ranges from 10^{-8} to 10^{16} Ω cm. When an electric field, E, is applied to a material, an electric current is induced. Assuming diffusive transport and an isotropic material, the resistivity of the material can be defined by the ratio of the electric field and the current density, J.[92]

$$\rho = {}^{E}/_{J} \qquad 2.18$$

The electric field is given in units V cm^{-1} and the current density uses A cm^{-2}. Dividing these gives the resistivity of a material, which is Ω cm. In experiment, the resistance, R, is measured as opposed to the resistivity. Resistance is deduced from the ratio of an applied bias, V and the responding current, I. [92]

The simplest method to measure resistance is by measuring the voltage drop between two electrodes when a current is injected into the sample. The problem with this layout is that the measured resistance includes contributions from the contact of the probes

with the sample. The probes act as series resistors with the sample. This problem was first identified in 1915 by Frank Wenner[93] when trying to measure the resistivity of the planet. Wenner proposed a setup that contained four probes instead of two. The four-probe method minimises the contributions of the contacts. The Wenner method moved from geophysics to microelectronics in 1954 when Leopoldo Valdes[94] used a four-probe geometry to measure the resistivity of a semiconductor wafer. In 1975, the four-probe measurement was widely accepted into the semiconductor industry with a reference procedure in the American Society for Testing and for Material Standards. [92]

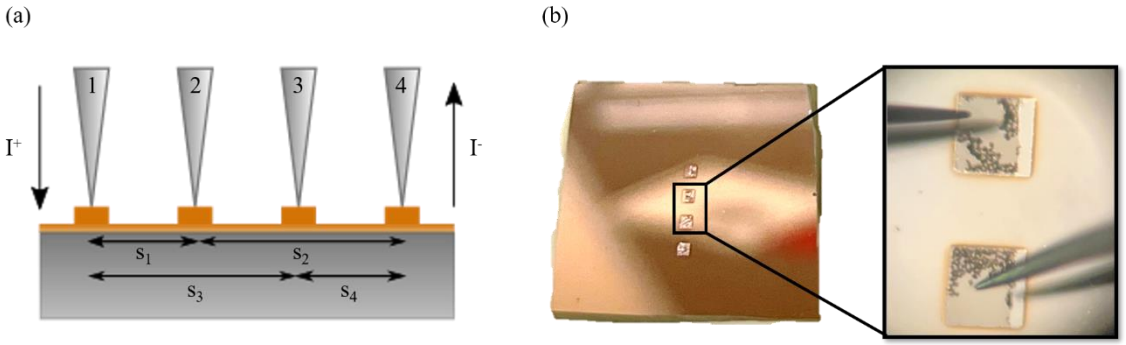

Figure 2.8 (a) Schematic of a linear four point probe array. The probes are equidistantly spaced. (b) A Cu(50 nm)/Ta(7 nm)/Si(100) sample used for resistivity measurements. After processing, four thick copper pads are deposited on the sample to act as a guide for probe positioning and to ensure the probes do not pierce through the copper film into the doped silicon.

In a linear four-probe configuration, shown in ***Figure 2.8(a)***, the voltage drop between two inner contacts is measured while a set current is injected into a sample via two outer probes. The ratio of voltage to current gives the resistance of the sample. The conversion of resistance to resistivity depends on the sample's dimensions and geometry as well as the probe's geometry and spacing. The starting model for this type of measurement is a semi-infinite 3D material. The four electrodes are spaced equally apart in a straight line, known as the in-line array. The material's resistivity is given by ***Equation 2.19*** [92].

$$\rho_{3D}^{line} = 2\pi s \frac{V}{I} \qquad 2.19$$

Here, V is the voltage drop between the two inner probes, I is the current injected into the sample through the two outer probes. ***Equation 2.19*** is derived by analysing the current. The current, +I, is injected into the sample. The current spreads spherically in a homogenous, isotropic material. At a distance, r_1, from the first electrode, the current density can be expressed as

$$J = \frac{I}{2\pi r_1^2} \tag{2.20}$$

The associated electric field, or the gradient of the potential, can be written as

$$E(r_1) = \rho J = \frac{\rho I}{2\pi r_1^2} = -\frac{dV}{dr} \tag{2.21}$$

The potential at a point, P, can be determined by integrating both sides of ***Equation 2.21*** [92].

$$\int_0^V dV = \frac{I\rho}{2\pi}\int_0^{r_1} \frac{dr}{r^2} \Rightarrow V(P) = \frac{I\rho}{2\pi r_1} \tag{2.22}$$

In a linear configuration, the voltage drop between the two central probes can be expressed as

$$V(P) = \frac{I\rho}{2\pi r_1} - \frac{I\rho}{2\pi r_2} = \frac{I\rho}{2\pi}\left(\frac{1}{r_1} - \frac{1}{r_2}\right) \tag{2.23}$$

Applying this to the two inner probes of the inline geometry gives;

$$V = V_2 - V_3 = \frac{I\rho}{2\pi}\left[\left(\frac{1}{s_1} - \frac{1}{s_2}\right) - \left(\frac{1}{s_3} - \frac{1}{s_4}\right)\right] \tag{2.24}$$

When the probes are all equally spaced, s_1 and s_4 are equal to s, while s_2 and s_3 are equal to 2s. This simplifies to give ***Equation 2.19*** [92].

When the thickness of the sample, h, becomes small in comparison to the separation between the probes, the semi-infinite 3D material behaves as an infinite 2D sheet. The current in this model can be assumed to spread cylindrically as opposed to spherically. The current density, in this case, is given by;

$$J = \frac{I}{2\pi r h} \tag{2.25}$$

The electric field also changes to;

$$E(r_1) = \rho J = \frac{\rho I}{2\pi r h} = -\frac{dV}{dr} \tag{2.26}$$

The steps taken between ***Equation 2.22*** and ***Equation 2.24*** are repeated, providing a logarithmic dependency for the voltage drop between the two inner probes [92]

$$V = V_2 - V_3 = \frac{I\rho}{2\pi h} ln\left(\frac{s_2 s_3}{s_1 s_4}\right) \tag{2.27}$$

For the case of equally spaced in-line four probe geometry, the resistivity is given by;

$$\rho_{2D}^{line} = \frac{\pi h}{ln2}\frac{V}{I} \quad (2.28)$$

As can be seen from ***Equation 2.28***, the resistance measured is not dependent on the probe spacing. In these samples, it can be assumed that the resistivity is constant[95]. As a result, the bulk resistivity is replaced by the so-called sheet resistance, R_{sh}. The sheet resistance is defined as;

$$R_{sh} = \frac{\rho}{h}\ (\Omega) \quad (2.29)$$

The dimension of the sheet resistance is measured in ohms but is also denoted as Ω sq^{-1} to distinguish it from resistance. The origin of the unit comes from the fact that a square sheet of resistance 1 Ω sq^{-1} would have an equivalent resistance, regardless of its dimensions. This can also be expressed using the resistance of a rectangular rod of length, l, and cross-section, A=wh. The rod's resistance is given as $R = {\rho l}/{A}$. This simplifies to $R = R_{sh}$ when $l = w$. [92]

It is important to note that real specimens are not infinite in either the vertical or the lateral directions. As a result, the equations derived previously need to be amended to account for finite sample geometries. Likewise, correction factors need to account for the influence of the sample boundary. In the case of finite and arbitrarily shaped samples, the bulk resistivity is expressed as;

$$\rho = F\frac{V}{I} \quad (2.30)$$

Where F is separated into three separate geometric correction factors: F_1, F_2 and F_3. F_1 accounts for the finite thickness of the sample, F_2 accounts for the alignment of the probes in the proximity of a sample's edge, and F_3 accounts for the finite lateral width of the sample. F is dimensionally equivalent to length, but F_1, F_2 and F_3 are defined as being dimensionless. For anisotropic samples, further correction factors must be considered. Several mathematical approaches have been considered to study correction factors. These include the method of images, conformal mapping theory, solving Laplace's equations, expansion of the Euler-Maclaurin series and the finite element method (FEM). [92]

The resistivity of an infinite sheet of finite thickness can be written formally as

$$\rho = R_{sh-2D}^{line} \cdot h \cdot F_1\left(\frac{h}{s}\right) = \left[\frac{\pi}{\ln 2}\frac{V}{I}\right] \cdot h \cdot F_1\left(\frac{h}{s}\right) \quad (2.31)$$

Here, R_{sh-2D}^{line} is the sheet resistance measured on an infinite 2D sheet. F_1 is a dimensionless function of the normalised sample which reduces to 1 as h approaches 0. A detailed derivation of the thickness correction factor was first given by Valdes[94] in 1958 using the method of images. The method of images results in a power series, which is unsuitable for numerical computation. Albers and Berkowitz[96] approximated a solution of Laplace's equation. In the case of a four-probe line array on an infinite sheet of thickness, h, the correction factor can be written as[97];

$$F_1 = \frac{\ln 2}{\ln\left\{\left[sinh\left(h/s\right)\right] / \left[sinh\left(h/2s\right)\right]\right\}} \tag{2.32}$$

The correction factor, F_2, accounts for the positioning of the probes in proximity to an edge on a semi-infinite sample. A reflecting boundary can be mathematically modelled by inserting two current image sources of the same sign at a distance, -d for probe four and –(d+3s) for probe one. Applying this to ***Equation 2.22***, the potential at probe two can be rewritten as;

$$V_2 = \frac{I\rho}{2\pi}\left(\frac{1}{s} - \frac{1}{2s} - \frac{1}{2d+s} + \frac{1}{2d+5s}\right) \tag{2.33}$$

A similar equation is obtained for probe three. The total voltage drop can be rewritten as;

$$V = \frac{I\rho}{2\pi s}\left(1 + \frac{s}{2d+s} - \frac{s}{2d+2s} - \frac{1}{2d+4s} + \frac{1}{2d+5s}\right) \tag{2.34}$$

The bulk resistivity can be rewritten as;

$$\rho = 2\pi s \cdot \left(V/I\right) \cdot F_2 = \rho_{3D}^{line} \cdot F_2\left(d/s\right) \tag{2.35}$$

Where;

$$F_2 = \left(1 + \frac{s}{2d+s} - \frac{s}{2d+2s} - \frac{1}{2d+4s} + \frac{1}{2d+5s}\right) \tag{2.36}$$

When the probe distance from the boundary is four times the probe spacing, the correction factor, F_2, reduces to unity. The correction factor can reach a minimum of ½ when the four-probe array is aligned parallel to a sample edge. This would mean that the measured resistance could be increased by a factor of two compared to the semi-infinite 3D sample. [92]

The case of a four-probe setup positioned close to a single edge of the sample is an idealised approximation. The correction factor F_2 is insufficient for a realistic approximation. A third correction factor is applied. F_3 accounts for the entire effect caused

by all lateral boundaries of the sample. For certain sample geometries, such as circular samples, the correction factor can be calculated using theories such as conformal mapping or by transforming the circular sheet into an infinite half-plane. In the case of an inline probe set-up with a square sample geometry, the value of F_3 is determined empirically rather than by theory-based equations [98].

2.4 SAMPLE CREATION

2.4.1 Etching the Cu (50 nm)/Ta (7nm)/ Si (100) Samples

The samples used within this study were provided by Intel. The 50 nm thick nanocrystalline copper film samples were prepared using physical vapour deposition. The copper was deposited onto a 7 nm thick tantalum film that was coated onto a twelve-inch doped silicon wafer. Prior to any further modification, samples were cut from the parent wafer using a diamond scribe. Depending on use, the measurements cut were varied. Various etchants were attempted throughout this project to find an etchant which provided a reproducible etch rate and minimised the subsequent surface roughness. The specifics of each etch process are;

1. Submersion in a 0.89 M aqueous citric acid (99%, Sigma-Aldrich, C0759-1KG) solution up to 24 hr. The citric acid solution had a pH 1.45 ± 0.005. The solution was left aside in a clean, sealed vessel for 24 hours prior to use as an etchant.
2. The phosphoric acid electrochemical etch was created using a similar set-up to that of Moser et al. [99]. A schematic of the experimental setup is given in ***Figure 2.9***. The set-up consisted of a 250 mL beaker, a copper mesh cathode with a 65 mm height and a circumference of 202 mm (~ 64 mm diameter). The cathode was connected to a Keithley 2450 source meter via a copper crocodile clip. The anode consisted of the sample and a copper crocodile clip. All experiments were completed at room temperature, with a stirring frequency of 200 revolutions per minute (RPM). The

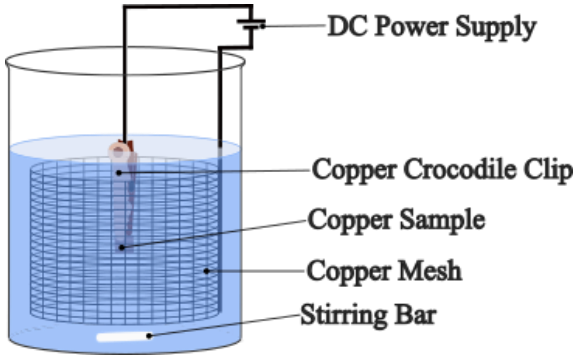

Figure 2.9: Schematic of the electrochemical etch setup used for etching.

etchant used was a 0.43 M aqueous solution of phosphoric acid made via dilution of an 8.67 M stock solution (Sigma-Aldrich, W290017-1KG-K). The pH of the phosphoric acid solution was recorded as 1.03 ± 0.005. The solution was stirred at 200 RPM for an hour prior to use.

3. The cyclic etch of copper using formic acid occurred in two steps. Firstly, samples underwent oxidation in a Diener PICO Barrel Asher. Oxidation was done under a 0.3 mbar flow of oxygen at 100% power for 10 minutes. The oxidised samples were etched in formic acid (≥95%, Sigma-Aldrich, W248703-1KG-K) for 1 minute. Once etching was complete, the samples were rinsed with DI water and dried under nitrogen. Following this, all samples were immersed in IPA for thirty seconds, followed by three IPA rinse and nitrogen drying cycles.
4. Submersion in glacial acetic acid (Glacial, ReagentPlus®, ≥ 99%, Sigma-Aldrich, A6283-2.5L) up to 24 hr.
5. The cyclic etch of copper using acetic acid also occurred in two steps. The oxidation step for copper remained the same as that used in the formic acid etch. The oxidised samples were etched in acetic acid (Glacial, ReagentPlus®, ≥ 99%, Sigma-Aldrich, A6283-2.5L) for 10 minutes. Once etching was complete, the samples were dried under nitrogen. Following this, all samples were immersed in IPA for thirty seconds, followed by three IPA rinsing and nitrogen drying cycles.

2.4.2 Etch-anneal cycling on the Cu (50 nm)/Ta (7nm)/ Si (100) Samples

To test the effect of recovery annealing on the cyclical etch of copper in acetic acid, an anneal step was included before every etch step. Annealing occurred at 350 °C in a Carbolite tube furnace under 200 S.C.C.M of Argon for 1 hour and 30 minutes. Sample oxidation was done under a 0.3 mbar flow of oxygen at 100% power for 10 minutes in a Diener PICO Barrel Asher. The oxidised samples were submerged in acetic acid (Glacial, ReagentPlus®, ≥ 99%, Sigma-Aldrich, 1003545482) for 10 minutes. Once etching was complete, the samples were dried under nitrogen. Following this, all samples were immersed in IPA for thirty seconds, followed by three IPA rinsing and nitrogen drying cycles. Post etch, samples were annealed a final time at 350 °C in a Carbolite tube furnace under 200 S.C.C.M of Argon for 1 hour and 30 minutes.

2.4.3 Etch-anneal cycling the Cu (60 nm)/Al_2O_3 Samples

For comparison with the Cu (50 nm)/Ta (7nm)/ Si (100) sample, samples of Cu (60 nm)/Al_2O_3 were produced in-house. The sapphire substrates used in this study were

purchased from University Wafer. The single-side polished, C-Plane sapphire substrates are 250 μm thick and 50.8 mm in diameter. The 60 nm thick copper film samples were prepared using the Shamrock multi-chamber sputter and UHV evaporation system. Samples were deposited using RF Magnetron sputtering at a rate of 13.333 nm min^{-1} with a base pressure of $1x10^{-8}$ Torr. The samples were then moved, without breaking vacuum, into a second chamber with a base pressure of $1x10^{-9}$ Torr for a 2-hour anneal at 300 °C. To match the processing on the copper on silicon samples, the copper on sapphire samples experienced the same process for etching and annealing as given in ***subsection 2.4.2.***

2.4.4 Etch Characterisation of Cu (50 nm)/Ta (7nm)/ Si (100) Samples and Cu (60 nm)/Al_2O_3 Samples

The samples used to determine the etch rate were 2 cm^2 squares cut from the 12-inch wafer. These were coated with a thin layer of S1813 photoresist via spin coating at a rate of 5000 RPM. The samples were subsequently baked on a hotplate at 60 °C for five minutes. All samples were patterned using an OAI mask aligner. All copper samples were patterned with 10-micron dots that were spaced 10 microns apart by exposure to UV light for five seconds. The excess resist was then removed by immersion of the samples into MF319 for fifty seconds. Following this all samples were immersed in DI water for a further 30 seconds and dried using Nitrogen. The etching processes were completed as given in ***subsection 2.4.1.*** Upon completion, the photoresist pattern was removed using acetone (HPLC, ≥99.8 %, Sigma-Aldrich). This left samples of etched regions with a pattern of unetched dots as reference features.

Unlike the Cu (50 nm)/Ta (7nm)/ Si (100) samples, the Cu (60 nm)/Al_2O_3 samples did not contain a strong adhesion layer. As such, the etch rate was able to be determined by placing scratches through the copper layer post the processing of the sample. To determine the height difference between the etched and unetched features of Cu (50 nm)/Ta (7 nm)/ Si (100) or the etched copper and the sapphire substrate for Cu (60 nm)/Al_2O_3 samples, tapping mode AFM was used.

2.5 ETCH ROUGHNESS CHARACTERISATION

In the microelectronics industry, flat and smooth interconnect surfaces are desirable as they promote a minimum in resistivity and offer fewer defect sites for electromigration and stress voiding to occur. During processing, increases in roughness can be caused by methods such as annealing, etching, and sputter cleaning. AFM has previously been used

in the semiconductor industry for metrological purposes as well as for imaging fine electronic structures. The three-dimensional images provided by AFM allow for several methods of roughness characterisation to be implemented, three of which are discussed in detail below. For these studies all images were taken on the Asylum AFM using Budget Sensors Tap150Al-G tips. All images were 5 μm x 5μm in size with a resolution of 256 x 256 pixels to allow for direct comparisons between etches.

2.5.1 Classical Roughness Measurements

In order to define the effects such processes have on roughness, roughness must first be defined. A rough surface is defined as a surface with a non-zero variance in height with respect to its mean height. [100] It is clear, by this definition, no surface can be completely smooth; all surfaces will have some degree of roughness. In practical applications, the variation in a surface's height is not always considered down to the atomic scale. As a result, the qualification of a surface as either rough or smooth is subject to the constraints a user applies. For example, the instrument used to measure roughness can define the extent of a surface's roughness. In particular, an instrument offers two limits to roughness observation; vertical and lateral resolution. Vertical resolution determines the smallest difference in height a tool is capable of detecting. Meanwhile, the lateral or spatial resolution sets the smallest area an instrument is capable of measuring.

The most common measurement used to quantify a surface's roughness is known as the RMS roughness. RMS roughness is denoted by the symbol ω and is defined as;

$$\omega^2 = \int_{-\infty}^{+\infty} h^2 p(h) dh \qquad 2.37$$

Here, h is equal to the height and p(h) is the probability of a surface height between the value h and h+dh. The RMS roughness is equal to the standard deviation of heights (h) when the average height, $\bar{h}$, is set to zero. The RMS roughness of an AFM or STM image can be determined via the equation;

$$\langle \omega \rangle_N = \left\{ \frac{1}{N} \sum_{i=1}^{N} |h_i - \langle h \rangle_N|^2 \right\}^{\frac{1}{2}} \qquad 2.38$$

In ***Equation 2.38***, N is the number of pixels within the image, h_i is the height or z position of the i^{th} pixel of the image, and $\langle h \rangle_N$, is the average z position measured over the surface.

It is important to understand that RMS roughness is only capable of describing the statistical properties of random variables within a random field. The RMS is not capable of expressing the connection between variables at different positions. As an example, two surfaces are capable of having the same RMS roughness while objectively looking completely different. This occurs because the changes in height occur over different length scales. In order to differentiate the spatial differences between two surfaces, the relationship between the heights on the surfaces at two different positions must be quantified.

The most common method to quantify spatial roughness is via an auto-correlation function, R (r_1, r_2). For a homogenous and isotropically rough surface, the auto-correlation function can be written as;

$$R(r_1, r_2) = R(\rho) \tag{2.39}$$

The quantity, ρ, is known as the translation. It is also referred to as the lag or the slip. The translation represents the difference in length between one point (r_1) and another (r_2). In a true randomly rough surface, R(ρ) decays to zero as ρ increases. The rate of the decay is dependent on the distance over which two points become uncorrelated.

The autocorrelation length, ζ, in an autocorrelation function defines the value of the lag at which the autocorrelation function drops to 1/e of its value where R(ρ) becomes zero. As such

$$R(\zeta) = \frac{1}{e} \tag{2.40}$$

The autocorrelation length, ζ, is a representative lateral dimension of a rough surface. If the distance between two points being considered is within ζ, then the two points are considered correlated. Likewise, if the separation between the two points under consideration is larger than ζ, then the heights at the two points are independent of one another. For a randomly rough surface, the information provided by the autocorrelation function is a good representation of the surface's morphology. As a general rule of thumb, the shorter the autocorrelation function is, the rougher the surface appears.

2.5.2 The Fractal Dimension

The traditional roughness measurements outlined in the previous section are widely accepted and serve as valuable descriptors of surface roughness. However, this does not mean that these measures are without fault. The most glaring drawback of using such descriptors is that they vary depending on the size of the area under observation. This means

to compare two surfaces, they must be measured over the same area. Similarly, there is one value for vertical roughness and another for spatial variation; a refinement of these into a single parameter would allow for a more convenient method to compare surface roughness. One method by which we can do this is by using the fractal dimension.

The Euclidian dimensions of 0, 1, 2 and 3 allow us to define a point, a line, and a three-dimensional object, respectively. In reality, there are many objects that do not neatly fit into any of these categories.[101] For example, a dashed line or, perhaps more relevant to this discussion, a rough surface. Mandelbrot was able to account for such geometries through the use of intermediate dimensions. A broken line could be described as having a dimension between 0 and 1; likewise, a rough surface would have a dimension between that of a two-dimensional plane and a three-dimensional object. In these dimensions, Mandelbrot defined fractal objects. Fractal objects also include an infinite scaling of self-similarity[101], [102]. In this way, no matter what scale a fractal object is observed at, the fractal dimension remains the same. In practical applications, there is usually a limit to the size range over which the texture is self-similar; these fractals are referred to as self-affine.

There are several methods which can be used to determine the fractal dimension. Gwyddion's[103] fractal analysis software contains four methods by which a fractal dimension can be defined. These are the cube counting method[104], [105], the triangulation method[102], [105], the variance method[106], [107], [108], [109], [110], [111] and the power spectrum method[104], [105], [106], [107], [112]. Each of these methods uses different variables to determine the fractal dimension.

The cube counting method is an expansion of the popular box counting method[101], [107], [108]. In this algorithm, a cubic lattice with lattice constant, l, is applied to a z-expanded surface. Initially, l is set to X/2, where X is the edge length of the surface. This creates a 2x2x2 lattice or a lattice of 8 cubes. The number of cubes which contain surface pixels, N(l), are counted. The lattice constant is reduced by a factor of 2, and the counting process is repeated. The steps are repeated until l is equal to the distance between two adjacent pixels. A log-log plot of boxes versus 1/l gives a straight line whose slope is the fractal dimension D_{cc}. [103]

The triangulation method is also a derivation of the box-counting method. In this process, a grid of unit dimension, l, is applied to the surface. Each unit square uses the Z-height from the four corners in the unit square to form a set of two triangles inclined at

varying angles with respect to the XY plane. For example, when l is equal to X/2, the grid is comprised of 4 squares that make 8 triangles. The area of each triangle is determined and summed to approximate the surface area, S(l), which corresponds to that value of l. The box size is reduced by successive factors of 2, with the corresponding surface area measured at each step until the unit length is the distance between 2 adjacent pixels. A plot of S(l) versus log 1/l provides a linear graph whose slope corresponds to D_T -2. Here, D_T is the fractal dimension according to the triangulation method.[103]

The variance method is based on the scale dependence that variance has in fractional Brownian motion. Much like the triangulation method, the variation method starts by applying a grid of equally sized unit squares on the surface. The Z-heights encapsulated within each unit square are used to define the variance for each square. The variance is then averaged for every square within the grid. A log-log plot of variance versus grid size provides a linear graph with a slope, β. [103]The slope can be converted into a fractal dimension, D_v, by the equation[111]

$$D_v = 3 - {}^{\beta}/_{2} \qquad 2.41$$

The final method is the power spectrum method. The power spectrum method employs the fact that fractional Brownian motion has a power spectrum dependence to determine a fractal dimension, D_{ps}. To employ this technique, an AFM or STM image is broken up into line profiles. Each line profile is Fourier transformed to obtain a power spectrum. The power spectra are then averaged.[103] A log-log plot of the averaged power spectrum versus the frequency gives a straight-line plot of slope, β.[113] The slope can be converted into a fractal dimension via the equation

$$D_{ps} = {}^{7}/_{2} + {}^{\beta}/_{2} \qquad 2.42$$

In ideal circumstances, each of these methods would independently draw the same value of fractal dimension. In practice, this occurrence is rare. Many comparative studies reveal that the dimension estimators provide biased results. This can make surface interpretation difficult. This could be due to the nature of the data itself. AFM and STM images have a finite resolution, meanwhile, true fractals have an infinite resolution. This, combined with the differences in approaches could go some way to explaining the discrepancy. [113]

AFM and STM also have the drawback that the microscopic tip, which scans the surface, is not perfectly atomically sharp. This allows for a convolution between the surface and the tip. Measurements can also be distorted by tip orientation, tip-sample forces, thermal noise, and piezo-electric drift. Mannelquist et al. [106] studied the effects of tip geometry on fractal analysis in AFM using both the power spectrum method and the variance method. Comparison of the methods revealed the power spectrum method performed poorly compared to the variance method.

Arman et al.[104] has previously used the cube counting method to determine the fractal dimension of several copper thin films between 5 and 50 nm thick. The areas under study were 4.4 μm square images of 256 x 256-pixel resolution taken in contact mode. The fit of the linear regression for the cube-counting method was 0.992, indicating the cube-counting method was able to provide a strong linear regression for the data provided. All four fractal dimension analysis methods were applied to a variety of AFM images from all attempted etches. In all cases, the cube counting method provided the strongest performance with a Pearson correlation coefficient of 0.99. As such, the fractal dimension quoted in the forthcoming sections are taken from the cube counting method.

3 ETCHING PROCESS

The aim of this thesis is to fabricate nanoscale films solely comprised of CSBs. According to simulation, the depth of the CSB reconstruction ranges from a few nanometres up to 10 nm depending on the in-plane misorientation angle. The starting material for this project is a 50 nm film, as used by Zhang et al. [12] to induce the reconstruction originally seen in STM. The 50 nm copper film is deposited via PVD onto a 7 nm Ta adhesion layer resting on top of doped silicon. The Ta layer, much like a barrier layer in interconnects acts as a physical barrier stopping Cu from entering the Si.

In order to obtain a thickness of approximately 10 nm, the film needs to be thinned via a controlled etch. Etching processes can be subdivided into two types; wet chemical etching and dry chemical etching [114] In wet etching, unwanted material is removed from a surface by exposure to a strong acidic or alkaline solution[115]. Such processes have been in use since ancient Egypt to add designs onto jewellery [115]. As such, the use of wet etchants is well-established in the literature. Other benefits of such processes are; they are simple to implement, they do not necessarily require a cleaning step, and they are selective and relatively cheap [115]. However, this type of process is generally isotropic, making it a poor choice for the preparation of microelectronic components [115].

In terms of the production of copper interconnects excess copper can be removed via a hybrid wet etch-mechanical abrasion process known as chemical mechanical planarization (CMP) [21]. CMP removes copper using a combination of dissolution, passivation, and abrasion [116]. In this process, wafers are placed face-down onto a rotating pad on which a slurry is dispensed [117] The slurry contains different agents, including an oxidiser, a complexing agent, a corrosion inhibitor, and abrasive particulates. In terms of wet chemical processes, the oxidiser forms porous, unstable surface oxides, which the complexing agent then dissolves by creating a water-soluble complex [117]. A corrosion inhibitor is added as a counterbalance to the etch process. The inhibitor forms an insoluble, stable complex with the surface, which prevents copper corrosion [116]. In parallel, mechanical material removal is accomplished with abrasive particulates.

Another wet chemical etch process typically employed in ULSI applications is electropolishing. Electropolishing is the process in which the topography of a conductive surface can be planarized by polarising a surface anodically [118]. Anodic polarisation

causes electrons to move from a metal surface, acting as an anode, to a cathode. This leaves behind an oxidised metal surface. The oxidised metal complexes with ions in the electrolyte. This complex is water soluble, allowing it to be removed from the surface. Electropolishing differs from electrochemical etching in that the rate of etching is mass transport limited as opposed to reaction rate limited. In the transport-limited conditions, a viscous electrolyte layer[119] builds up at the surface. As a result, protrusions from the average surface height, which extends further into the layer, are able to etch faster, creating a smoother surface.

The second category of etching, referred to as dry etching or plasma-assisted etching, involves the removal of material via exposure to a plasma, which carries out etching in the gas phase as opposed to the liquid phase. This process is anisotropic, allowing for higher resolution for etch features, which is desirable for microelectronics. Dry etching also utilises mechanical etching as well as chemical etching to achieve its aim. For example, in a reactive ion etch (RIE) process, copper is exposed to a halogen plasma. The halogen ions can be directed towards the surface allowing for sputter removal of material. Simultaneously, the halogen ions can react with the oxide on the surface to form etch products that can be desorbed from the surface. Most of these reaction products have low volatility, so heating samples to a high temperature allows for desorption. Alternatively, the etch products can also be removed by using a secondary hydrogen plasma or by laser-induced desorption.

To determine the etch rate, 50 nm copper films were patterned using S1813 photoresist. The pattern created is a series of 10 µm wide circular islands spaced 10 µm apart. The islands are protected during the etching process. An example of a surface with this pattern is shown in ***Figure 3.1***. The samples are etched in accordance with the details in ***subsection 2.4.1***. Post etching, the resist is removed from the protected features. AFM is used to measure the height difference between the etched and

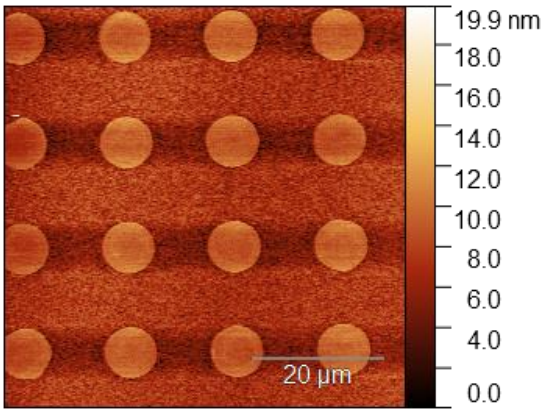

Figure 3.1: 60 µm x 60 µm AFM image of the patterned copper surface. Circles on sample are sections of copper that were protected by S1813 photoresist during etching. Sample was etched in citric acid for 30 minutes.

unetched features to determine the thickness of material removed by the etch at various time stamps.

3.1 CITRIC ACID

One of the most common organic acids that has been utilised as a complexing agent in the CMP of copper is citric acid [116], [117], [120], [121], [122], [123]. Depending on the composition of the CMP slurry, the rate of removal by citric acid can be anywhere from 0 nm min^{-1} to > 100 nm min^{-1}[116], [117], [120], [121], [122], [124]. In particular, citric acid without any oxidising agent has an etch rate between 0 and ~ 2 nm min^{-1}[116], [117], [122]. As such, a good starting point for a citric acid etch is submerging copper in aqueous citric acid. In aqueous solutions with dissolved oxygen, oxides are capable of forming on the copper surface [125].

$$Cu + H_2O \rightarrow CuO + H_2 \quad 3.1$$

$$2Cu + H_2O \rightarrow Cu_2O + H_2 \quad 3.2$$

$$Cu + 2H_2O \rightarrow Cu(OH)_2 + H_2 \quad 3.3$$

In solutions at pH of 1.45, the stable forms of citric acid are H_3X and H_2X^-, where X = $^-OOCH_2OHCOO^-CH_2COO^-$[126], [127]. The H_2X^- anions likely adsorb onto oxide sites compared to copper metallic sites. The adsorbed anions allow for water-soluble complexes to form. The dissolution efficiency of citric acid on copper oxides was tested by Ko and Lee[123]. In their study, Cu_2O and CuO were able to be dissolved in citric acid solutions at low pH values. As the pH decreased, the concentration of dissolved oxides increased. At every stage, Cu_2O was more soluble than CuO. At a pH of 2, Cu_2O was 20 times more soluble than CuO.

Table 3.1: Etch depth and instantaneous etch rates for citric acid etch development

Time Elapsed (h)	Mean Unetched Peak Position (nm)	Mean Etched Peak Position (nm)	Height Difference (nm)	Etch Rate (nm h^{-1})
0.5	10.8	6.7	4.1 ± 0.3	8.2 ± 0.6
1.0	22	15	7.3 ± 0.4	7.3 ± 0.4
1.5	34	20	14 ± 2	9 ± 1
2.0	53	32	21 ± 1	10.5 ± 0.7

The etching data for the citric acid is shown in ***Table 3.1***. Aqueous citric acid is capable of efficiently etching copper oxide without the addition of a specific oxidising agent. The average etch rate for citric acid was determined to be 8.2 ± 0.7 nm h^{-1} from a least squares linear regression. The fit line can be seen in ***Figure 3.2***. A potential source of the etch rate variation could be a result of the etchants interaction with the sample's topography. Using citric acid to etch the sample produced a surface which contained a series of pit features. These features could be an extension of the pinhole features images on the unetched surface. It is known that different crystal faces of copper oxidise at different rates. Within the pinhole defects, crystal planes could be present which oxidise much more readily than the (111) surface. This could allow for the pinholes to act as faster etching fronts. Alternatively, the misorientation angles and differing structures of the grain boundaries and grain boundary triple points could also provide preferential oxidation sites, which, in turn, allow for preferential etching. Imaging the surface during an active etch may allow for the origin of the pit features to be discovered, but such work is out of the scope of this project.

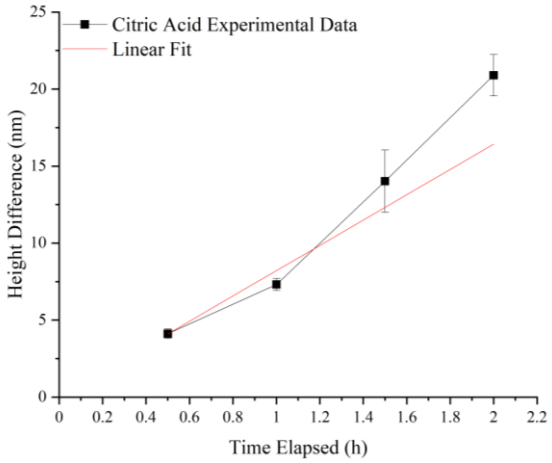

Figure 3.2: Scatter plot of height difference between etched and unetched sample sections versus time elapsed for citric acid. The red line is a linear regression used to determine the average etch rate of citric acid.

3.2 PHOSPHORIC ACID

Phosphoric acid is one of the most studied electrolytes for the electropolishing of both copper and other metals [99], [118], [128], [129], [130]. Depending on the exact specification of the etch solution (electrolyte), the rate of material removal in electropolishing can vary between ~ 4 nm s^{-1} to ~ 25 nm s^{-1} [131], [132]. In the general electrochemical reaction scheme, the anodic potential oxidises metallic copper at the surface into cupric cations. These cations react with phosphate anions dissolved in the etch solution to form a $(Cu\text{-}H_2PO_4)^+$ complex [133]. From literature, there is universal agreement that electropolishing occurs when the reaction is controlled by mass transfer. This condition is found at a well-defined potential range where the limiting current density is a plateau in the polarisation curve [118]. The polarization behaviour of a 4 cm^2 sample in a 0.43 M aqueous phosphoric acid solution at room temperature is shown as ***Figure 3.3***.

Three regimes have been seen for the removal of copper. This is in agreement with the results found in previous studies [118]. In the initial stages, the current rises steeply with increasing potential. In this region, the sample is etched preferentially at crystallographic sites or planes that have higher surface energies. As a result, the etching process results in a dull surface where roughness is not minimised[118]. A similar bias dependence is seen beyond ~1100 mV. Here, the current rises rapidly with applied potential due to oxygen evolution at the anode surface.

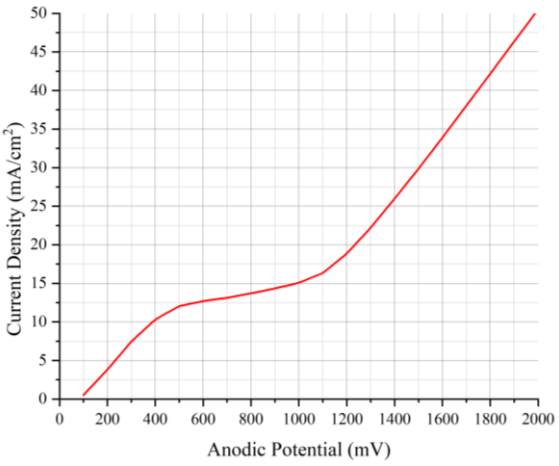

Figure 3.3: Line plot of current density versus anodic potential expressing the polarisation behaviour of 4 cm^2 square of copper thin film in 0.43 M phosphoric acid at 25 °C

Between 0.5 V and 1.1 V, the current density nearly plateaus to a constant level. The current density plateau in electrochemical planarization is the result of the dissolution of copper being controlled by mass transfer via a surface boundary layer. In this region, high points of the surface extend out into the layer, allowing them to be preferentially oxidised, creating a smoother surface. An exact mechanism for copper electropolishing is not available due to the complicated dissolution process at the interface between the electrolyte and the anode [130]. The two theories that have gained prominence are the salt film model[129], [134], [135] and the water acceptor model[118], [128], [136], [137]. Though, in recent years, the water acceptor mechanism has more supporting evidence. In this mechanism, the electrical current oxidises copper into its +2 state. From here, an acceptor phosphate ion diffuses to the anode surface and enhances removal of the copper ion due to its favourable thermodynamic driving force. Once the $(Cu\text{-}H_2PO_4)^+$ is formed it can be solvated with six molecules and can diffuse from the surface. The six molecules can be a mix of either H_2O or $H_2PO_4^-$.

In ***Figure 3.3***, the current density does not completely plateau, suggesting the process may not be entirely transport-limited. This may be the result of the low concentration of phosphoric acid in the etching solution. The bias independence requires a $(Cu\text{-}H_2PO_4)^+$ viscous barrier to form at the surface. If there is insufficient $H_2PO_4^-$ to saturate

the surface there may be a voltage dependence on the rate of polishing. This is supported by Chang et al. [131] who noted a decrease in etch rate when the concentration of phosphoric acid decreased from 85% to 50%.

Since the phosphoric acid etch did not provide a complete plateau, the etching process was potential controlled rather than current controlled. To select the etch conditions which provided the smoothest surface, etching was conducted for 2 seconds at voltages between 0.4 V and 1.5 V. The roughness of the resulting surfaces are provided in ***Figure 3.4***. A comprehensive explanation of each roughness metric will be given in ***Chapter 4.*** Both the root mean square (RMS) and Autocorrelation length (ACL) roughness values have standard deviations large enough to make a conclusive determination of the sample with the smoothest finish impossible. The final measurement provided is the fractal dimension (***Figure 3.4 (c)***). The fractal dimension measures surface roughness as being between a perfect plane (Fractal dimension of 2) and a perfect three-dimensional object (Fractal dimension of 3). From the fractal dimension, the sample with the lowest surface roughness is the sample etched at 1.0 V.

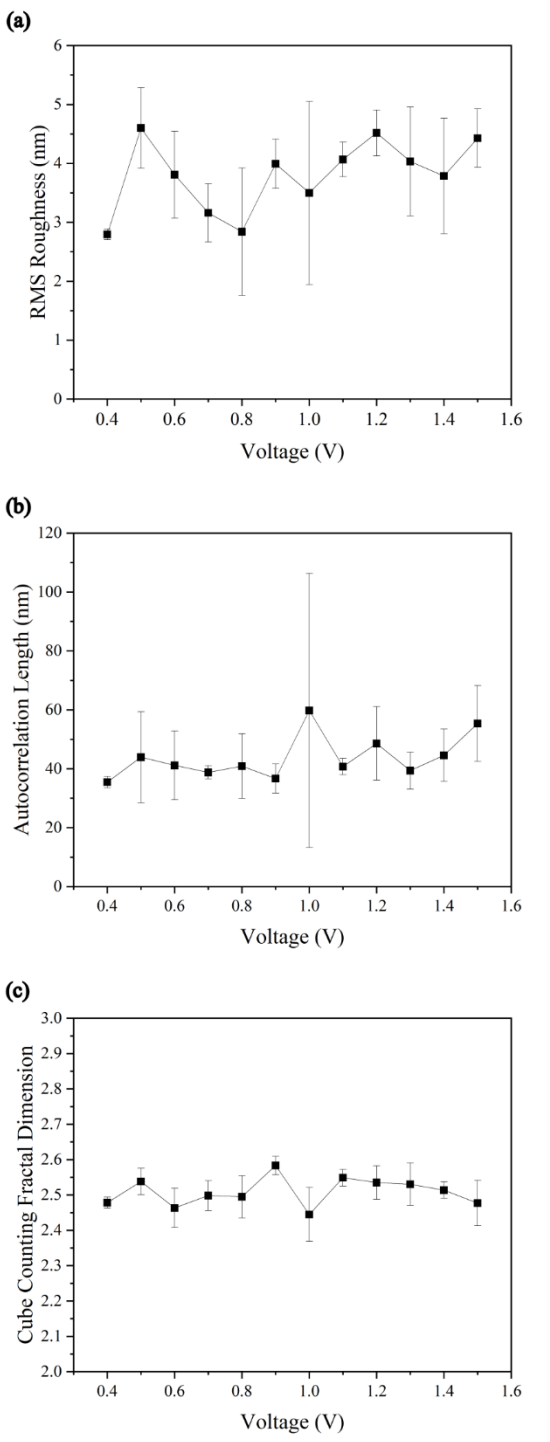

Figure 3.4: Scatter plot of roughness measurements at various etching voltages. (a) root mean square roughness vs etching voltage, (b) autocorrelation length vs etching voltage and (c) cube counting fractal dimension vs etching voltage.

Example line profiles for the surfaces after 2 seconds are given in ***Figure 3.5***. 0.4 V sits within the first region of the I-V curve (***Figure 3.3***), where preferential etching

occurs. The near plateau feature exists between 0.5 V and 1.1 V. From 1.1 V onwards, current density begins to increase, indicating oxygen generation is occurring. Of note in ***Figure 3.5*** is the 1.0 V surface, which provided a relatively smooth surface which was interspersed with pits. The presence of pits is proof the etch is acting somewhat preferentially as opposed to a polishing. The 1.0V samples also have regions that are exceptionally smooth, indicating that some degree of polishing was accomplished in the initial stages of the etch.

As can be seen from ***Table 3.2***, etching using these parameters occurs in a matter of seconds. To make etching reproducible, a Keithley 2450 source meter is employed. The Keithley 2450 source meter allows for the application of a set bias or current for a defined amount of time. The Keithley 2450 can take 59 measurements over a second, making it an appropriate method for performing etches in the regime of seconds [138].

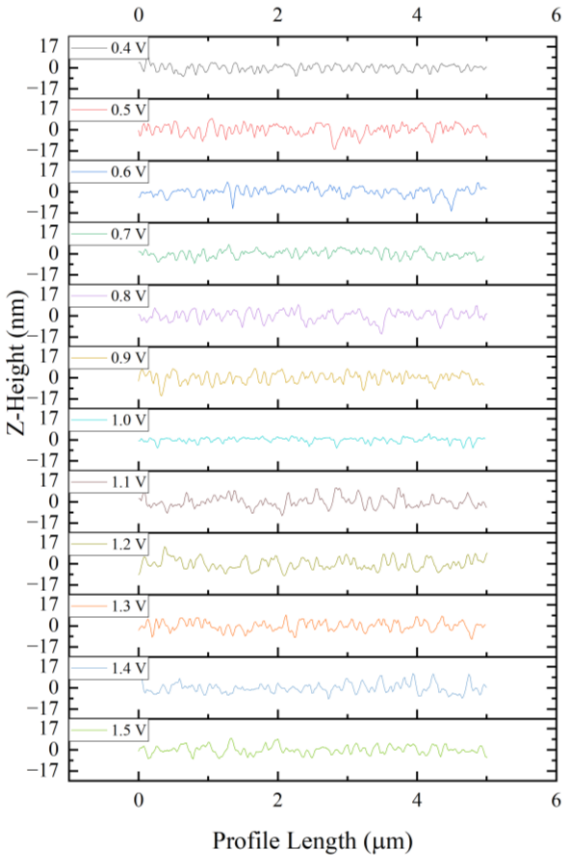

Figure 3.5: Line profiles extracted from AFM images of electrochemically etched samples. The samples were etched for 2 seconds in a 0.43 M phosphoric acid solution at varying voltages, starting at 0.4 V (Top) to 1.5 V (Bottom).

Table 3.2: Etch depth and instantaneous etch rates for phosphoric acid etch development.

Time Elapsed (s)	Mean Unetched Peak Position (nm)	Mean Etched Peak Position (nm)	Height Difference (nm)	Etch Rate (nm s^{-1})
1	102	96	7 ± 1	7 ± 1
2	180	170	9 ± 3	5 ± 1
3	232	221	11 ± 3	4 ± 1
4	196	181	15 ± 8	4 ± 2
5	307	282	26 ± 3	5.1 ± 0.7
10	773	745	29 ± 23	3 ± 2
15	1724	1655	69 ± 14	4.6 ± 0.9

The average etch rate for the phosphoric acid was determined by a least squares linear regression to be 4.8 ± 0.4 nm s^{-1} (***Figure 3.6***). Compared to the citric acid etch, the electrochemical etch is much faster. However, such small-time scales lead to difficulty when determining the exact times that will produce a sample of desired thickness compared to citric acid. In ***Table 3.1***, the variation in the thickness of material removed increases as the etch develops. This is particularly evident in the 10 second and 15 second etch samples, which had some regions where the etch could not develop due to the crocodile clip covering the surface and other regions where the full thickness of the material was removed. The variation in the etch rate can also be seen visually in ***Figure 3.7***.

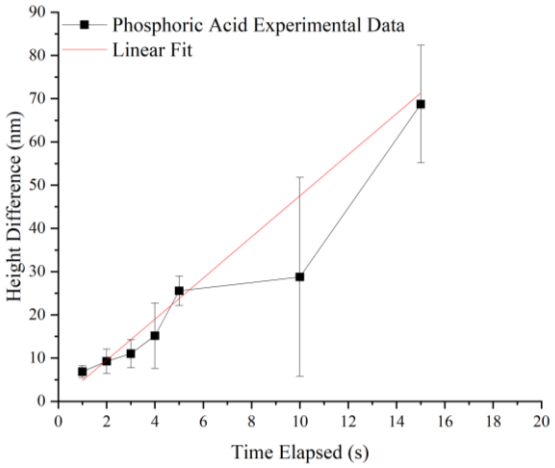

Figure 3.6: Scatter plot of height difference between etched and unetched sample sections versus time elapsed for phosphoric acid. The red line is a linear regression used to determine the average etch rate of phosphoric acid.

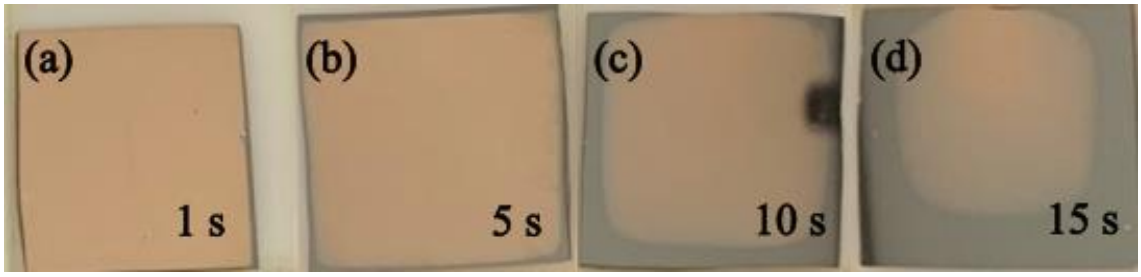

Figure 3.7: 2 cm square samples of 50 nm copper films deposited onto a 7 nm tantalum adhesion layer which is deposited onto p-doped silicon. Each sample has been exposed to the 0.43M phosphoric acid etch solution at 1.0 V for a time, t. (a)t =1 s, (b)t =5 s, (c)t =10 s and (d) t=15 s

The difference in etch rate between the centre of the sample and the edge of the sample could be due to the geometry of the sample. The samples are square. The presence of sharp edges and corners provide locations where the electric field is strengthened. These regions could preferentially oxidise copper into its +2 state. This would lead to increased reactions with phosphoric acid making the etch rate increase [139]. A second source for variation within the etch was considered. In these experiments, etching is completed in a 250 mL beaker, which contains two electrodes. Positioned in the centre of the beaker is a copper crocodile clip holding the 2 cm square sample, making the anode. Surrounding the anode is a cylindrical mesh of copper, which functions as the cathode. The cathode is attached to the power supply via another copper crocodile clip. From this geometry, it is noted that two of the sample's edges are closer to the cathode mesh than the centre of the sample. Since the bottom edge of the sample etches in a similar way to the edges closer to the cathode, it is unlikely that the variation in interelectrode distance is responsible for the etch rate variation.

3.3 FORMIC ACID

As has been seen in many CMP studies, copper can be etched by organic acids. Another example of such an acid is formic acid (CH_2O_2) [140]. Organic acid anions make up 0.1 to 1% of the total ion concentration in corrosion products for copper exposed in outdoor atmospheres over extended periods. Formic acid has also been detected in rainwater and has been linked to the early corrosion failure of copper tubes used in air conditioning or heat exchange systems [141]. Formic acid is not as easily ionised as citric or phosphoric acid. As a result, formic acid is expected to be less corrosive compared to the previously used acids[142].

Sheil et al. [143] used formic acid as a method to dissolve copper oxide in a cyclical etch process. In this process, an oxygen plasma was used to control the depth of the copper

oxide, while a formic acid vapour was used to selectively remove the copper oxide from the metallic copper. Such an etch process can allow for a step-by-step removal of copper, providing a thickness control that is desirable for this project.

The oxidation of Cu (100) and Cu (111) surfaces in a low-pressure oxygen plasma was studied by Kunze et al. [144]. The chemical composition of the oxide layer was studied by STM – XPS and NEXAFS. Both single-crystal films developed a sandwich-like film structure with CuO at the surface and Cu_2O at the interface between the metallic surface and the CuO. In both cases, the oxides aligned to the Cu (111) surface. Similar structures have also been seen to develop during the thermal oxidation of copper but at a much slower rate[145].

Sheil et al. [143] confirmed the etch selectivity of formic acid for Cu and Cu oxide thin films by submersing both films in a liquid-phase formic acid solution. The copper oxide thin films were produced by thermal oxidation of a 70 nm copper film at 150 °C for 1 hr. The etch results showed the CuO_x film etched over 10 s, providing an etch rate of 520 nm/min, versus the Cu film, which was etched for over 600 s to provide an etch rate of 1.7 nm/min. The etch mechanism of the oxide is suspected to be an acid-base reaction between the formic acid and the copper oxide. This reaction results in the formation of water and Cu (II)-formato complexes.

In our study, a patterned polycrystalline copper thin film was exposed to a 0.3 mbar oxygen plasma at 100% power for 10 minutes to create an oxide layer on the copper surface. The oxide was then exposed to formic acid for 1 minute. After exposure to the etchant, the copper was cleaned by rinsing it in DI water and dried with a nitrogen purge. This process was repeated in increments of two before removing the S1813 photoresist. The etch depth per round was determined via AFM. The process was repeated for up to 12 rounds of etching. The results of the stepwise etch process are shown in ***Table 3.3***. Up to the 10th round of etching, the etch rate

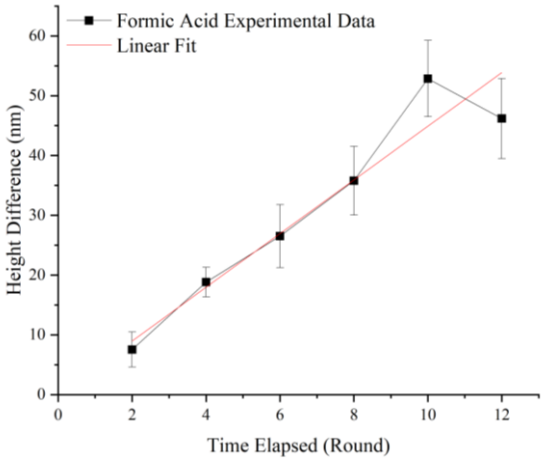

Figure 3.8: Scatter plot of height difference between etched and unetched sample sections versus time elapsed for formic acid. The red line is a linear regression used to determine the average etch rate of formic acid.

between the samples remains the same within the limits of experimental error. The low value seen at the 12th round may be the result of an insufficient thickness of copper remaining. If there is not enough copper remaining for an oxide of the same thickness seen in the first set of rounds to form, the etch rate decreases. As seen in the previous analyses, the average etch rate for the overall process was determined via a least squares linear regression of the etch depth data, as seen in ***Figure 3.8.*** The value obtained for the formic acid etch was 4.5 ± 0.2 nm per round

Table 3.3: Etch depth and instantaneous etch rates for formic acid etch development

Time Elapsed (Round)	Mean Unetched Peak Position (nm)	Mean Etched Peak Position (nm)	Height Difference (nm)	Etch Rate (nm Round^{-1})
2	377	369	8 ± 3	4 ± 2
4	57	38	19 ± 3	4.7 ± 0.6
6	65	38	27 ± 5	4.4 ± 0.9
8	125	89	36 ± 6	4.5 ± 0.7
10	511	458	53 ± 6	5.3 ± 0.6
12	108	62	46 ± 7	3.9 ± 0.6

3.4 ACETIC ACID

3.4.1 Without a Controlled Oxidation Step

Copper has three different oxidation states; $Cu^{(0)}$ or metallic copper, $Cu^{(1)}$ known as cuprous oxide and $Cu^{(2)}$ also known as cupric oxide [146] Upon exposure to air, copper readily forms a film of cuprous oxide, cupric oxide, cupric hydroxide, chemisorbed water, and carboxylate species [146]. Chavez and Hess utilised acetic acid to remove the copper oxide layer while metallic copper beneath remained intact. Acetic acid is able to react with copper oxides to form cupric acetate[146] via the reaction.

$$CuO + 2CH_3COOH \rightarrow Cu(CH_3COO)_2 + H_2O \quad 3.4$$

$$Cu_2O + 4CH_3COOH \rightarrow 2Cu(CH_3COO)_2 + H_2O + H_2 \quad 3.5$$

Acetic acid also has the benefit of a low surface tension, which allows residual acetic acid to be removed without using a water rinse[146]. In their study, Chavez and Hess showed that the oxide layer of copper could be near fully removed after 5 seconds of exposure to acetic acid. Submersion of the samples to extended periods up to 10 minutes within the

acetic acid showed no adverse effect on the copper-to-silicon ratio. Likewise, XPS analysis of the nitrogen-dried samples did not detect the presence of acetic acid on the surface. However, preliminary AFM analysis on these samples did reveal a slight roughening of the surface due to exposure to acetic acid.

Zhang et al. [12] utilised acetic acid to remove copper oxide from the Cu 50 nm nanocrystalline film prior to introducing the sample into UHV. The sample was submerged for 30 seconds and immediately transferred to the load lock, which was at a Nitrogen overpressure. After cleaning anneals on the surface, Zhang et al. [12] managed to achieve a film with a roughness of 0.5 nm over a μm scale. To begin this work, copper samples were immersed in pure glacial acetic acid for times ranging between 8 and 24 hours. The aim of this process was to ensure that acetic acid would only consume the oxide layer of the film, and a controlled oxidation step could be included to initiate and control the rate at which the copper was removed from the surface. In theory, the samples should lose their initial oxide layer and remain unchanged after this.

If only the topmost oxide layer is removed, the height difference between the etch and unetched features should remain the same at all time points. This did not occur; instead, the copper samples showed a wide variety of etch rates that could not be reproduced between runs. The source of the slow etching with large variation is a result of the ambient environment in which the etch is undertaken. When in contact with the outside atmosphere for extended periods of time, non-oxidising acids are capable of becoming more corrosive. This is a result of oxygen in the air dissolving into the etchant[142]. Likewise, the acetic acid used, though glacial, is used over several months and is subjected to atmosphere the moment it is opened. This would also contribute to the amount of atmospheric oxygen dissolved into the acid.

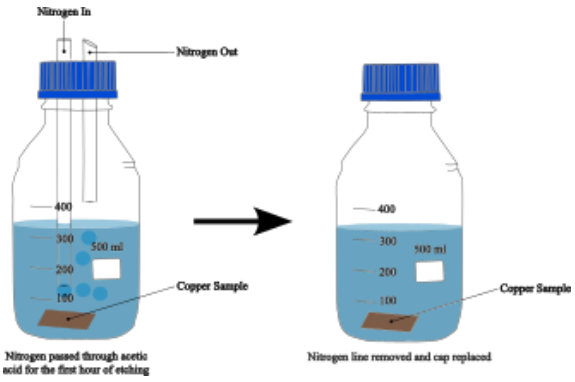

Figure 3.9: Schematic of acetic acid etch purge and sealing process. Prior to introducing the sample, nitrogen was passed through the acetic acid for an hour. Nitrogen continued to bubble through the etch solution for the first hour of etching. After this the cap of the etching vessel is replaced by a screw cap lid.

To confirm this, a second set of submerged samples were completed. In these etches the acetic acid was purged under a nitrogen flow to try and minimise the effect of dissolved

oxygen. Here, nitrogen was passed through the acetic acid for an hour prior to etching and for the first hour after the sample had been added to the solution. After this point, the vessel was sealed for the remaining etch time. A schematic for the etch process is given in ***Figure 3.9***. The etch results for acetic acid under a nitrogen flow are shown in ***Table 3.4***. The average etch rate of the nitrogen purged samples was determined using a least squares linear regression of thickness removed (Height difference) versus time elapsed. The average etch rate is 0.94 ± 0.04 nm h^{-1}. The regression can be seen in ***Figure 3.10.*** The fitting process for the linear trendline has the intercept set to 0 since at t= 0 h, there should be no etching of the surface. As a result of this choice, the linear trendline does not pass through the first data point at 8 h.

Table 3.4: Etch depth and instantons etch rates for acetic acid etch development under Nitrogen.

Time Elapsed (h)	Mean Unetched Peak Position (nm)	Mean Etched Peak Position (nm)	Height Difference (nm)	Etch Rate (nm h^{-1})
8	29	19	10 ± 3	1.3 ± 0.3
16.5	39	21	18 ± 2	1.1 ± 0.1
23	42	20	22 ± 1	0.94 ± 0.06

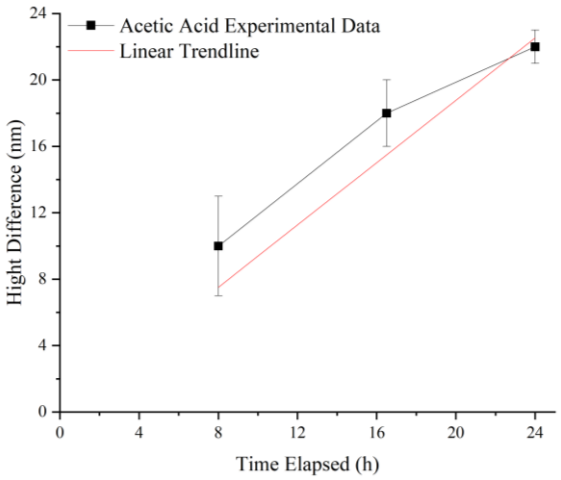

Figure 3.10: Scatter plot of height difference between etched and unetched sample sections versus time elapsed (h) for acetic acid. The red line is a linear regression used to determine the average etch rate of acetic acid.

Unlike the report by Chavez and Hess, extended exposures of copper to acetic acid are capable of etching copper without the addition of a specific oxidising agent, albeit incredibly slowly. Schaefer et al. [142] reinforces that copper is resistant to acetic acid provided no route of oxidation exists. However, laboratory experiments on copper found the etch rate of copper in 50% aqueous acetic acid under a nitrogen flow was 0.46 nm h^{-1}. Meanwhile, in the presence of an oxygen atmosphere, the same 50% acetic acid was quoted as having an etch rate ranging from 2.28 to 28.5 nm h^{-1}. Though not directly comparable to the etching process of glacial acetic acid. The experiment from Schafer does show that the presence of oxygen in the environment can allow acetic acid to etch copper over extended

periods of time. As such, introducing a controlled oxidation step to this etch could improve acetic acid's etching rate and reproducibility.

3.4.2 With a Controlled Oxidation Step

Many studies on copper corrosion have compared the effects of formic acid corrosion with acetic acid corrosion. In these studies, the severity of corrosion increases as the number of atoms in the alkyl chain decreases. [140] Since acetic acid has two carbons as opposed to formic acid, which has one, acetic acid should not etch as severely as formic acid. However, in Chavez and Hess' analysis[146], acetic acid was capable of removing copper oxides within five seconds of exposure. As a comparison, the formic acid etch process steps were repeated, this time using glacial acetic acid as the etchant. The results of the etch development are shown in ***Table 3.5*** and ***Figure 3.11***. The average etch rate for this set was determined to be 3.4 ± 0.1 nm per round by linear regression of the etch depth versus round number plot. In this process, the height difference between etched and unetched features is much smaller per round for acetic acid etch than formic acid etch. The etch depth difference at the sixth round provides a clear comparison between the two. In formic acid, the etch has removed 27 ± 5 nm worth of material as opposed to acetic acid, which has removed 19 ± 7 nm.

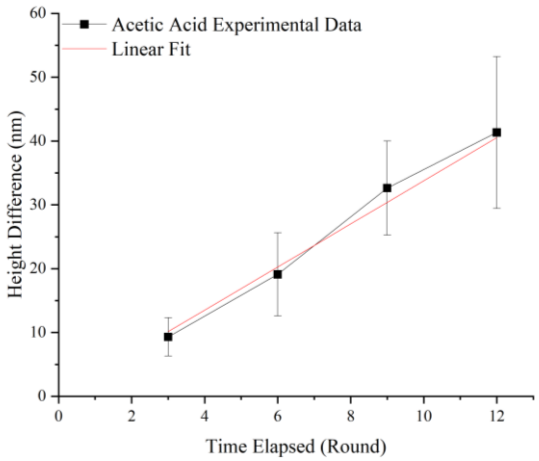

Figure 3.11: Figure 3.12: Scatter plot of height difference between etched and unetched sample sections versus time elapsed (Round) for acetic acid. The red line is a linear regression used to determine the average etch rate of acetic acid.

Both etch sets consist of samples from the same parent wafer and undergo the same oxidation step. If the thickness of the oxide layer was the controlling factor for the etch rate, both etchants should have the same rate. This, however, does not appear to be the case; rather, acetic acid seems to etch a smaller thickness of oxide. In Kunze et al. [144] both Cu (100) and Cu (111) formed a Cu_2O layer, which seemed to hit a peak between 0.66 nm for Cu (111) and 1.3 to 1.7 nm for Cu (100). The difference in material removed per round between formic acid and acetic acid is 1.1 ± 0.3 nm. Given the potential for the plasma-formed Cu_2O layer in polycrystalline samples to be in a similar thickness range. Such a difference in etch rate may be the result of formic acid being able to etch Cu_2O, while acetic acid is not. This is supported by the presence of Cu_2O on the surface of copper post 5 second

acetic acid etch was acknowledged by Chavez & Hess[146] during their ARXPS of the copper sample post etching.

Table 3.5: Etch depth and instantons etch rates for acetic acid etch development

Time Elapsed (Round)	Mean Unetched Peak Position (nm)	Mean Etched Peak Position (nm)	Height Difference (nm)	Etch Rate (nm Round^{-1})
3	23	14	9 ± 3	3 ± 1
6	45	26	19 ± 7	3 ± 1
9	59	27	33 ± 7	3.6 ± 0.8
12	67	25	41 ± 12	4 ± 1

4 ETCH ROUGHNESS

A well-defined etch rate is not the only parameter considered for the creation of nanoscale films. In microelectronics, smooth interconnect surfaces are required as they minimise surface-related effects such as resistivity increases with the size effect, electromigration and stress voiding. In Zhang et al. [12] original study, imaging of the reconstructed boundaries was possible due to the low roughness of the sample. The root mean square (RMS) roughness of the sample is quoted as 0.5 nm over a micron scale. AFM has previously been used in industry for metrological purposes as well as for imaging fine electronic structures. Images provided by AFM allow for several methods of roughness characterisation to be implemented. For the following analysis all images were taken on the Asylum AFM using Budget Sensors Tap150Al-G tips. All images were 5 µm x 5µm in size with a resolution of 256 x 256 pixels to allow for direct comparisons between etch morphology.

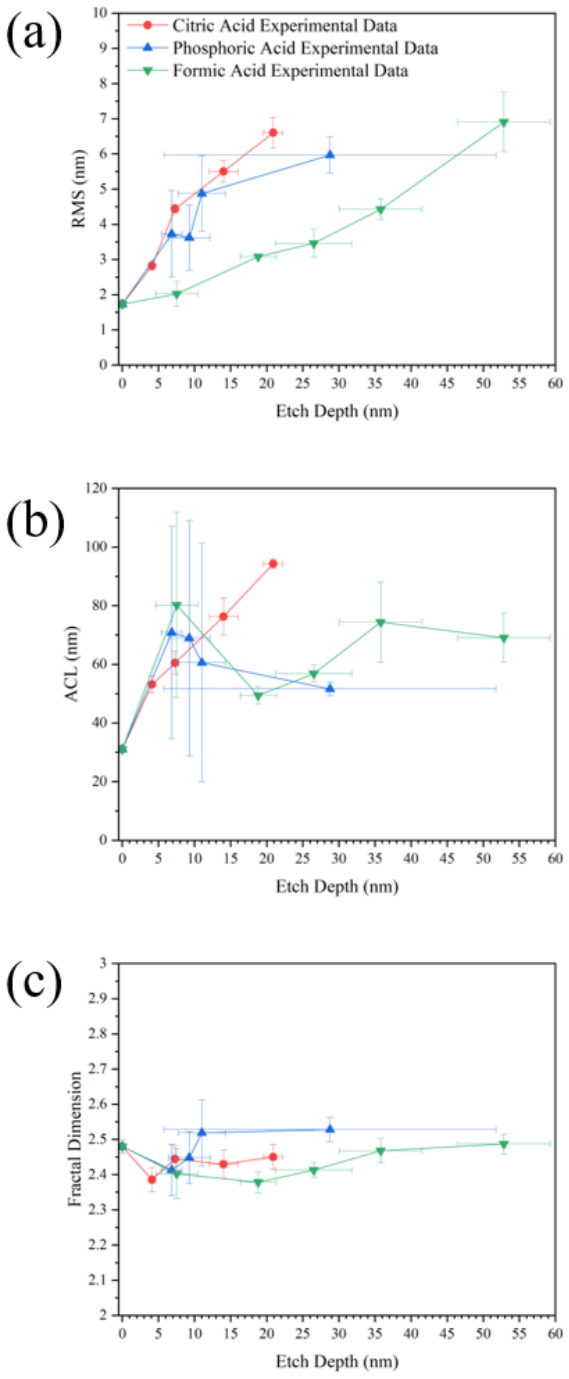

Figure 4.1: Scatter plots of roughness descriptors for sample surfaces versus the thickness of film removed. All three plots compare citric acid (Red), phosphoric acid (Blue) and formic acid (Green). (a) Root mean square roughness vs etch depth, (b) Auto correlation length vs etch depth and (c) cube counting fractal dimension vs etch depth.

4.1 COMPARISON OF DIFFERENT ETCH METHODS

The results of traditional roughness analysis and fractal dimension analysis as a function of the thickness of film removed for submersion in citric acid, electropolishing in phosphoric acid and oxidation-etching in formic acid are shown in ***Figure 4.1.*** The roughness values given for the unetched surface are the same for all samples. These values were determined using a sample taken from the parent wafer, which had not been processed in any way. The first value under consideration is the root mean square (RMS) roughness. The RMS roughness measures the deviation of heights around the average height of the sample. All three etches cause an increase in the RMS roughness as the film is thinned. Citric acid provides the largest rate of increase in RMS roughness, with an RMS of 6.6 ± 0.4 nm achieved when 21 ± 1 nm of the film was removed. Phosphoric acid provides a slightly smaller rate with an RMS roughness of 6.0 ± 0.5 nm achieved when 29 ± 23 nm of the film was removed. The two-step etch using formic acid provides the lowest rate of increase for the RMS roughness. As can be seen in ***Figure 4.1(a),*** formic acid gained an RMS of 6.9 ± 0.8 nm when 53 ± 6 nm of the film was removed.

Figure 4.1 (b) plots the autocorrelation length (ACL) measured on the samples as a function of the depth of material removed. The ACL represents the distance at which two points can be considered correlated. The larger this value is, the smoother the surface appears. For the citric acid etch, the ACL increases linearly with thickness of material removed. The increasing ACL indicates that the surface is becoming smoother in the lateral dimension. In conjunction, the peaks and valleys of the surface are increasing according to the RMS analysis. Combining these results together, particular features on the surface appear to etch quicker than the remainder of the surface creating a surface which appears laterally smoother but has a high degree of thickness variation.

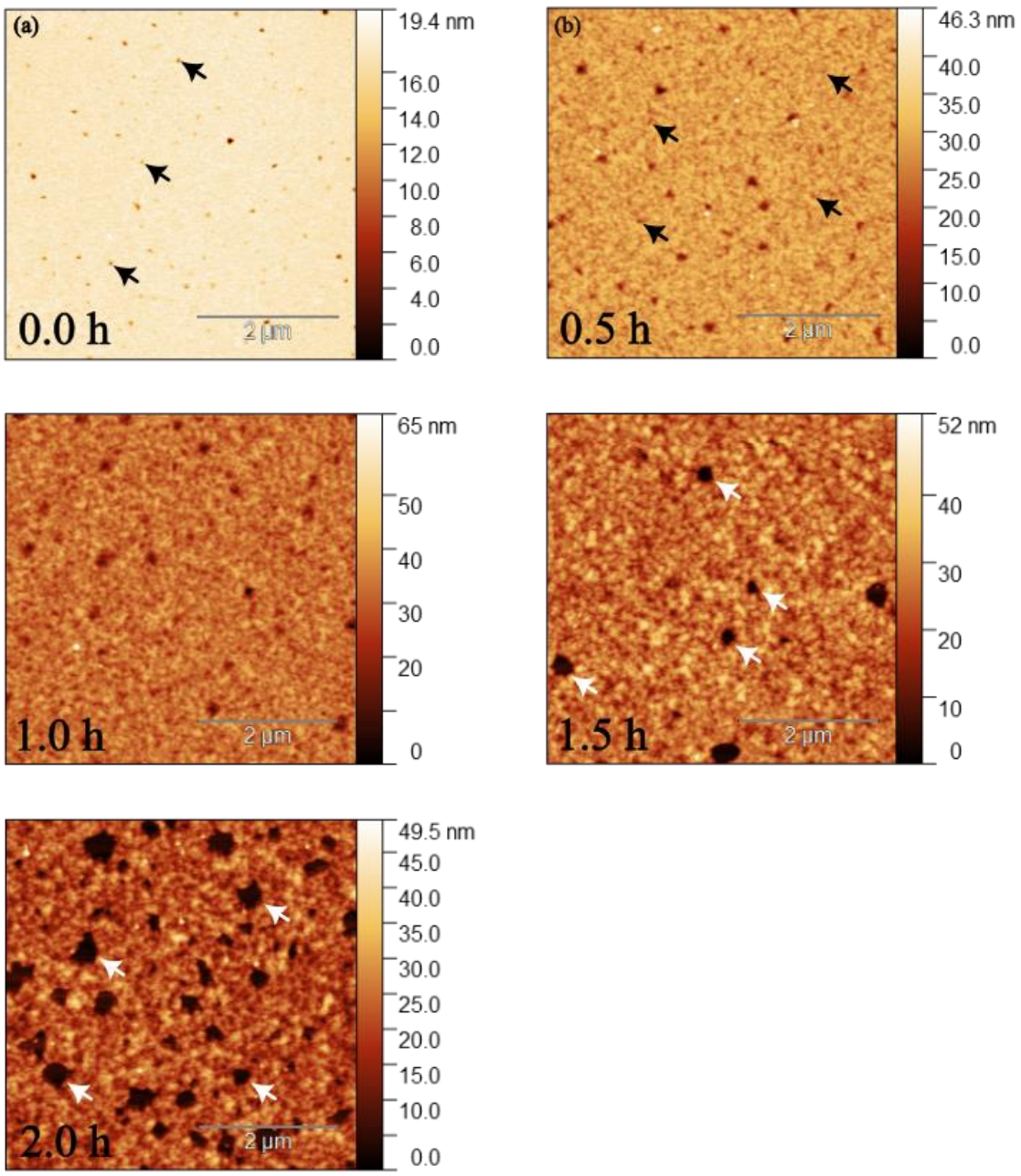

Figure 4.2: 5 µm AFM images at (a) 0 hr, (b) 0.5 hr, (c)1.0 hr, (d) 1.5 hr and (e)2.0 hr of citric acid etching. The black arrows in (a) and (b) are pointing towards pore features that are present on the surface prior to etching. Meanwhile, the white arrows in (d) and (e) represent pit features which become present as the etch process develops.

Example images of the surface at various points during the citric acid etch are shown in ***Figure 4.2.*** As can be seen from the etch progress images, holes develop on the surface; these features grow in size as the etch progresses. Potential sources of preferential etch sites are grain boundaries, grain boundary triple points or surface defects[124], [147], [148]. Examples of surface defect features are noted to be present on the surface of ***Figure 4.2(a)***. These features are referred to as pinholes and are an artefact from thin film physical vapour deposition processes[149]. In order to determine preferential etch sites, a single area

on the surface would need to be monitored throughout the etch development. Another limitation in the Cu (50 nm)/ Ta (7 nm)/ Si (100) sample is that individual grains are so small they cannot be resolved in the AFM in great detail, making analysis of grain boundaries and grain boundary triple points difficult.

The ACL (ζ) plot of phosphoric acid in ***Figure 4.1(b)*** initially sees an increase in ACL with increasing etch depth. As a result, the spatial roughness is perceived to increase. This may be assumed as an indicator that the phosphoric acid initially polishes the surface as is expected for an electrochemical etch taking place at the I-V plateau. However, the increase in the RMS roughness opposes this. Instead, as seen in citric acid, preferential etch sites can cause holes in the surface. These holes dominate the measurement of the ACL, making the surface between pits appear smoother by comparison. Past the initial second, the ACL decreases, meaning the spatial change in height increases. This result indicates that the etch removes material preferentially, as opposed to polishing the surface. Looking at the surface images in ***Figure 4.3***, the surface after 1 second of etching is relatively flat with a series of pit features. Similar features are seen for the 2 and 3-second samples.

The ACL (ζ) of the formic acid-etched surface as a function of the film thickness removed is also shown in ***Figure 4.1(b)***. Like phosphoric acid, the spatial roughness of the formic acid initially appears to decrease, as indicated by the large increase in the ACL. The sample's ACL then drops again. However, unlike phosphoric acid, the oxidation-etch process shows spatial roughness increases again, meaning there are periods of roughening and smoothing which take place. Compared to citric acid, both formic acid and phosphoric acid never achieve a similar level of spatial smoothness. AFM images of the formic acid etch shown in ***Figure 4.3*** do show hole features on the surface. The hole features identified in formic acid etching do not grow to the same size as those in the citric acid etch (***Figure 4.2***). These features provide a false sense of a smooth surface compared to phosphoric acid. Towards the latter end of the ACL plot, formic acid etching provides a slightly smoother surface compared to phosphoric acid, making it more desirable for the 10 nm thickness range desired for the final film.

The final metric used to evaluate roughness is the cube counting fractal dimension. A comparison of the fractal dimension against etch depth is shown in ***Figure 4.1(c).*** The previous two metrics analyse vertical roughness and spatial variation separately. The fractal dimension simplifies roughness in both dimensions into a single parameter. The citric acid

etch initially decreases the surface fractal dimension indicating etching starts by smoothing the surface. After the initial decrease, the fractal dimension increases again. The fractal dimension, however, does not increase to the same level of the initial surface. Alongside this, the fractal dimension at 7.3 ± 0.4 nm, 14 ± 2 nm and 21 ± 1 nm remain constant.

In the cube-counting process, a cubic lattice is applied to the surface. The length of a cube's edge (l) is measured and the number of cubes which contain surface pixels, N(l), are counted. The edge length is decreased by a factor of 2, and the counting process is repeated. The steps are repeated until l is the distance between two adjacent pixels. A log-log plot of cube count versus 1/l gives the fractal dimension. The citric acid surface has a series of defined holes which are deeper than the general etch front. These features are prominent height deviations which make the general surface appear smoother by comparison to these features. As such, the fractal dimension of the etched surface may be seen as lower than the clean surface.

The cubic counting fractal dimension of phosphoric acid also shows an initial decrease during etching. The decrease in roughness is most likely linked to the decrease in spatial roughness. Looking at ***Figure 4.3(b)***, the etch leaves a series of pits on the surface. Between these pits, the sample surface looks relatively flat. This influences both the ACL and the fractal dimension, giving lower spatial roughness values. The same phenomenon is observed in citric acid. After this point, the fractal dimension increases to a plateau. Unlike citric acid, phosphoric acid samples show fractal dimensions higher than the initial surface after etching away 11 ± 3 nm. The increase in roughness detected supports that phosphoric acid is etching as opposed to polishing. Comparison with ***Figure 4.3***, shows these pit features grow, forming networks as the etch progresses. The loss of individual pit features coincides with a decrease in the ACL and the heightened fractal dimension values.

The cube counting fractal dimension in formic acid etched samples decreases up to a thickness of 19 ± 2 nm. Post this, the fractal dimension increases to a roughness above that of the original surface. Like citric acid, the formic acid etched surfaces seen in ***Figure 4.6*** do contain a number of hole features. These features persist throughout the etch process. However, as the etch progresses, their prominence against the etch front does not appear to be maintained.

Comparing all three etches together, formic acid has the lowest RMS roughness at each depth point, while citric and phosphoric acid behave in a similar fashion. At all

comparable points the fractal dimension of the formic acid etch is closer to a two-dimensional surface compared to both the citric acid and phosphoric acid. In terms of ACL, citric acid appears to have the lowest spatial roughness. This, however, is attributed to the hole features the citric acid leaves on the surface. The strong controllability of the formic acid etch rate combined with the RMS and fractal dimension performance indicates that formic acid provides both strong control of the etch rate and a relatively smooth surface when compared with the other etch methods considered.

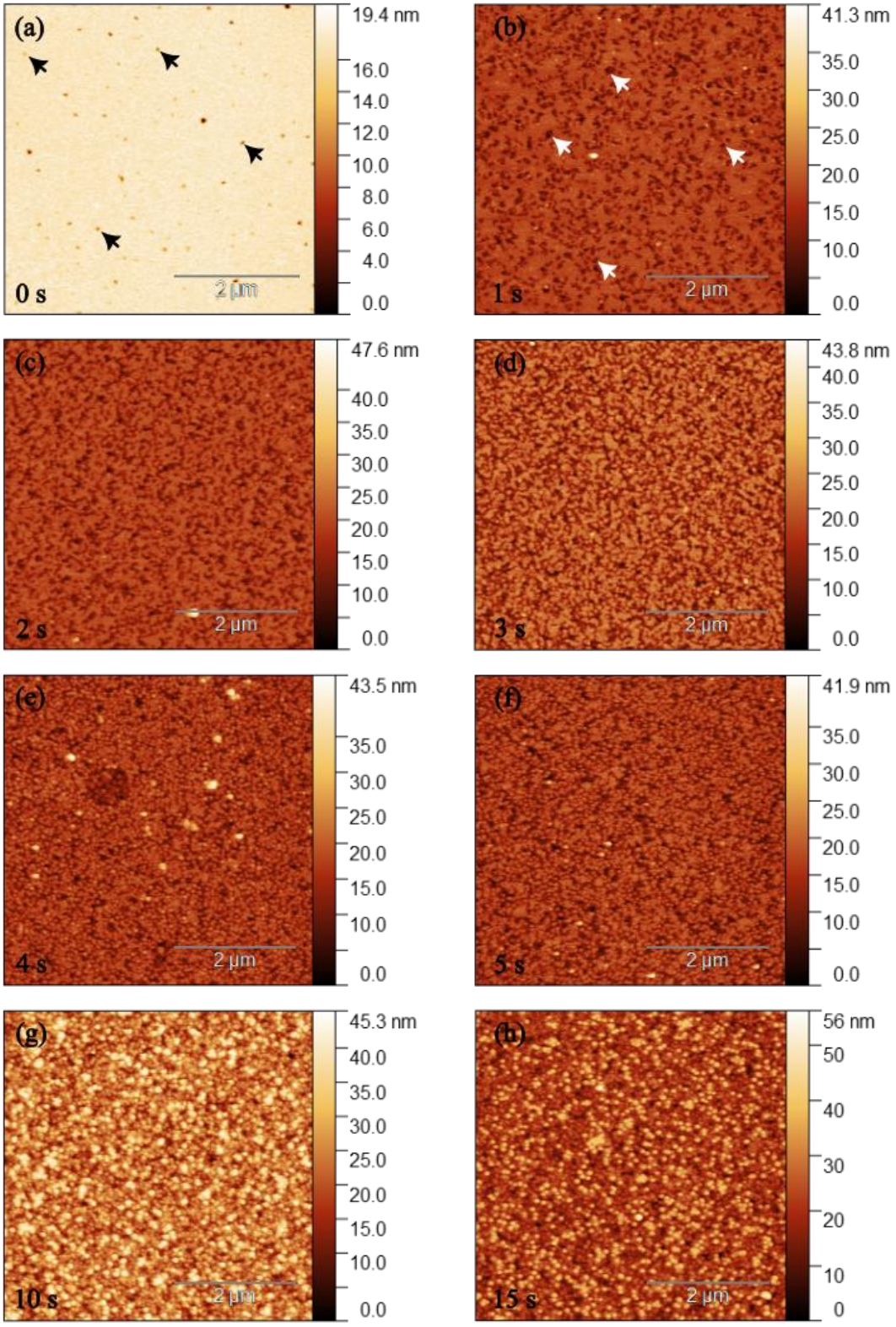

Figure 4.3: 5 µm AFM images at (a) 0 s, (b) 1 s, (c)2 s, (d) 3 s, (e)4 s, (f)5 s, (g) 10 s, and (h) 15 s of phosphoric acid etching. The black arrows in (a) indicate examples of the pinhole features seen on the surface prior to etching. The white arrows in (b) indicate the etch pits that form on the surface because of the etch process.

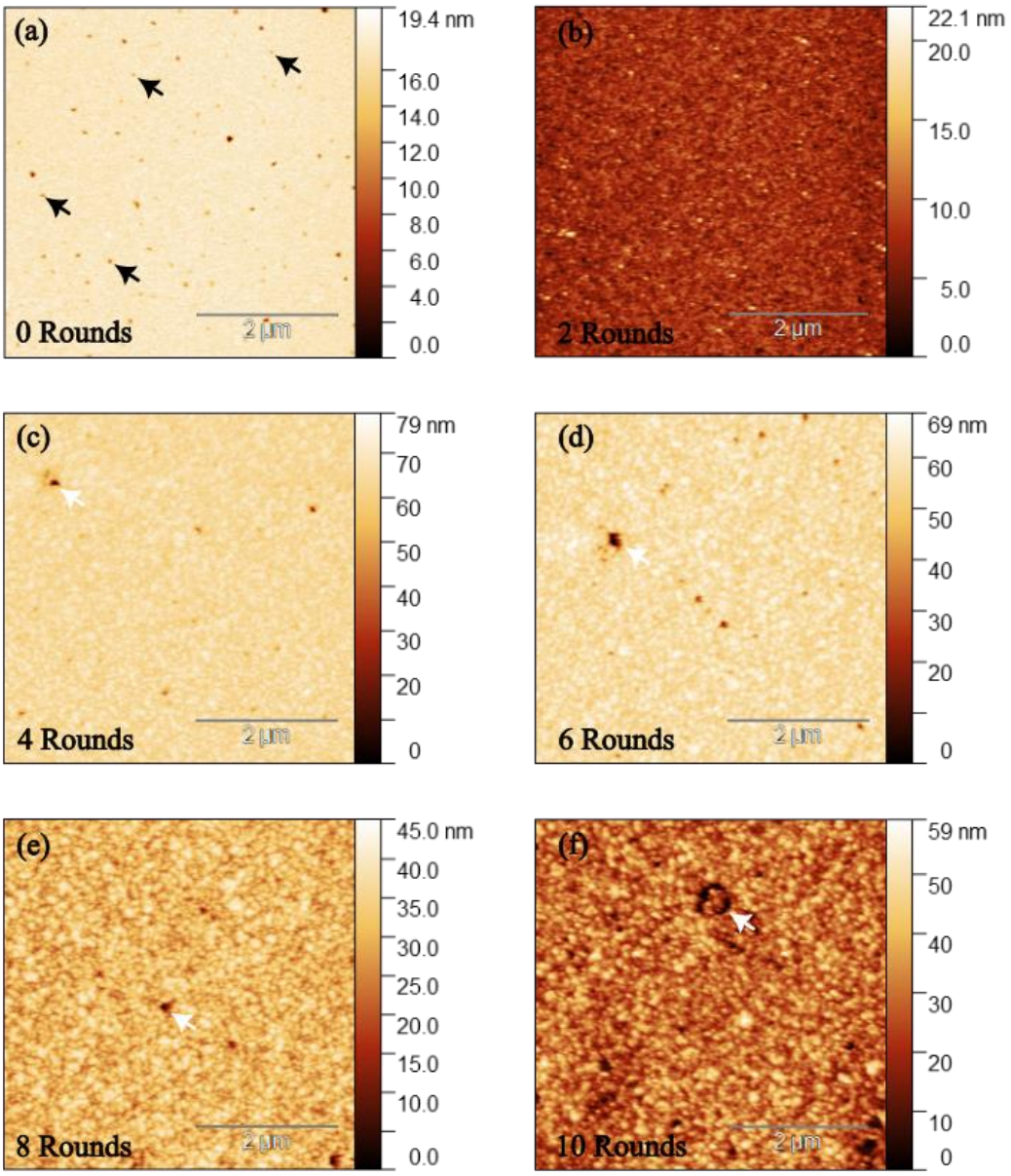

Figure 4.4: 5 µm AFM images at (a) 0 rounds, (b) 2 rounds, (c)4 rounds, (d) 6 rounds, (e)8 rounds, and (f) 10 rounds of oxidation-formic acid etching. The black arrows in (a) represent examples on the pinhole features present on the surface prior to etching. The white arrows in (c), (d), (e) and (f) show pit features that develop on the surface because of etching.

4.2 FORMIC ACID VERSUS ACETIC ACID AS AN ETCHANT

As stated in the previous chapter, studies of copper corrosion often compare formic acid corrosion with acetic acid corrosion. The same comparison is made in the following section. The citric acid and phosphoric acid roughness results are omitted from ***Figure 4.5*** for ease of interpretation. As can be seen in ***Figure 4.5,*** the RMS roughness of the copper surface submerged in acetic acid decreases as a function of etch depth for the submersion of copper in pure acetic acid. This is in opposition to the roughness analysis done by Chavez and Hess[146] and the behaviour of copper submerged in citric acid which both show an increase in the roughness as the etch develops. There is potential that the decrease in RMS roughness is due to a reduction in the height difference between the pin holes and the average surface height. AFM images of the surface during etch processing are seen in ***Figure 4.6***. When the acetic acid etches the surface, holes appear on the surface. This was also seen in ***Figure 4.3*** for citric acid. However, the hole sizes seen in acetic acid are clearly smaller than those seen in citric acid.

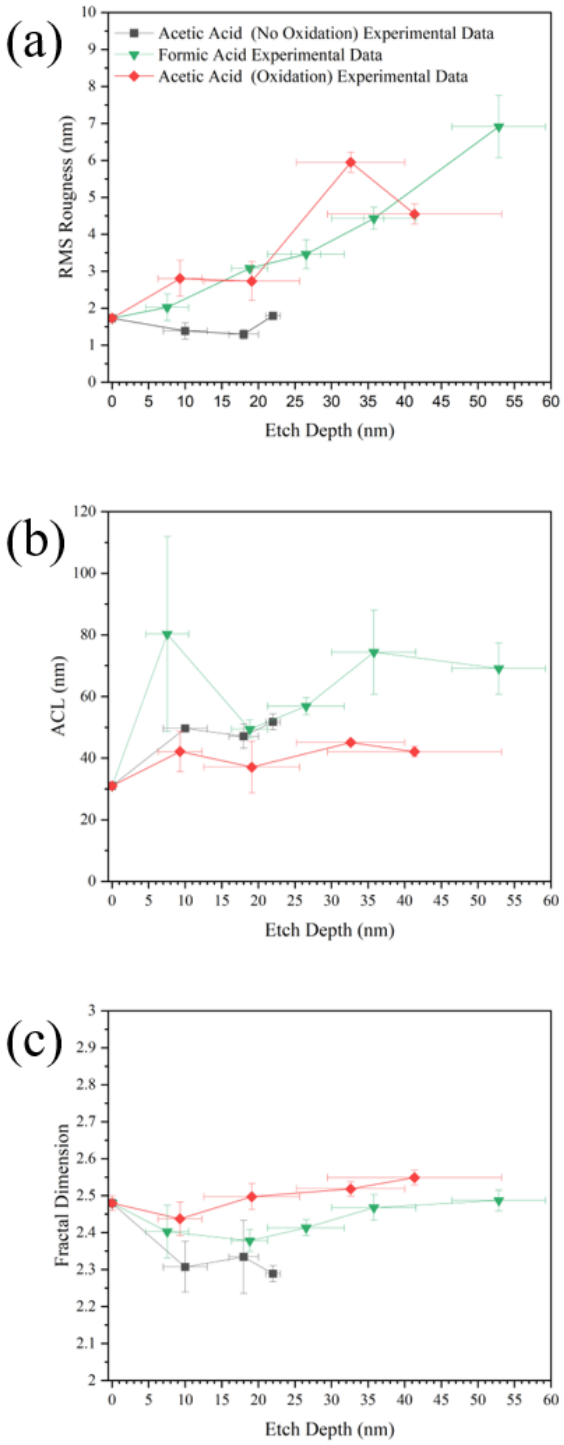

Figure 4.5: Scatter plots of roughness descriptors for sample surfaces versus the thickness of film removed. All three plots compare acetic acid submersion etch (Red), formic acid etch using plasma oxidation (Blue) and acetic acid using plasma oxidation (Green). (a) Root mean square roughness vs etch depth, (b) Auto correlation length vs etch depth and (c) cube counting fractal dimension vs etch depth.

The ACL of the submerged acetic acid, shown in ***Figure 4.5(b),*** is seen to increase throughout the development of the etch. Likewise, the cube counting fractal dimension of the copper surface submerged

in acetic acid in ***Figure 4.5(c)*** also shows a general trend of decreasing roughness with time. If the shallower pores are no longer discernible from the etch front, a smaller number of deeper pores in the surface are left behind. The remaining pores would be spaced further apart, explaining the increasing ACL and the decreasing fractal dimension. Alongside this, the remaining pores would have a smaller perceived depth. The trend of decreasing roughness continues until 22 ± 1 nm etch depth, where the RMS roughness increases to 1.80 ± 0.08 nm. This is slightly rougher than the initial surface.

By comparison, the submerged acetic acid etch outperforms the oxidation-formic acid etch in terms of RMS roughness. The auto-correlation lengths of the two etches are largely similar, with the exception of the auto-correlation length of formic acid at 8 ± 3 nm, which largely exceeds the autocorrelation length of acetic acid. The cube-counting fractal dimension comparison shows that acetic acid outperforms formic acid. The RMS and fractal dimension comparison gives some evidence that a hybrid etch using the process employed with formic acid using glacial acetic acid as the wet chemical etchant may be an optimal etch.

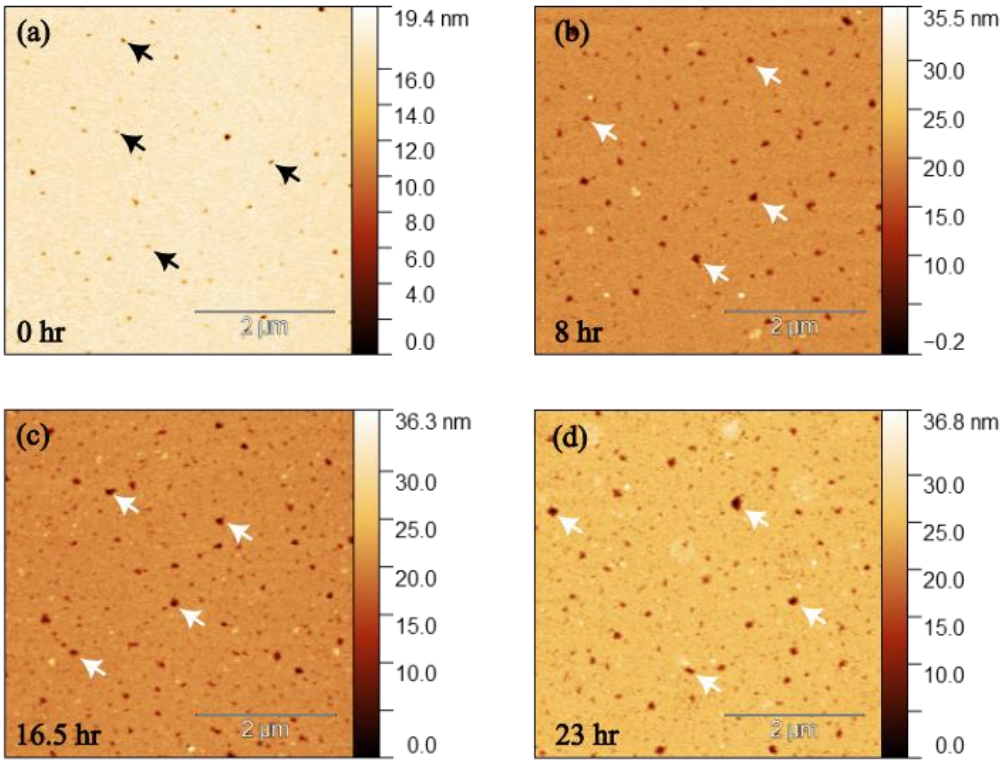

Figure 4.6: 5 µm AFM images at (a) 0 hr, (b) 8 hr, (c)16.5 hr and (d) 23 hr of acetic acid etching. The black arrows in (a) highlight hole features present in the film prior to any etch processing in the film. The white arrows in (b), (c) and (d) are hole features that develop on the surface as a function of etch processing.

The results of an oxidation-acetic acid etch are shown in ***Figure 4.5,*** alongside the roughness results of the submerged acetic acid etch, and the two-step formic acid etch. Comparison of the root mean square roughness versus etch depth for acetic acid and formic acid do not provide a clear preferential etchant at some points during the acetic acid etch process; the acetic acid provides a lower RMS roughness compared to formic acid. Likewise, there are also points during the etch development where formic acid provides a vertically smoother etch compared to acetic acid. Both etches show a similar trend for increasing RMS roughness with the amount of etch material removed.

The ACL analysis of the oxidation-acetic acid etch shows the spatial change in surface height occurs over much shorter distances compared to both the acetic acid submersion and the oxidation-formic acid etch process. Unlike formic acid, acetic acid also does not show as strong an increase in ACL with the amount of material removed. Comparing the AFM images of the formic acid surface (***Figure 4.4***) with the acetic acid surface (***Figure 4.7***), both surfaces show hole features. However, the hole features do not appear as strongly in the acetic acid etch. The low ACL in the acetic acid etch could indicate that acetic acid has fewer preferential etch sites. As such, acetic acid could be a better choice of etchant.

The final plot included in ***Figure 4.5(c)*** is the cube counting fractal dimension. Of all the etch processes considered, the copper sample submerged in acetic acid provided a surface that was closest to a perfectly flat 2D surface. Following on from this is the oxidation-formic acid etch process. According to the fractal dimension plot, the roughest surface is the oxidation-acetic acid etch sample. The same interpretation can be made when looking at both the RMS roughness and ACL results together. A combination of all three analyses indicates formic acid etching provides a smoother finish on the surface. However, the oxidation-acetic acid etch surfaces show fewer pore features. Acetic acid also has the added bonus of providing smaller etch steps, allowing for better control of the film's thickness and being able to be cleaned from the surface without leaving behind acetic acid as a surface contaminant. [146]

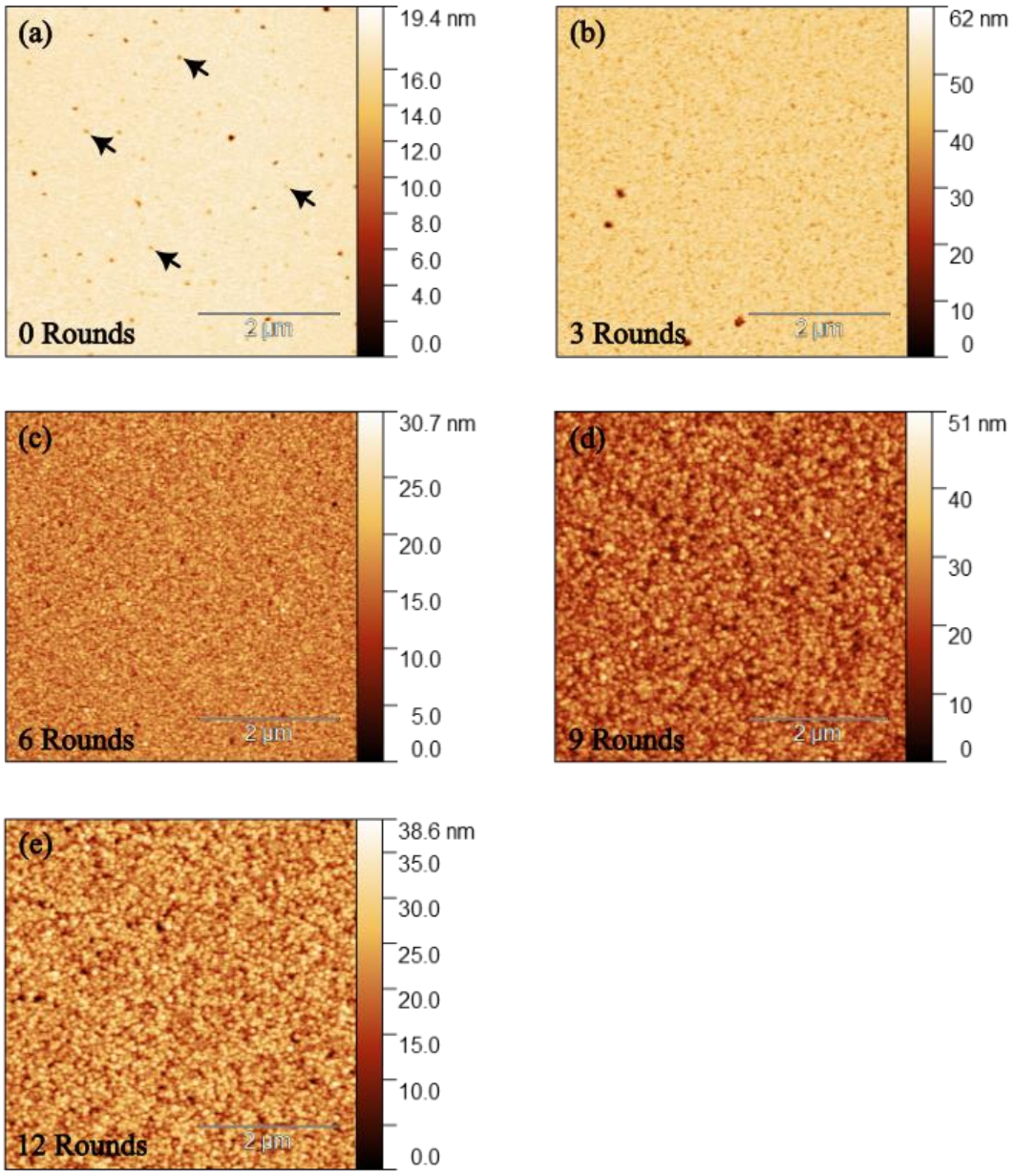

Figure 4.7: 5 µm AFM images at (a) 0 rounds, (b) 3 rounds, (c) 6 rounds, (d) 9 rounds, and (e) 12 rounds of oxidation - acetic acid etching. The black arrows in (a) highlight the pore features present in the initial surface prior to any etching.

5 SURFACE RECOVERY VIA ANNEALING

The rapid decrease in feature size seen in ultra-large scale integrated (ULSI) circuits have highlighted the influence microstructure has on mechanical properties and how microstructure can be exploited to improve performance[150]. For interconnects, films with large grain diameters, narrow grain size distributions and smooth surface/interfaces are desired in order to minimise electrical resistivity. As a result, methods which optimise grain size are crucial in the development of interconnects.

Many previous studies have focused on the effects of varying deposition parameters to enhance grain size. In depositions, there are several parameters which can be adjusted to change the resulting film. Examples are; deposition method, growth rate, nature of substrate, concentration of reagent, substrate temperature or growth environment. However, deposition processes are complex processes[151]. As such, changing deposition conditions cannot guarantee films with desired properties.

As an alternative, post-deposition treatments such as sputtering, annealing or room temperature recrystallisation can be employed as complementary processes to deposition control to optimise grain size, grain size distribution and roughness [151]. Annealing is a process in which the surface morphology of a film is modified using temperature and time[152]. Thermal annealing has been employed to liberate stress, improve film structure, minimise defects and control roughness. In single-crystal films, annealing causes thermodynamically driven mass transport on the surface. This allows step density on the surface to decrease. Fewer steps on the surface spaced further apart lowers the vertical height difference on the surface, creating a lower root mean square (RMS) roughness as well as a larger autocorrelation length (ACL)[153]. For polycrystalline films, annealing allows grain boundaries to rearrange themselves and for grains to grow. Grain boundaries are planar defects. Eliminating them makes the film smoother, improving film roughness.

Annealing is also capable of roughening the surface via a process known as agglomeration. Agglomeration is the thermally activated break up of a thin film into individual islands. This process occurs at temperatures below the melting point of the metal. Agglomeration has two stages; void nucleation and void growth. Void nucleation can occur homogenously, or film defects such as pinhole defects, grain boundaries and grain boundary triple points act as sources for void nucleation. When a grain boundary is a void

source, the grain boundary forms a depression along its intersection with the free surface. This is referred to as thermal grooving. The depression continues to deepen until the groove hits the substrate, creating a void. Once a void is created, it can grow. The same process occurs at grain boundary triple points. When several of the voids grow and overlap, the film becomes a series of isolated islands as opposed to a continuous film.

5.1 AFM STUDY OF THE 50 NM COPPER 7 NM TANTALUM/SILICON

5.1.1 Effect of a Single Anneal Step

In order to understand the influence of annealing on surface roughness, AFM analysis on the surface before and after a single anneal round was performed. An AFM image of a Cu (50 nm)/ Ta (7 nm)/ Si (100) sample prior to any annealing is shown in ***Figure 5.1(a)***. The mean grain size for the sample was d= 51 ± 20 nm. The grain diameters were obtained by extracting line profiles from several AFM images and counting the number of grains per line profile. The length of the line profile was divided by the number of grains to find the grain diameter. The histogram of grain diameters, shown in ***Figure 5.1(b),*** is monomodal, indicating abnormal grain growth did not occur during deposition. The initial roughness parameters of this sample were root mean square (RMS) roughness (ω): 0.63 ± 0.04 nm, Autocorrelation length (ξ): 45 ± 2 nm, and cube counting fractal dimension (D_F) 2.297 ± 0.001.

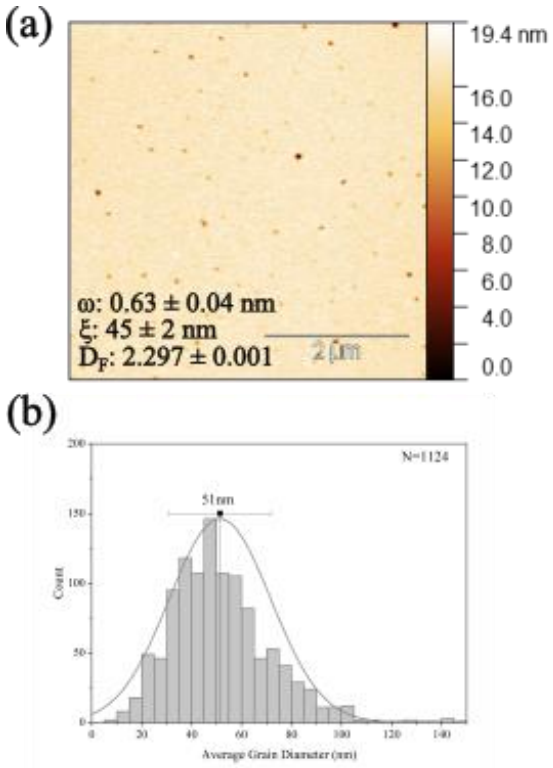

Figure 5.1: (a) 5 μm AFM image of the as-deposited copper surface. (Insert) The RMS roughness (ω), autocorrelation length (ξ) and fractal dimension (D_F) of the as-deposited surface averaged over several AFM images. (b) Distribution of grain sizes in the as-deposited Cu (50 nm)/ Ta (7 nm)/ Si (100).

Zhang et al. [12] used several anneal cycles under vacuum to restructure the grain boundaries and minimise surface roughness. Each anneal was approximately 350 °C and 20 minutes long. To approximate this, the same 50 nm thick copper films were subjected to a thermal anneal round in a tube furnace under an inert atmosphere at T=350 °C for a

time of t=90 min. The result of the anneal process can be seen in ***Figure 5.2(a)***. The average grain diameter increased from d = 51 ± 20 nm to d=114 ± 47 nm. The increase in grain size leads to fewer grain boundaries per unit distance. Annealing decreases the contribution of grain boundary scattering to the resistance on the film. That being said, the increase in the grain size distribution that results is less desirable as it is a potential source of flux divergence for electromigration. The histogram of grain diameters in ***Figure 5.2(b)*** also shows potential for a bimodal distribution. As a result, abnormal grain growth is possibly occurring during the anneal process.

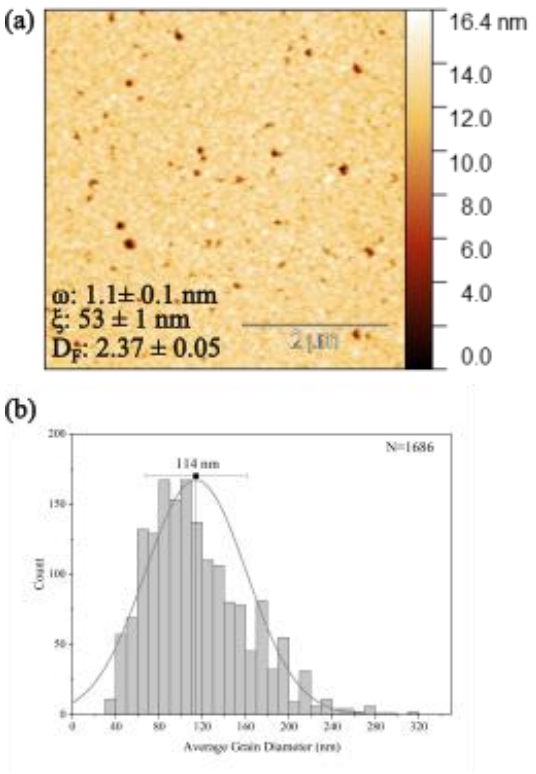

Figure 5.2: (a) 5 μm AFM image of the copper surface after a single anneal (Round 0). (Insert) The RMS roughness (ω), autocorrelation length (ξ) and fractal dimension (D_F) of the annealed surface averaged over several AFM images. (b) Distribution of grain sizes in the annealed Cu (50 nm)/ Ta (7 nm)/ Si (100).

The roughness parameters of the annealed sample were root mean square (RMS) roughness (ω): 1.1 ± 0.1 nm, Autocorrelation length (ξ): 53 ± 1 nm, and cube counting fractal dimension (D_F) 2.37 ± 0.05. Compared to the initial sample, the annealed sample shows a slight increase in vertical roughness and a decrease in horizontal roughness. The fractal dimension indicates that the surface has moved closer to a three-dimensional object as opposed to a two-dimensional surface. The increase of the RMS roughness, as well as the fractal dimension, show that features on the surface have a larger variation in height, which effectively means there is a variation in the film thickness across the film that will have an impact on electrical conduction. This is discussed further in ***Chapter 6.*** However, it is important to realise that this could also arise from deepening of the pinhole defects, grain boundary and grain boundary triple point grooving, or some combination of these effects.

The increase in the autocorrelation length is most closely related to the increase in grain size. Initially, the grain size measured from the AFM images and the autocorrelation length have a strong overlap. Post-annealing, the autocorrelation length is nearly half the

mean grain size. If the grain's boundaries groove as the grains grow, the grains move from being planar features to groove-like features on the surface. As such, the autocorrelation length is only a fraction of the grain size as opposed to being the same as the grain size. Though grain growth occurs at 350 °C, the increased number and size of the pinholes in ***Figure 5.1*** and ***Figure 5.2*** indicate unwanted processes such as deepening of the pinhole defects, grain boundary grooving and grain boundary triple point grooving occur.

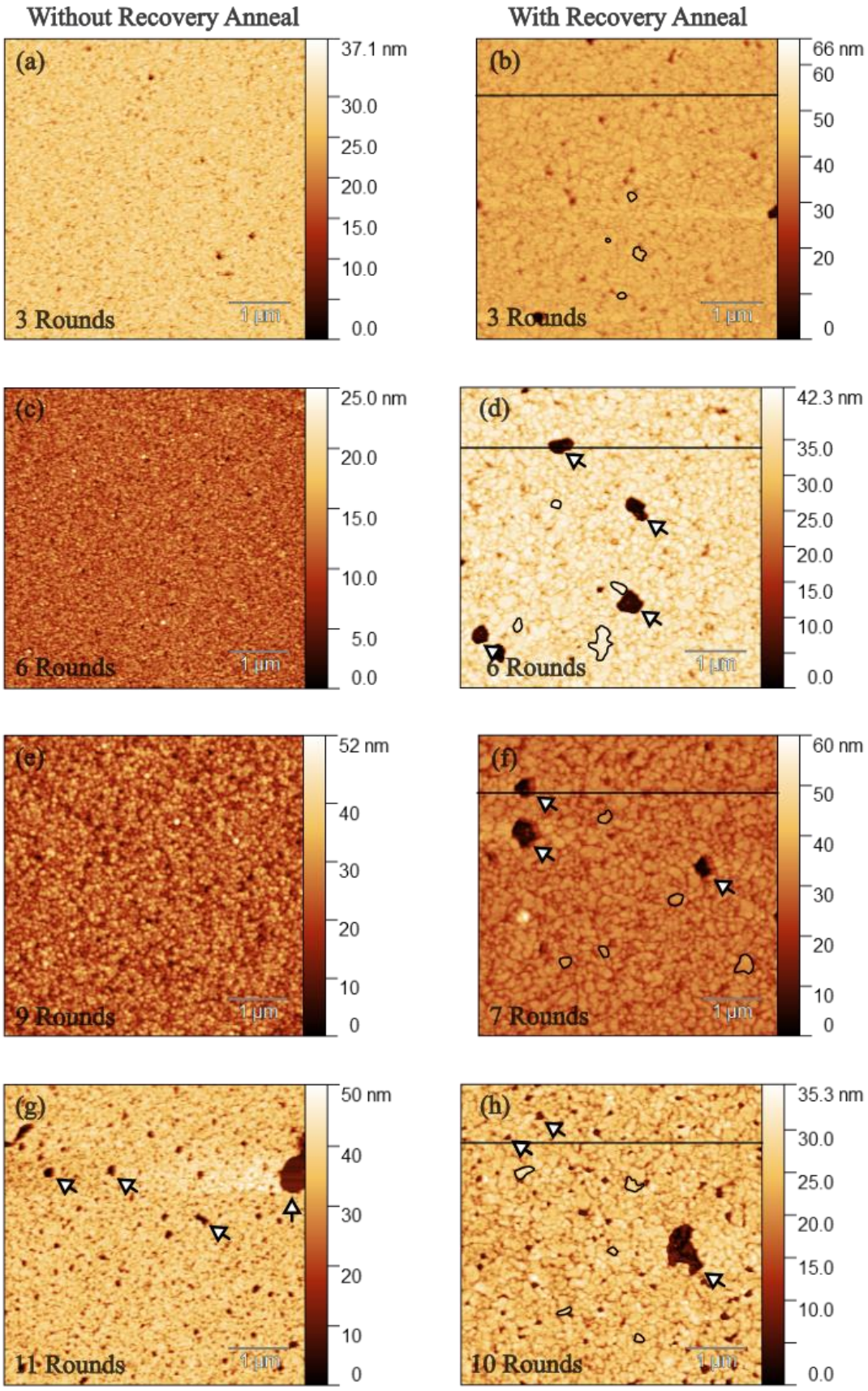

Figure 5.3: 5 µm AFM images of the surface post etching. On the left-hand side are the surfaces etched without recovery anneals between etches. Meanwhile on the right-hand side, each etch round is punctuated with an anneal done under the same conditions as the initial anneal. The black lines present in (b), (d), (f) and (h) represent the locations for the line profiles shown in ***Figure 5.7.*** *The arrows in (d), (f), (g) and (h) indicate examples of hole features that develop on the surface as the etch progresses. Alongside this some grains in (b), (d),(f) and (h) are outlined for reference. The same could not be done for the without anneal set as the grains are too small to be outlined in 5µm images.*

5.1.2 Effect of Annealing Between Oxidation Etch Rounds.

As the copper film is etched via the plasma oxidation–glacial acetic acid process described in ***subsection 2.4.1***, the roughness of the sample increases. To counter this, annealing can be used to allow the step density of the surface to decrease. AFM images of the etched surfaces without an anneal step between etch rounds are shown in ***Figure 5.3(a), (c), (e)*** *and* ***(g)***. For comparison, images taken at the same etch points using a process that included an annealing step are shown in **Figure 5.3*(b), (d), (f)*** and ***(h)***. Immediately obvious, by comparing the two image sets, there is a significant difference in grain size.

The average grain size as a function of the etch round was analysed and plotted, as shown in ***Figure 5.4***. The average grain size remains constant as a function of the process round for the samples without recovery annealing. Small variations between process points can be accounted for by sample inhomogeneity or different tip-sample convolutions. For the recovery anneal set, an initial anneal is completed prior to any etch (Etch round number 0). As shown in ***Figure 5.1*** to ***Figure 5.2***, the first anneal induces grain growth. However, after this anneal, there is no increase in either the average grain size or the grain distributions. The histograms produced monomodal distributions similar to that seen in ***Figure 5.2(b)***. This suggests that no further grain growth, abnormal or otherwise, is occurring.

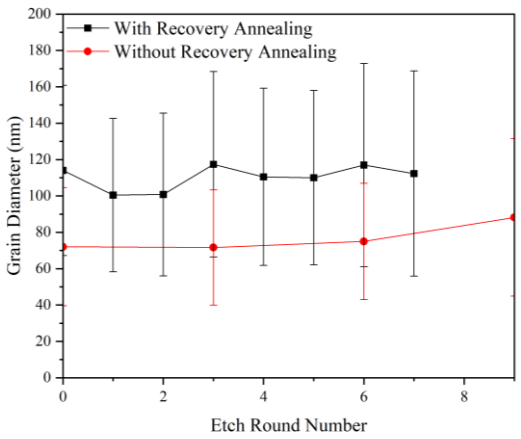

Figure 5.4: Scatter plot of average grain diameter vs etch round for samples. The etch process that does not include recovery anneals between etches is represented by red circles, Meanwhile the etch process containing recovery anneals between etches are given in grey. As can be seen a etch round 0, the grain diameter for the recovery anneal sample is much larger than that of the sample without recovery annealing. This is due to an initial anneal that is completed prior to any etch as expressed through ***Figure 5.1*** *and* ***Figure 5.2****.*

It is interesting to note the 3 Rounds, 6 Rounds, and 9 Rounds samples in the recovery anneal samples of ***Figure 5.3*** show larger hole features than that of their no recovery anneal counterparts. This supports the interpterion of the single anneal step. Grain growth occurs during the first anneal at 350 °C. After this, the grain size remains constant. Instead, potentially unwanted processes such as deepening of the pinhole defects, grain

boundary grooving, and grain boundary triple point grooving occur during subsequent etch and anneal rounds. At 10 Rounds and 11 Rounds, both the samples with and without annealing have hole features on the surface that contact the substrate surface, forming voids. Examples of these are shown in ***Figure 5.5***. For the 11 Rounds samples without annealing, the remaining sample should be 12.6 ± 1.1 nm thick. Hole depths in the film extend to 26 ± 5 nm into the film. Meanwhile, the 10 Rounds sample with annealing should have a film thickness of 16 ± 1 nm. The hole features were found to extend 18 ± 3 nm into the film, showing holes have contacted the tantalum substrate beneath.

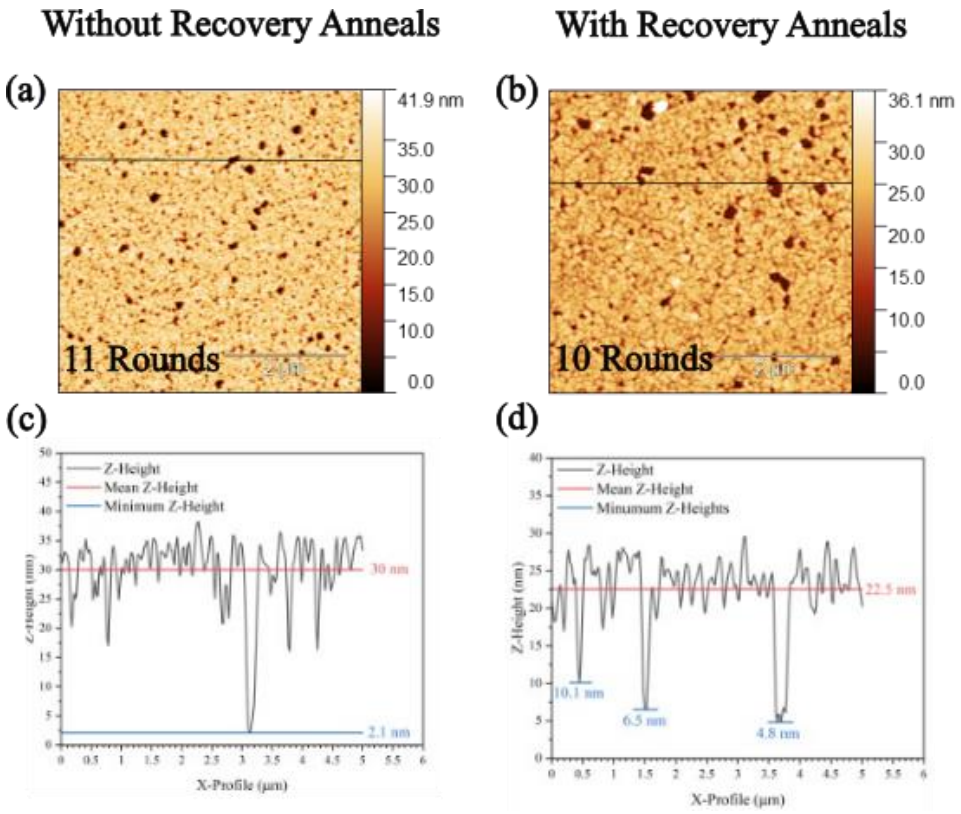

Figure 5.5: (a) 5 µm AFM image of 50 nm thin film after 11 rounds of etching. (b) 5 µm AFM image of 50 nm thin film after 10 rounds of etching with an anneal after each etch round. (c) A line profile extracted from (a) showing a hole feature on the surface. (d) A line profile extracted from (b)showing three hole features on the surface. The lowest Z-Height value measured in the AFM is set to 0 in the Gwyddion software. These values are also referenced as the 0-value in the line profiles provided in (c) and (d).

Root mean square (RMS) roughness analysis of the recovery anneal sample set is compared to its unannealed counterpart in ***Figure 5.6(a)***. It is important to note that there is a difference in roughness between the recovery anneal, and no recovery anneal samples prior to any processing. For the recovery annealing samples, a new wafer of 50 nm of Cu on 7 nm of Ta on Si had to be commissioned from Intel. As a result, the samples used in the recovery anneal samples come from a different parent wafer, contributing to differences in initial roughness. According to the RMS analysis, recovery annealing causes an increase in vertical roughness up to the 6th round; after this, the RMS roughness decreases. The additional roughness resulting from the anneal is either created from sites of increased preferential etch or thermal grooving at grain boundaries, triple point intersections and pinhole defects, as evidenced by the pit features on the samples that include recovery annealing. These features are particularly prominent in the comparison of 6 Rounds images. In ***Figure 5.3(c)***, there are no obvious hole features contrasted against the etch front. Meanwhile, in ***Figure 5.3(d),*** there are clear hole features against the etch front. Likewise, in ***Figure 5.3(c),*** there are no distinct features that can be associated with the grain boundaries. This is due to the grain size being below the resolution capability of the Asylum AFM. On the other hand, the larger grains in ***Figure 5.3(d)*** can be resolved. The boundaries between

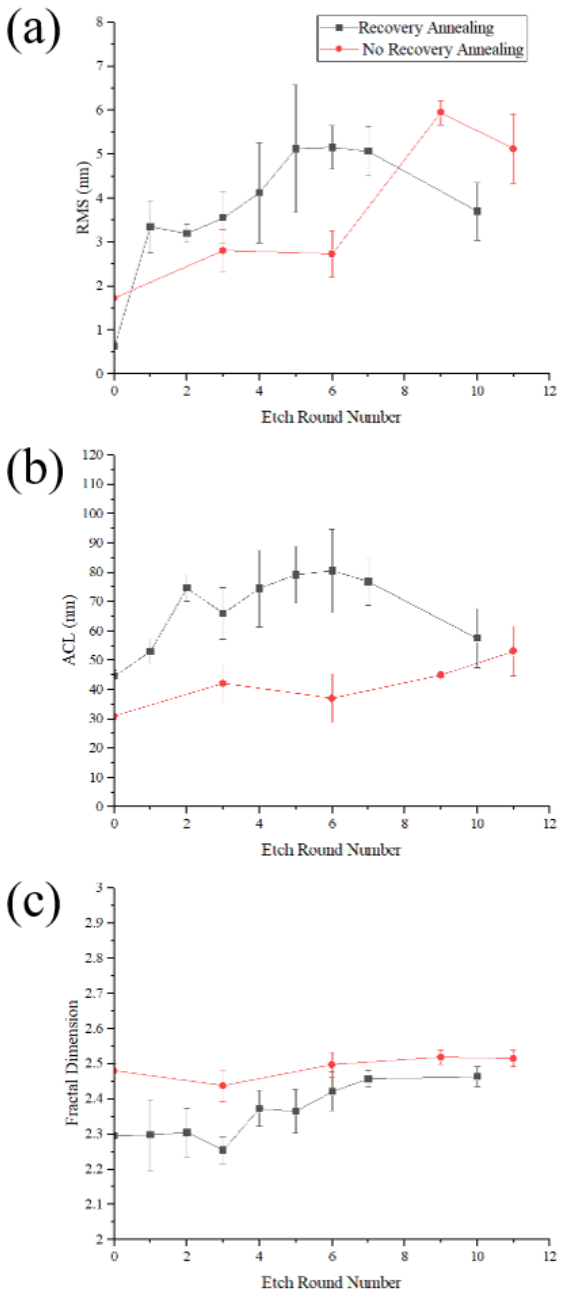

Figure 5.6 Cyclic acetic acid with (grey) and without (red)recovery annealing between etch rounds. (a) root mean square (RMS) roughness vs etch round; (b) Auto correlation length (ACL) vs etch depth and (c) cube counting fractal dimension vs etch depth. For the sample set with recovery annealing, there is an initial anneal that is completed prior to any etch. As a result, the starting roughness descriptors for the two samples are different.

grains are lower in height compared to the grain centre, resulting in them having a darker contrast to the grain centres.

The decreasing roughness seen after the 6th etch round is the result of a decreasing height difference between the general etch front and the pit features. For example, after 6 rounds of etching, the remaining film is 29.6 ± 0.6 nm thick. The film height difference between the etch front and the deepest pits of ***Figure 5.3(d)*** was found to be 32 ± 1 nm. Meanwhile, after 10 rounds of etching (***Figure 5.3(h)),*** the film is 16 ± 1 nm thick. The height difference between the average surface height and the maximum pit depth is 18 ± 3 nm.

In contrast to the increased vertical roughness shown in ***Figure 5.6(a)***, the horizontal roughness of the annealed samples in ***Figure 5.6(b)*** is decreased. Interestingly, the autocorrelation length continues to increase despite the fact the grain size remains constant after the first anneal. This indicates that the variation in height at the centre of the grains is overpowered by the grain boundary grooving or grain boundary etching that makes the vertical roughness decrease appear to decrease with annealing. Line profiles were extracted from ***Figure 5.3(b), (d), (f)*** and ***(h)*** and are shown in ***Figure 5.7***. In the 3 Rounds sample, the line profile varies in height over very short distances compared to the 6 Rounds and 7 Rounds line profiles. The change in height in 3 Rounds is detected on the grains as well as at the boundaries. Whereas 6 Rounds and 7 Rounds show distinct variations in height at the grain boundaries. After the 6th etch, the ACL decreases. With voids being nucleated on the surface, the grains will thermally groove at boundaries as the film moves from being continuous to a series of three-dimensional crystallites. The ACL decrease is an indicator that after 6 anneal rounds, agglomeration has

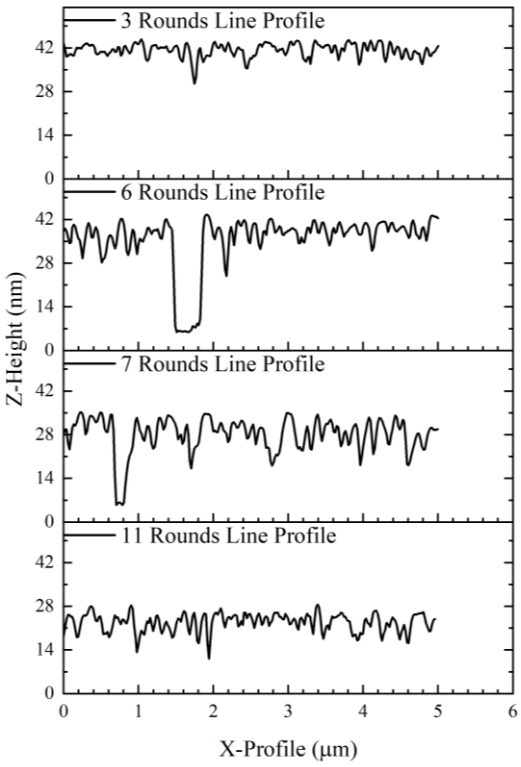

Figure 5.7: Line profiles extracted from 5 µm AFM images in Figure 5.3 (b), (d), (f) and (h). In each line profile, the round number represents the number of etch rounds the sample has undergone.

entered the void growth stage. This is supported by the average hole depth of 6 Rounds samples being the same depth as the remaining film.

The cube counting fractal dimension of the recovery annealed samples is represented in grey in ***Figure 5.6(c)***. The fractal dimension of recovery annealed samples appear closer to a 2D surface compared to samples without annealing, given by the red data points. At surface level, this result would support the idea that the anneal between etches allows the surface roughness to minimise. However, this interpretation overlooks the effect that the large pit features can have on the cube counting code. When large, vertical, well-spaced features are included in a surface, the variation in height of the remaining surface appears much smoother by comparison. This can give a false sense that the surface is, in general, very smooth compared to a surface without these pit features. One way to visualise the influence of hole features on the cube counting method is to compare the 6 Rounds line profile and 7 Rounds line profile shown in ***Figure 5.7***. The 6 Rounds and 7 Rounds samples have similar descriptions of roughness; however, the 7 Rounds line profile seems rougher than 6 Rounds profile because of the inclusion of a hole feature in the 6 Rounds line profile that dominates the vertical Z-height range, making the general etch front appear smoother by comparison.

The two types of processed films also appear vastly different when compared optically. Examples of the surfaces seen under light microscopy using x 50 magnification are shown in ***Figure 5.8***. After 3 rounds of etching, both samples are comparable. At 6 rounds of etching, dark spots appear on both samples. The dark spots on the copper without recovery annealing appear smaller and darker than those seen on the recovery-annealed sample. These features correspond to pits in the copper. At 9 Rounds, the features in the sample with no annealing appear similar to those in 6 Rounds. In opposition, the pit features within the 9 Rounds sample with recovery annealing have grown. This is in line with dewetting behaviour as pit features grow as dewetting progresses.

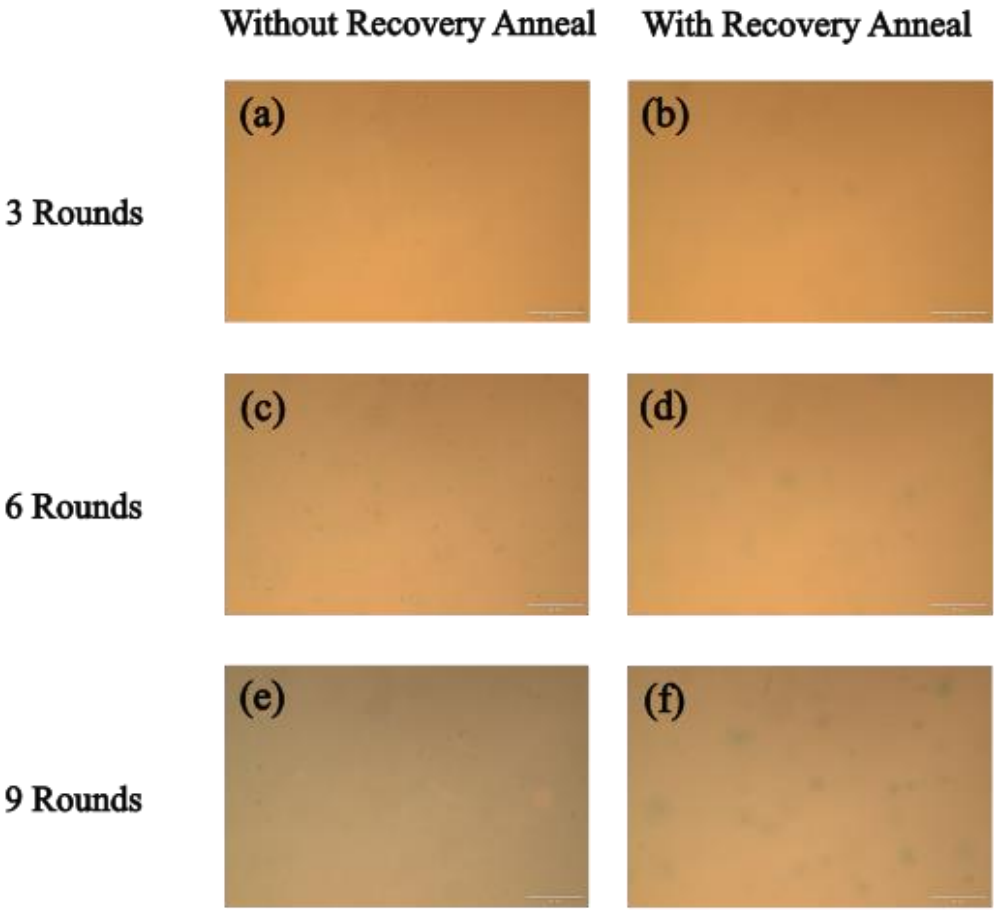

Figure 5.8: Optical images taken at x50 magnification. On the left-hand side are etched surfaces without recovery annealing. The right-hand side are etched surfaces with the recovery anneal step included between each etch. The scale bar present in each image indicates a distance of 50 μm.

5.2 STM STUDY OF THE 50 NM COPPER ON SILICON

In the original study by Zhang et al.[12] , the 50 nm copper film was sputtered and annealed to minimise surface roughness. The resulting surface had an RMS roughness of 0.5 nm over a 1 μm scale. A corresponding STM analysis was undertaken on a sample that had undergone 7 rounds of etching. The sample also underwent an anneal prior to etching and post each round of etching for a total of 8 anneals. The RMS roughness of the resulting sample is 2 ± 1 nm over a 1 μm

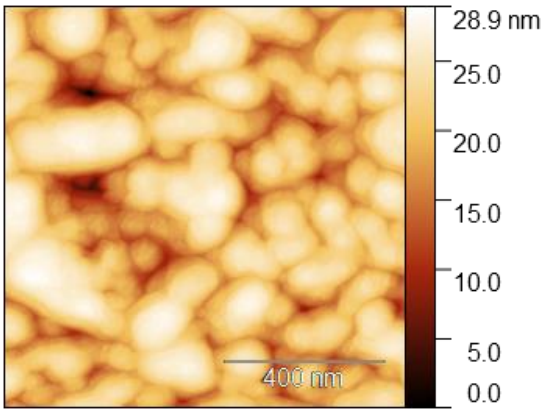

Figure 5.9: 1 μm STM image of a Cu(50 nm)/ Ta (7 nm)/ Si(100) sample after 7 rounds of etching. Prior to etching the copper undergoes an initial anneal at 350 °C for 120 minutes under inert atmosphere. The sample also undergoes the same anneal after each etch. Image taken at 5V at a setpoint of 0.03 nA

scale. This is a 300% increase from the roughness recorded from an unetched sample. The increase in roughness makes atomic studies at the grain boundaries rather difficult, as a majority of the change in Z-height occurs in the area surrounding the grain boundary.

After the seven rounds of etching, the resulting sample is 26.2 ± 0.7 nm thick, according to the etch rate analysis. As can be seen from ***Figure 5.9***, the max Z-height extends to the expected thickness range for the copper film. On average, the variation in Z-height across a 1 x 1 μm image is 17 ± 10 nm. This variation in height may indicate that a majority of the grain boundaries are either etched away or at least experience significant thermal grooving due to the number of recovery anneals completed on the sample prior to STM analysis.

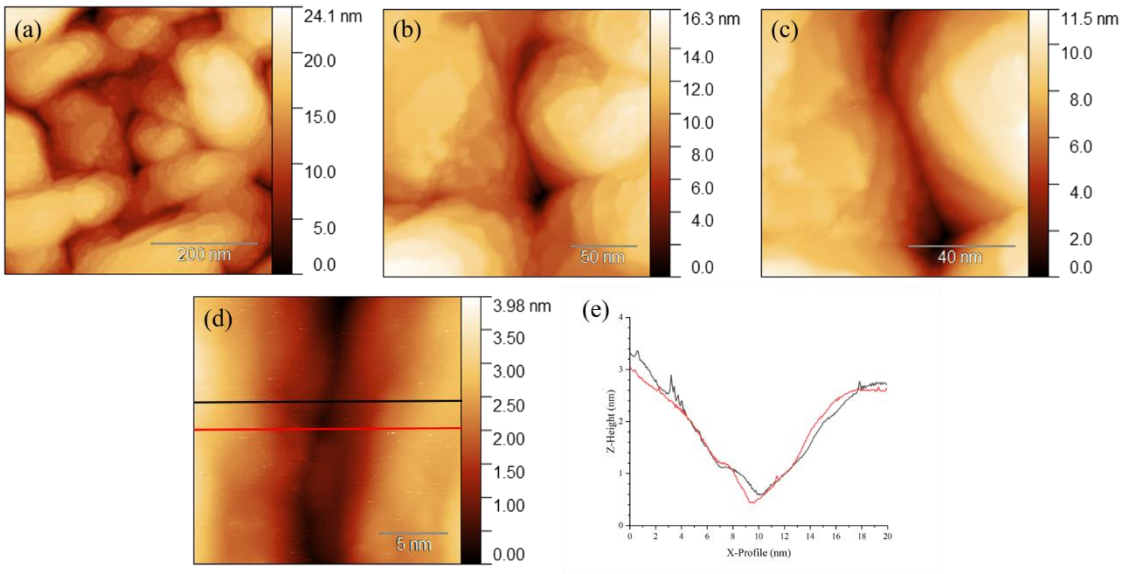

Figure 5.10: (a) 0.5 μm, (b) 0.2 μm,(c) 0.1 μm, (d) 50 nm STM images and (e) a 20 nm line profile taken from (d) of the copper surface post sputter-annealing. Image taken at 5 V at a setpoint of 0.03 nA.

On the 50 nm as-deposited sample, Zhang et al. [12] showed that grain boundaries were present at either ridge or valley locations between adjoining grains. The depth of the valley or ridge features extended up to 100 picometers over a distance of 10 nm. In the present study, the etch-anneal sample has valleys of varying grain boundary depths, an example of which is shown in ***Figure 5.10***. The two STM line profiles are taken from ***Figure 5.10(d)***, showing the extent of the depth of the boundary. Unlike Zhang et al. [12] work, the boundaries in the etch-anneal sample are, on average, 4 ± 2 nm deep. This makes obtaining atomic resolution at the grain boundary difficult as several surface states at the side of the boundary interact with the tip, preventing the acquisition of atomic resolution images and an examination of the detailed structure of the boundary.

5.3 AFM STUDY ON 60 NM COPPER ON AL_2O_3

5.3.1 Effect of a Single Anneal Step

In order to produce samples that could be electrically tested, a new substrate was required since the Intel-provided highly-doped silicon substrates used for STM studies allow current to leak between probes during four-point probe electrical testing. As a replacement, C-plane single-side polished sapphire substrates were used. The substrates have an average RMS roughness of 0.094 ± 0.006 nm, an average autocorrelation length of 61 ± 12 nm and a fractal dimension of 2.55 ± 0.02. 60 nm of copper was deposited onto the substrate by magnetron sputtering. The specific details of the deposition are given in ***subsection 2.4.3.*** As part of the deposition process, the copper samples were annealed under vacuum at 300 °C for 120 min. A third set of samples consisting of 50 nm of copper deposited onto 7 nm of Ta on a thick oxide on silicon are also under production as of the writing of this work.

The as-deposited surface prior to any etch processing is shown in ***Figure 5.11***. The initial surface has an average grain size of 398 ± 256 nm, making the copper grains 452.78 % larger compared to copper on tantalum on silicon samples. The surface also contains bright features that are nested within depression features corresponding to copper crystals that have evaporated during the 300 °C anneal applied as part of the deposition[154]. The histogram of grain diameters for the as-deposited sample is monomodal indicating that abnormal grain growth did not occur during deposition or during the post deposition anneal. Mechanical removal of the film from the substrate using a pair of blunted tweezers was possible, allowing for the exact thickness of the films to be determined. The average thickness of the films was

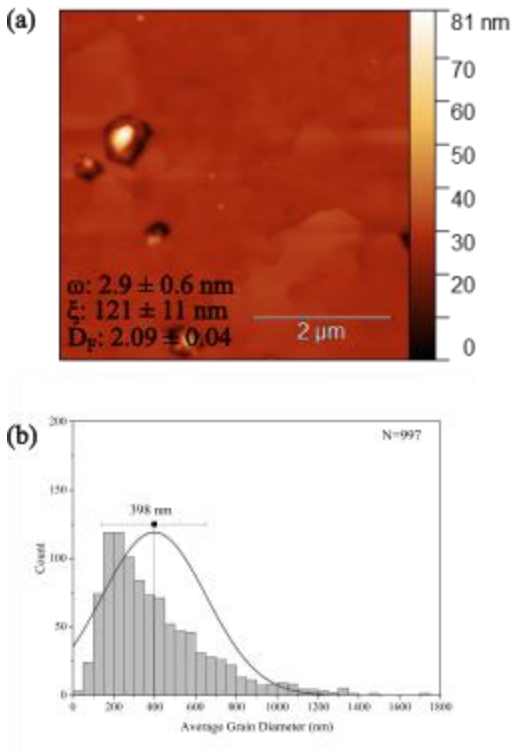

Figure 5.11: (a) 5 µm AFM image of the as-deposited copper surface. (Insert) The RMS roughness (ω), autocorrelation length (ξ) and fractal dimension (D_F) of the as-deposited surface averaged over several AFM images. (b) Distribution of grain sizes in the as-deposited Cu (60 nm)/Al_2O_3.

found to be 58 ± 4 nm. The initial roughness parameters of this sample were root mean square (RMS) roughness (ω): 2.9 ± 0.6 nm, Autocorrelation length (ξ): 121 ± 11 nm, and cube counting fractal dimension (D_F) 2.09 ± 0.04.

The same tube furnace anneal process used on the 50 nm copper on tantalum on silicon was applied to the sapphire samples prior to oxidation and etching. The results of this anneal are shown in ***Figure 5.12***. The average grain diameter is 523 ± 375 nm. This increase in grain size leads to fewer grain boundaries per unit area, thereby decreasing the contribution of grain boundary scattering to the resistance of the film.

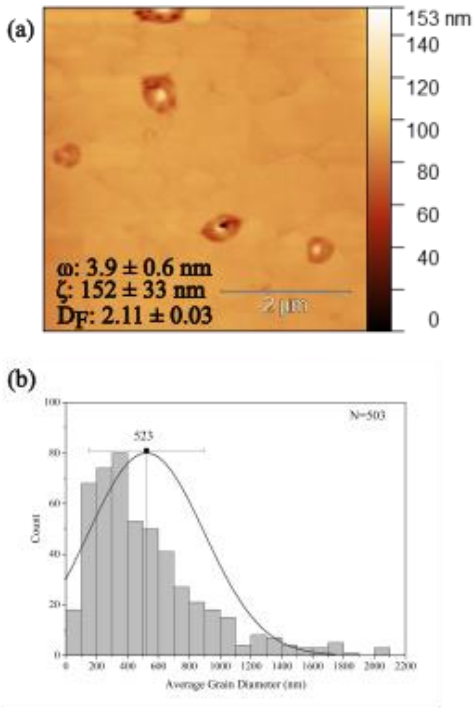

Figure 5.12: (a) 5 μm AFM image of the copper surface after a single anneal (Round 1). (Insert) The RMS roughness (ω), autocorrelation length (ξ) and fractal dimension (D_F) of the annealed surface averaged over several AFM images. (b) Distribution of grain sizes in the annealed Cu (60 nm)/ Al_2O_3.

The roughness parameters of the annealed sample were root mean square (RMS) roughness (ω): 3.9 ± 0.9 nm, Autocorrelation length (ξ): 152 ± 33 nm and cube counting fractal dimension (D_F) 2.11 ± 0.03. Compared to the initial sample, the annealed sample shows an increase in vertical roughness and a slight decrease in horizontal roughness. The fractal dimension indicates that the surface has moved closer to a three-dimensional object as opposed to a two-dimensional surface. The increase of the RMS roughness, as well as the fractal dimension, show that features on the surface have a larger variation in height. This could come from deepening of the hole defects or from grain boundary grooving and grain boundary triple point grooving.

5.3.2 Effect of Annealing Between Oxidation Etch Rounds

The copper films on Ta/Si substrates provided an average etch rate of 3.4 ± 0.1 nm per round. After 7 etch rounds, this gives the sample an average thickness of 26.2 ± 0.7 nm. The low adhesion between copper and Al_2O_3 meant the copper film could be removed mechanically from the substrate. After 7 rounds of etching, the remaining film on Al_2O_3

had an average thickness of 47 ± 12 nm. That means 7 rounds of etching is only capable of removing 12 ± 5 nm of material. This leads to an etch rate of 1.6 ± 0.7 nm per round. This is below half the etch rate seen for the Ta/Si sample sets. The decrease in etch rate is the result of a change in how the oxide develops on the surface. The oxidation of copper can be influenced by the orientation of the surface[144] and the size of the grains[155].

XRD was completed on the sample to determine the orientation of the thin copper film. The results of this analysis are shown in ***Figure 5.13***. The 60 nm copper film shows four peaks. The same analysis was performed on a bare Al_2O_3 wafer taken from the same batch as the Al_2O_3 that was used as the substrate. Three of the four peaks found in the XRD study of copper on Al_2O_3 originate from the Al_2O_3 substrate, leaving a single peak unaccounted for. Comparison of this peak position to XRD data from a polycrystalline copper foil identified the peak as the (111) crystallographic orientation. This is the same orientation as the quoted for the copper on silicon samples [12]. This is also supported by an analysis of Cu (50 nm) on Ta (7 nm) and Si(100), as shown in ***Figure 5.14***. In this analysis, three of the five peaks could be attributed to the Si (100) substrate. This leaves two peaks; one at 38.9° and 43.4°. The 43.4° corresponds to the (111) peak in the copper reference sample, indicating (111) oriented copper film. The small peak at 38.9 ° corresponds to the Ta adhesion layer[156]. Since the two copper films have the same orientation, the increase in grain size is responsible for the lower etch rate. The lower density of surface steps and grain boundaries available during oxidation decreases the thickness of the oxide layer formed during oxidation. This, in turn, decreases the etch rate per removal round.

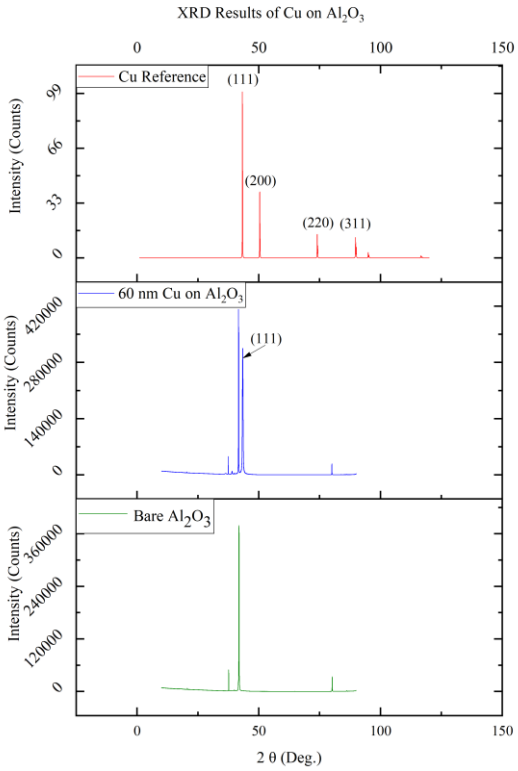

Figure 5.13: XRD pattern (a) from a polycrystalline copper reference sample (b)taken from an as-deposited Cu on Al_2O_3.and (c) taken from bare Al_2O_3.

As the copper film is etched, the roughness of the sample increases. The aim of annealing is to counter this. Annealing can decrease the step density of the surface, creating

a smoother finish. In the copper on silicon samples, the annealing process increases vertical roughness during etching due to boundary grooving. On the other hand, the autocorrelation length increases up to the 6th round, indicating that the horizontal roughness initially decreases. The autocorrelation lengths measured in this sample were far below the average grain diameter. This could indicate that the surfaces between boundaries become smoother. Alternatively, the decreasing horizontal roughness could be the result of the increasing influence of the etched grain boundaries on the height variation seen within the samples as the etch progresses.

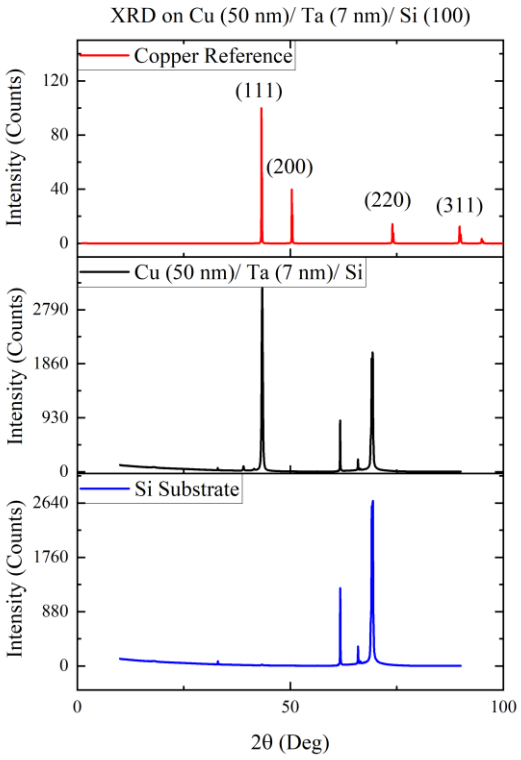

Figure 5.14: XRD pattern (a) from a polycrystalline copper reference sample (b)taken from an as-deposited Cu on Ta (7 nm) on Si(100).and (c) taken from bare Si(100)

The etch-anneal process employed on copper on silicon was also applied to copper on Al_2O_3. AFM images of the etch process with annealing steps between etch rounds are shown in ***Figure 5.15***. As the etch-anneal progresses, the grain boundaries can be seen to become darker in colour and depressed relative to the average surface height. The cause of this depression is likely due to grain boundary grooving during the anneal. In addition, at low temperatures, oxides will preferentially form at the boundaries. Since the acetic acid preferentially etches copper oxide over copper, the etch will be preferential to the boundaries.

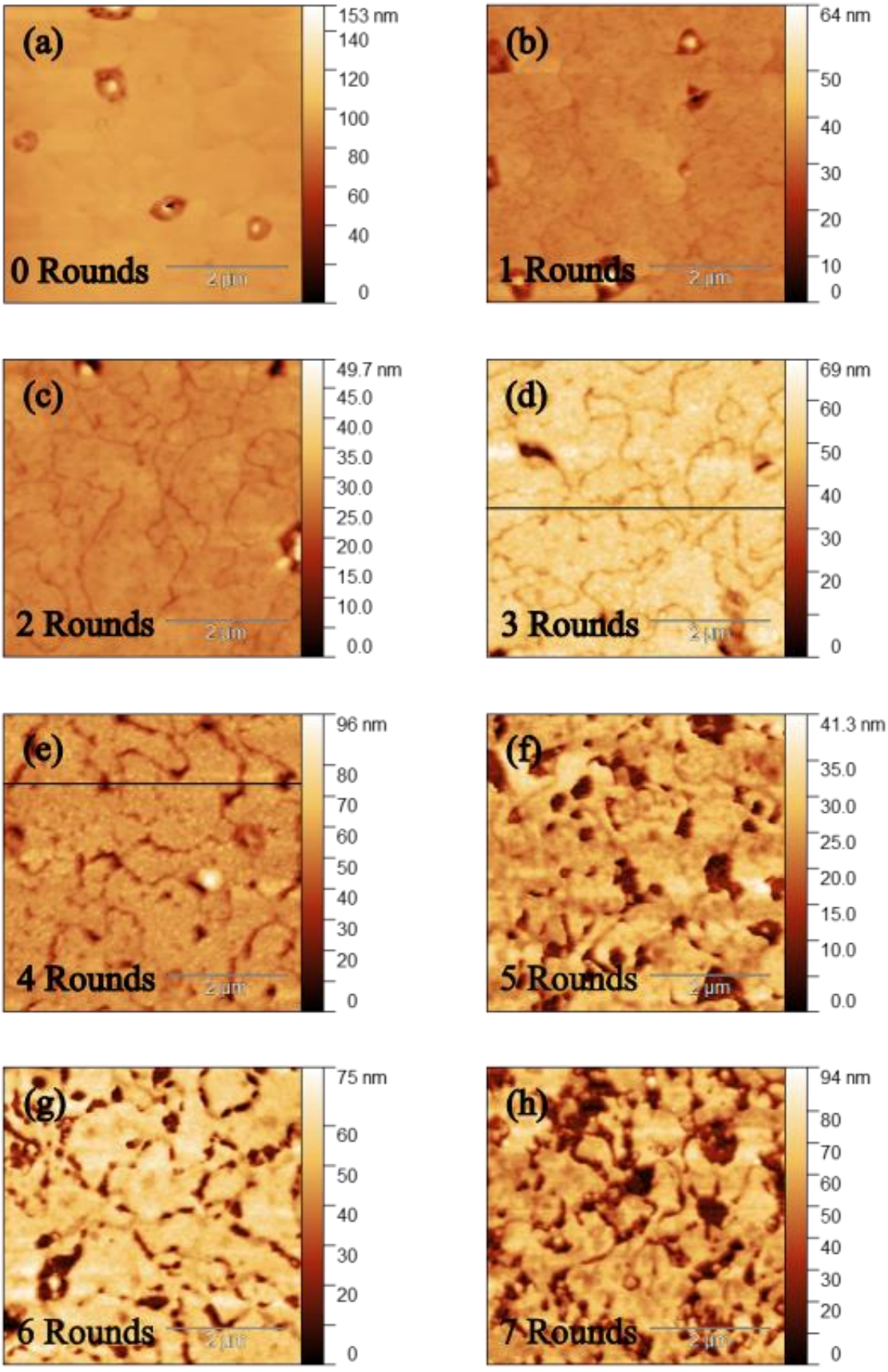

Figure 5.15: 5 µm AFM images of the surface post etch-annealing. (a) An AFM image of the copper surface after an initial anneal and prior to any etching. (b)-(h) AFM images of the surface post each etch round. Here the etch round consists of two stages; An etch followed by a recovery anneal. The lines marked on (d) and (e) indicate where the line profiles of ***Figure 6.3*** *are taken from.*

Roughness comparisons of the sapphire-substrate sample set with the Ta/Si set are shown in ***Figure 5.16(a)***. Not shown on the plot is an RMS roughness comparison of the as-deposited Cu 60 nm film, which has an RMS roughness of 2.9 ± 0.5 nm, to the as-deposited Cu 50 nm film with an RMS roughness of 0.63 ± 0.04 nm. From RMS analysis, both samples show an increase in vertical roughness as etching continues. That being said, the copper on Al_2O_3 samples (grey) shows a far larger increase in roughness compared to that of copper on Ta (7 nm)/Si samples with much wider degrees of variation. In the case of the former, the rougher areas were found to exist in the centre of the samples, while the sample's edges remained smoother. Examples of surface variation can be seen in ***Figure 5.18***

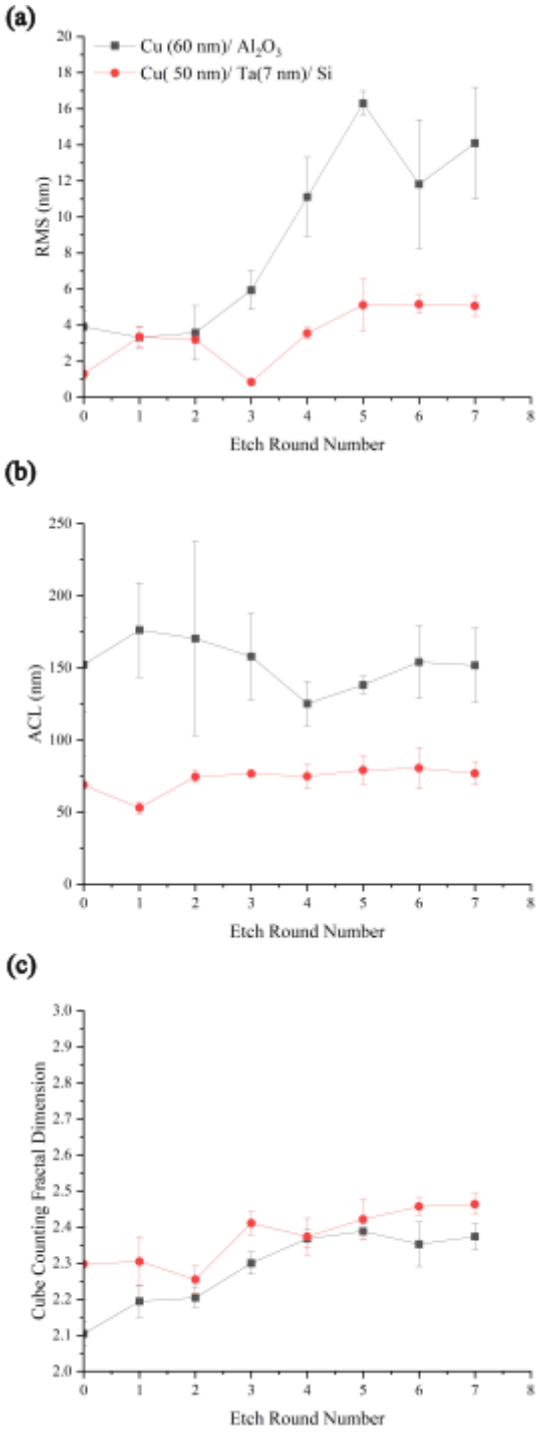

Figure 5.16:Roughness analysis for cyclic acetic acid etch-annealing for Cu 60 nm on Al_2O_3 (grey) and Cu 50 nm on Ta/ Si (red). (a) RMS roughness vs etch round, (b) ACL vs etch round and (c) cube counting fractal dimension vs etch round. Etch round 0 represents an initial anneal without any prior etching. After this point, each etch round consists of two steps; An etch followed and a recovery anneal.

ACL analysis of the Al_2O_3 samples, shown in ***Figure 5.16(b)***, found the Al_2O_3 samples had larger autocorrelation lengths compared to Ta/Si samples. The average grain size of the Al_2O_3 samples is larger than the Si samples. Grain size as a function of the process round was analysed separately and the results are presented in ***Figure 5.17***. After the second anneal (Etch Round 1), the grain size remained somewhat constant. The same trend was seen after the initial anneal of the copper on Ta (7 nm)/ Si samples in ***Figure 5.4***. Since the grains of the Al_2O_3 samples are larger, the ACL, by extension, should also be longer.

Interestingly, instead of showing an increasing value for the ACL, as seen in the copper on Ta (7 nm)/ Si set, the copper on Al_2O_3 samples shows an initial trend towards a decreasing ACL. Overall, however, there is a good correlation between the grain size in ***Figure 5.16(b)*** and the grain size in ***Figure 5.17.***

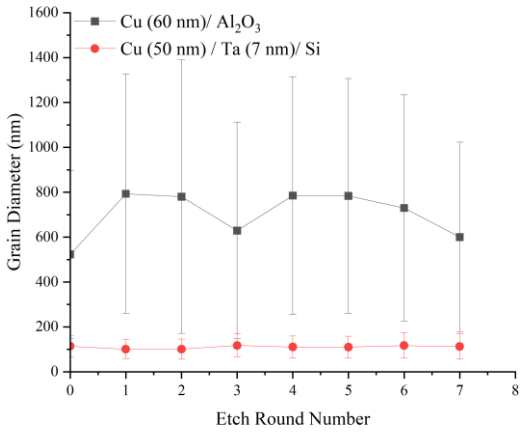

Figure 5.17: Line plot of average grain diameter vs etch round for samples Cu/Ta/Si (red) and Al_2O_3 (grey)

The final metric of comparison is the fractal dimensions shown in ***Figure 5.16(c)***. Unlike the RMS comparison, the fractal dimension sees the initial copper on Al_2O_3 sample as smoother compared to the copper on Ta (7 nm)/ Si. This is likely the influence of the larger grain sizes. Since the grain boundaries in the copper on sapphire samples are spread further apart compared to the copper on silicon sample, the surface of the sapphire sample set appears smoother on average. As the etch anneal process continues, the fractal dimensions of the copper films on Ta (7 nm) Si and Al_2O_3 become closer in value.

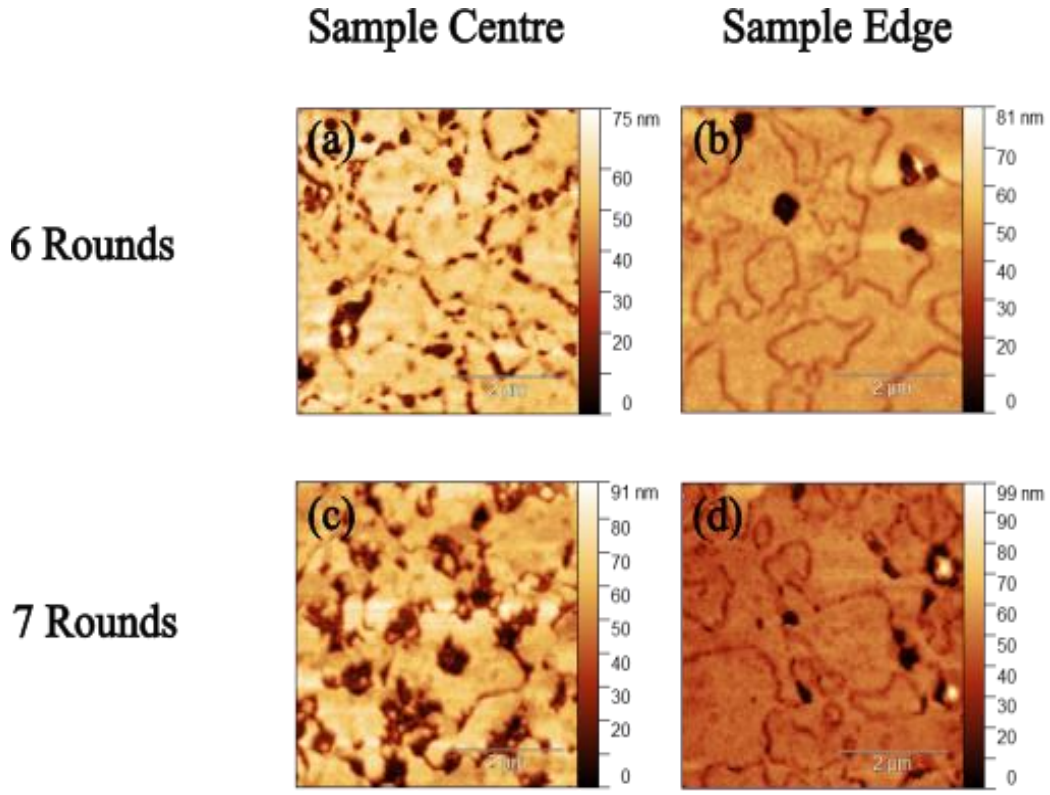

Figure 5.18: 5 µm AFM images of the surface of the Cu/Al_2O_3 post 6 and 6 rounds etch-annealing. The (a) and (c) are taken towards the centre of the sample, while (b) and (d) right are taken near the very edges of the sample.

5.4 STM ON CU-AL_2O_3

To further characterise the nature of the etch and its influence on the grain boundaries, the clean, as deposited copper 60 nm film was studied by STM. For this sample to be viable in STM, the metal film had to be electrically connected to the sample holder as the sapphire substrate is electrically insulating. A top-down view of the connection is provided in ***Figure 5.19***. The aim of using an unetched sample was to first evaluate the grain boundaries seen on the sample and to determine if the grain boundary reconstruction could be

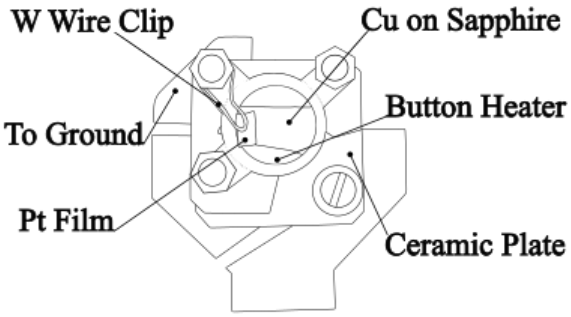

Figure 5.19: A top-down schematic of the sample holder assembly used for the 60 nm copper film deposited onto sapphire. The copper film is connected to the sample holder directly via a tungsten wire. To cushion the connection between the copper film and tungsten wire a small piece of platinum foil is placed between the two. This stops the tungsten wire from scratching away the copper film as the nut securing the wire is tightened. For a side-on schematic of the sample holder, see Figure 2.5.

induced in this sample by argon sputter cleaning and an annealing process. Once the reconstruction has been induced in an as-deposited sample, a sample that has undergone etching can be analysed by STM, using the current sample as a point for comparison.

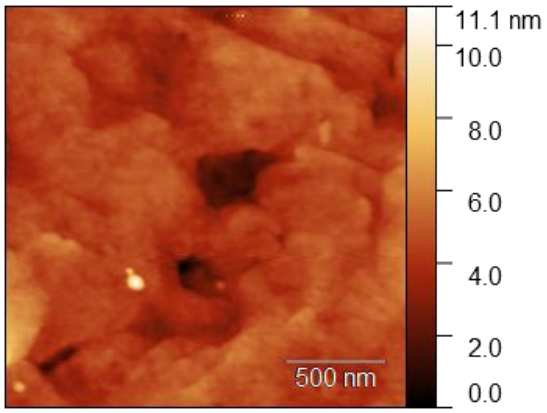

Figure 5.20: 2 μm AFM image of the as-deposited copper on Al_2O_3 surface.

To begin this study, a comparison of the surface by AFM and STM is completed. The closest possible comparison is between 2 μm AFM images and 1 μm STM images, the latter being the largest possible image size using STM. As can be seen from ***Figure 5.20***, the grain boundaries in AFM images do not provide strong contrast, making them difficult to visualise. The roughness parameters measured in ***Figure 5.20*** are ω: 0.787 nm, ξ: 145.11 nm and D_f: 2.168. Although the 1 μm STM images are not capable of imaging multiple grains, it can allow for details of individual boundaries to be resolved. An example image is ***Figure 5.21.*** The average roughness parameters for the STM images are ω: 0.9 ± 0.3 nm, ξ: 32 ± 18 nm and D_f: 2.29 ± 0.05. It is expected that the ACL (ξ) will be smaller for the 1 μm image by nature as the area over which the ACL is measured is smaller. More importantly, the RMS roughness for the STM images is larger than that of the AFM ones, indicating that the AFM tip is not as capable of imaging the regions next to the grain boundaries as the STM tip.

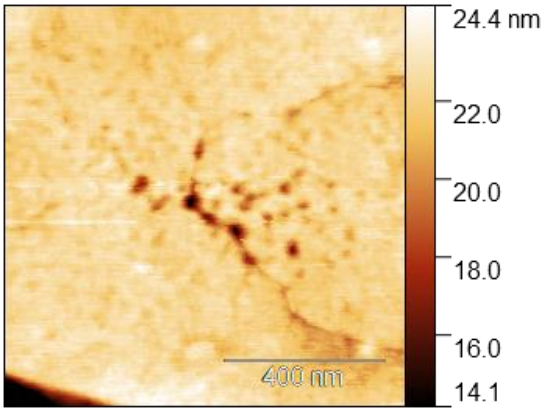

Figure 5.21: 1 μm STM image of as-deposited copper on Al_2O_3. Image taken at 4 V at a setpoint of 0.03 nA

In order to prepare the grain boundaries for STM analysis, the sample is submerged in acetic acid for 30 seconds in order to remove the oxide. After submersion, the sample is transferred into the load lock with a slight N_2 overpressure to minimise the reoxidation of the surface. As can be seen in ***Figure 5.22,*** the grain boundaries vary in depth and width along the surface. ***Figure 5.22(b)*** shows two profiles extracted from the same grain boundary. The grain boundary extends down to depths of 3.00 ± 2.00 nm into the surfaces. In places, it is difficult to identify separate grains from the general surface roughness, as evidenced by the hole feature on the red line profile, which extends beyond the depth the grain boundary appears to. The average width of the valley on the surface is 57 ± 19 nm. Due to adsorbates on the surface, atomic resolution of this boundary was not possible. As a result, there is no confirmation of the extent of the grain boundary valley or if the tip is capable of reaching down to the full depth of the valley.

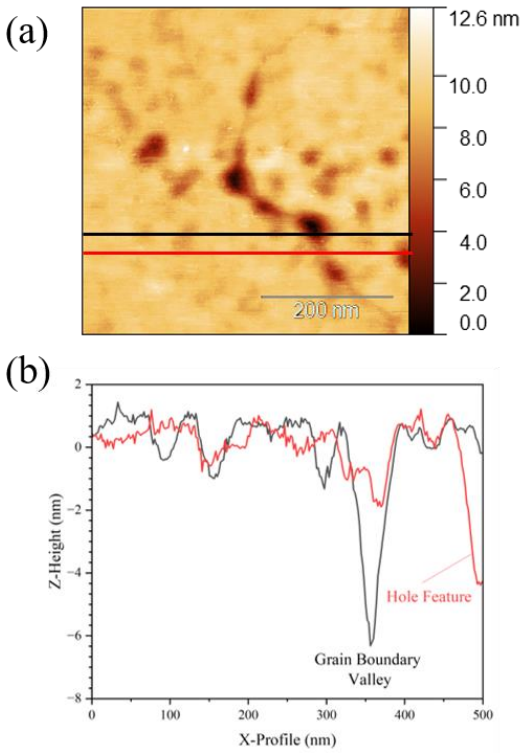

Figure 5.22: (a) 0 0.5 μm STM image of copper post entry into the STM. Image taken at 4 V at a setpoint of 0.03 nA.(b) Line profiles extracted from the grain boundaries.

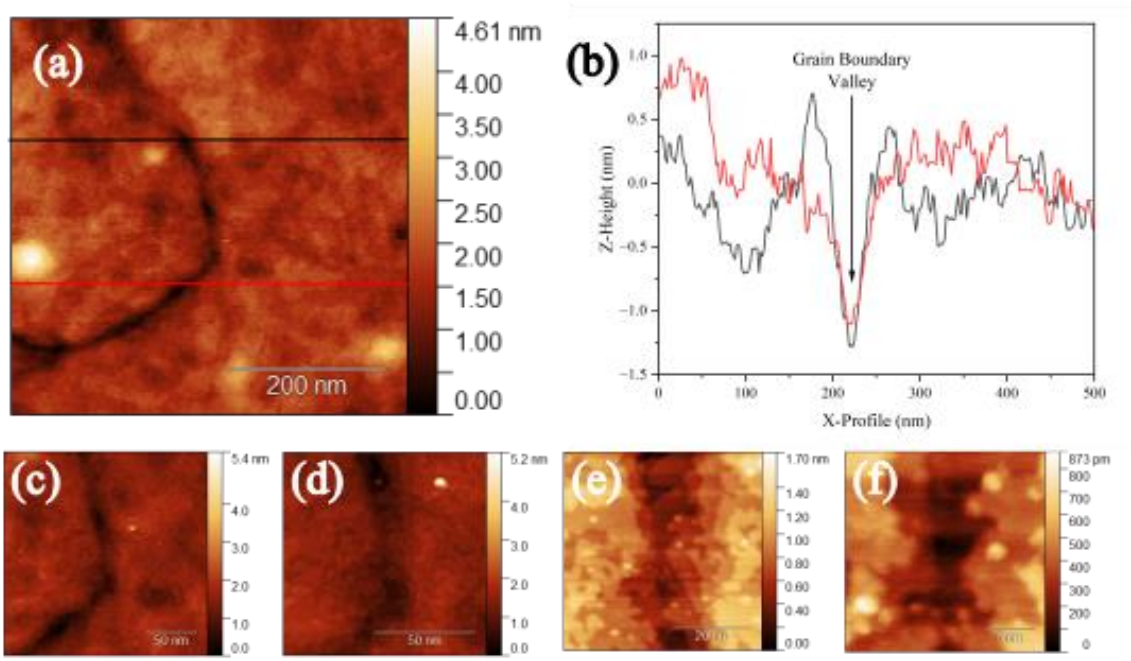

Figure 5.23: (a) 0.5 μm STM image. The black and red lines indicate where the line profiles of (b) were extracted from. (b) Line profiles extracted from (a). The average Z-Height is set to 0 nm. (c) 0.2 μm, (d) 0.1 μm, (e) 50 nm and (f) 20 nm STM images of copper post sputter-annealing. All images taken at 4 V at a setpoint of 0.03 nA.

A sputter-anneal (the details of which were expressed in ***subsection 2.2***) was performed on the sample. The roughness descriptors of the surface post-sputter-anneal are ω: 0.5 ± 0.2 nm, ξ: 38 ± 10 nm and D_F: 2.27 ± 0.07. Compared to the as-deposited surface studies, the sputter annealed surface is smoother for all three descriptors. The grain boundary valleys in the sample post-sputter-annealing have an average depth of 1.1 ± 0.2 nm. Examples of these features are given in ***Figure 5.23(b)***. Compared to that seen in ***Figure 5.22(b)***, the depth of the valley decreases. However, the width of the valley increased to 80 ± 20 nm. As a result of the valley becoming shallower and wider, the tip was capable of probing the boundary sitting at the bottom of the trench.

In ***Figure 5.24***, on either side of the boundary, there are islands of disorder. These islands have a morphology similar to that of Matsumoto et al.[157] In the later stages of copper oxidation, the growth of oxide is disrupted to form irregularly shaped islands. To this end, a single sputter is not enough to clean the sample surface. Further annealing of this surface allows for

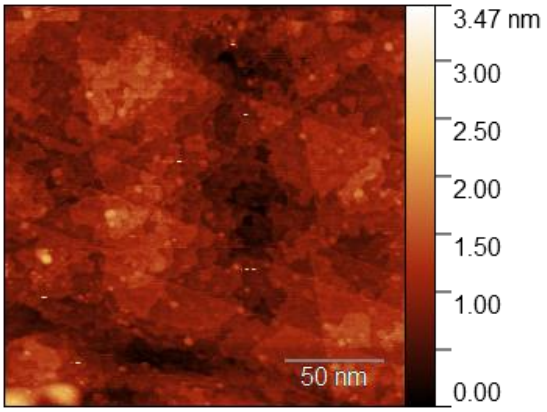

Figure 5.24: 200 nm STM image of a copper on Al_2O_3 sample post sputter annealing with an additional anneal. Image taken at 3 V with a setpoint of 0.03 nA.

the oxide to form triangular structures with edges along the close-packed directions of Cu (111), as seen in ***Figure 5.24***. These structures are seen also in the initial stages of surface oxidation.

After sputter-annealing, a further anneal at 300 °C was completed. Regions surrounding defects began to show the presence of adsorbate-free terraces. Larger scale views of the defect features can be seen in ***Figure 5.15***. These are particularly notable in the 0 Rounds, 1 Rounds and 2 Rounds images of the dataset. An example of the clean terraces next to the features created during the deposition is shown in ***Figure 5.25***. The step edges still have adsorbed material. The average step height measured over these steps is 2.3 ± 0.7 Å. This is very close to the monoatomic step height for copper (111), which is 2.1 Å.

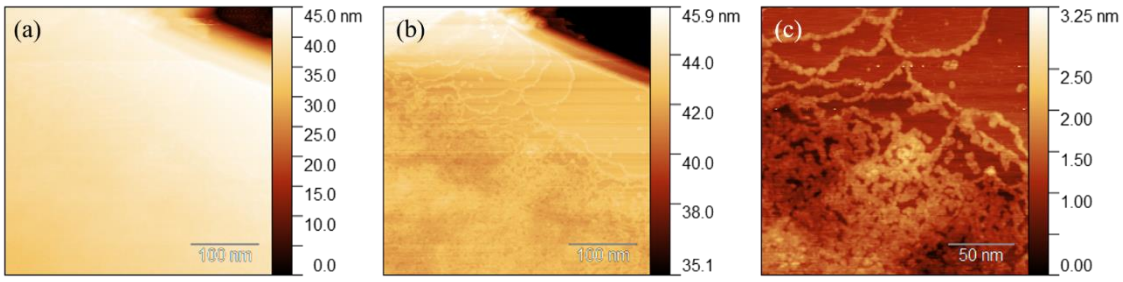

Figure 5.25: (a) 0.5 μm STM image of the surface close to a hole feature caused by the evaporation of a copper crystal seen in the top right corner, (b) The same image as shown in (a) with a reduced z-height colour bar allowing for the cleaner terraces to be seen against the adsorbates further away from the surface depression and (c) 0.2 μm close up of the transition from a partially cleaned copper surface to a surface covered in adsorbates. Images taken at 4 V with a setpoint of 0.03 nA.

A second sputter anneal on the surface removed the remaining adsorbates. Example images of this are shown in ***Figure 5.26***. The resulting surfaces had average roughness parameters of ω: 1.73 ± 1.26 nm, ζ: 67 ± 17 nm and D_F: 2.2 ± 0.1. Compared to the previous process, the second sputter-anneal produces a surface that is much rougher vertically, but the rate of change in height occurs over a much larger distance. Comparison of the as-deposited surface with the sample after two sputter-annealing cycling shows the surface is roughening in terms of the RMS values and becoming smoother according to the autocorrelation length and fractal dimension. Further anneals at lower temperatures may allow the large step densities, as seen in ***Figure 5.26***, to decrease, allowing for a smoother surface to be created.

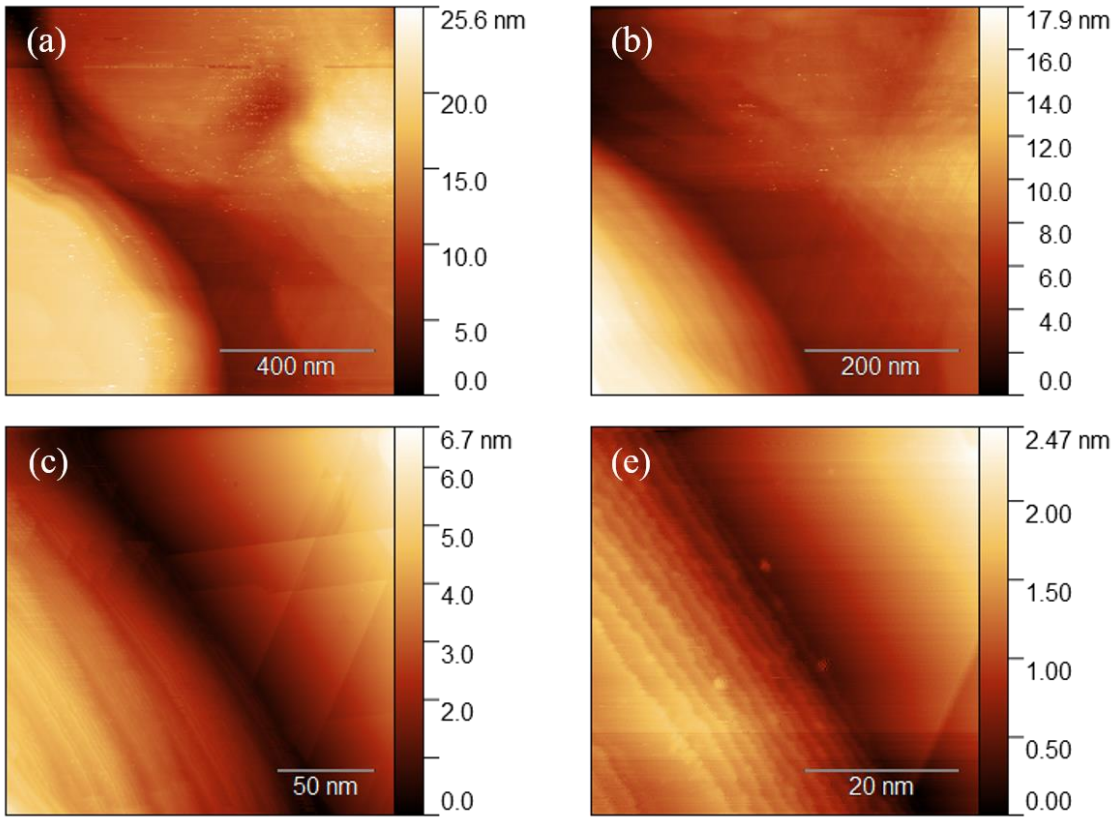

Figure 5.26: (a) 1 µm, (b) 0.5 µm, (c) 0.2 µm and (d) 50 nm of Cu 60 nm on Al_2O_3 post 2 sputter-anneal sessions. Images taken at 2V with a setpoint of 0.03 nA

In conclusion, the as-deposited copper (60 nm) on Al_2O_3 has been successfully cleaned at the expense of increasing sample roughness. As of the writing of this thesis, the sample has an RMS roughness of 1.73 ± 1.26 nm. At this scale of roughness, obtaining atomic resolution at the grain boundary is difficult as several surface states at the side of the boundary interact with the tip, preventing the acquisition of atomic resolution images and an examination of the detailed structure of the boundary. To further this study, low-temperature anneals that decrease the step density at the surface are required. The aim is to produce a sample with a roughness comparable to that quoted by Zhang et al. [12].

5.5 SAMPLE SUMMARIES

The descriptive parameters given in ***Table 5.1*** and ***Table 5.2*** are the key figures that will be used in the subsequent chapter for resistance modelling. The first row of each table gives the descriptive statistics for a sample without any etch or anneal processing completed. The second row is the sample statistics after an anneal without any etching. The following rows are the samples' statistics post etching where each etch round has two stages; the etch itself and a subsequent anneal to recover the surface.

Table 5.1: Key descriptive parameters of the Cu/Ta/Si samples as a function of the etch anneal process. In this table Each etch round consists of two steps, the etching process and a subsequent anneal to decrease surface roughness.

Etch Round Number	Film Thickness (nm)	Grain Diameter (nm)	RMS Roughness (nm)	ACL Roughness (nm)
As Deposited	50	51 ± 20	0.63 ± 0.04	45 ± 2
0	50	114 ± 46	1.3 ± 0.3	69 ± 20
1	46.7 ± 0.3	100 ± 42	3.3 ± 0.6	53 ± 4
2	43.3 ± 0.6	100 ± 44	3.2 ± 0.2	74 ± 5
3	40.1 ± 0.9	117 ± 51	0.84 ± 0.07	77 ± 2
4	37 ± 1	110 ± 48	3.6 ± 0.3	75 ± 8
5	34 ± 2	110 ± 56	5 ± 2	79 ± 10
6	30 ± 2	117 ± 56	5.2 ± 0.5	81 ± 14
7	27 ± 2	112 ± 56	5.1 ± 0.6	77 ± 8

Table 5.2: Key descriptive parameters of the Cu/Al_2O_3 samples as a function of the etch anneal process. In this table Each etch round consists of two steps, the etching process and a subsequent anneal to decrease surface roughness.

Etch Round Number	Film Thickness (nm)	Grain Diameter (nm)	RMS Roughness (nm)	ACL Roughness (nm)
As Deposited	60	398 ± 256	2.9 ± 0.6	121 ± 11
0	60	523 ± 375	3.9 ± 0.9	152 ± 33
1	58.4 ± 0.7	793 ± 533	3.3 ± 0.6	176 ± 33
2	57 ± 1	780 ± 609	4 ± 2	170 ± 67
3	55 ± 2	629 ± 482	6 ± 2	158 ± 30
4	54 ± 3	785 ± 530	11 ± 2	125 ± 15
5	52 ± 4	784 ± 523	16.3 ± 0.7	138 ± 6
6	50 ± 4	730 ± 504	12 ± 4	154 ± 25
7	49 ± 5	600 ± 423	14 ± 3	152 ± 26

One key difference between the two sample sets is grain size. The as-deposited copper film on Al_2O_3 has much larger grains than the copper film deposited on Ta(7 nm)/

Si. This is maintained after etch-anneal processing. However, both samples do experience grain growth, during annealing, as seen in the third columns of both ***Table 5.1*** and ***Table 5.2.*** The grain size increases for the initial anneal of the copper on Ta/Si but is maintained for the etch rounds. Alternatively, the grains of copper on Al_2O_3 increase for the initial anneal and the first etch round before being maintained for the remaining etch rounds.

It is important to note that the standard deviation of the grain diameter in the copper on Al_2O_3 samples is much larger than that for the copper on Ta (7 nm)/ Si samples. From ***Figure 5.15(c)***, the grains in copper on Al_2O_3 do not have a regular shape. By comparison, the grains in copper on Ta/Si, seen in ***Figure 5.3 (b), (d), (f) and (h),*** are more regular in shape and can be modelled as circular. For this study, the grain diameter was determined by extracting line profiles at every micron mark from 2 µm, 5 µm & 10 µm images and counting the number of grains per line profile. This method presents two drawbacks. Firstly, the gains are not regular shapes. Secondly, grains in the copper on Al_2O_3 sample are sufficiently large that the same grain can be counted over several profiles, underestimating grain size. Similarly, the grain may be extremely wide in one direction whilst also being extremely narrow in the orthogonal direction. Since the line profiles are only taken in the x-direction, the grains could be recorded as extremely thin or extremely thick, creating a wider range of grain sizes. This makes measuring changes in grain size more difficult.

The RMS roughness' of the copper on Ta (7 nm)/ Si samples is consistently lower than that of the copper on Al_2O_3. The as-deposited surface of the copper on Al_2O_3 starts with a larger roughness. However, as the etch process develops, the increase in roughness is much more pronounced for the copper on Al_2O_3 compared to the copper on Ta (7 nm)/ Si. This difference is a result of the difference in grain size. As oxidation happens preferentially at grain boundaries and surrounding areas, when grain boundaries are closer together, the variation in height across the surface is much smaller compared to surfaces where the grain boundaries are separated by more significant distances.

A difference in values also emerges in the autocorrelation lengths (ACL) for both sample sets. The autocorrelation lengths for both samples are below their respective grain diameters. That being said, the autocorrelation length for the copper on Ta (7 nm)/ Si values are far closer to the grain diameter values than that expressed for the copper on Al_2O_3. The difference could be the result of the larger pit features that are present on the surface of the

copper on Al_2O_3, as seen in ***Figure 5.11(a)***. Alternatively, the difference could also be the result of grain shape alongside the method used to determine the average grain diameter.

6 RESISTANCE AND RESISTIVITY MEASUREMENTS

As stated previously, the size effect is the term given to the increase in resistivity of metallic conductors as their dimensions decrease. Many size effect models are founded on the Boltzmann transport equation (BTE). The BTE is a semi-classical equation that describes the time-dependent position and momentum of electrons, or holes, in a material in terms of a distribution function f(r,v,t), where r is position and v is the momentum and t represents time. Quantum size effects due to the breakdown of band structure are not relevant here, given the dimensions of the films studied in this thesis. We now consider models of transport that consider the role of different types of interfacial film defects.

6.1 THE FUCHS-SONDHEIMER MODEL

The predominant resistance mechanism in bulk conductors is the scattering of conduction electrons by phonons. That being said, other resistivity mechanisms may also be present. These include electron scattering from residual impurities, point defects, line defects, planar defects or from the conductor's external surfaces. These, however, are considered secondary due to their typically negligible contribution to resistivity [32].

When the smallest dimension of a bulk conductor is reduced to the order of the electron mean free path, a significant percentage of its atoms are present at the external surface. This means that as the material's dimensions decrease, the once insignificant contribution of surface scattering now has a pivotal effect on its resistance. Fuchs[29] first introduced the concept of surface scattering in 1938 to explain the size effect when analysing thin metallic films.

The Fuchs model of surface scattering is derived from the Boltzmann transport equation in which the electron has a limited mean free path due to interactions with phonons. The Fuchs model expands on Boltzmann transport by including a specularity coefficient, p, which describes the fraction of electrons that are specularly scattered at the film's surface. When an electron is specularly scattered, its velocity perpendicular to the film surface is reversed in sign while its drift velocity is conserved. The remaining fraction of the scattered electrons scatter diffusively. In this scenario, electrons lose their drift velocity. The important length scales in the Fuchs model are the thickness of the film and the mean free path of the conduction electrons due to phonon and impurity scattering. The Fuchs model describes the resistivity of a thin film as[158];

$$\rho_{Fuchs} = \rho_i \left[1 - \left(\frac{3}{2\kappa}\right)(1-p)\int_1^{\infty}\left(\frac{1}{t^3} - \frac{1}{t^5}\right)\frac{1-\exp(-\kappa t)}{1-p\exp(-\kappa t)}dt\right]^{-1} \qquad 6.1$$

Here, $\kappa = h/\lambda$ and ρ_i is the bulk resistivity of the metal. For the limiting case of a small κ, ***Equation 6.1*** simplifies to [158]

$$\rho_{Fuchs} = \rho_i \left[1 + \left(\frac{3}{8}\right)\frac{\lambda}{h}(1-p)\right] \qquad 6.2$$

This equation is often used for the empirical analysis of resistivity versus thickness data. The resistivity increase over bulk resistivity that is predicted by Fuchs' model can be written as [158];

$$\Delta\rho_{Fuchs} = \rho_{Fuchs} - \rho_i \qquad 6.3$$

6.2 MAYADAS AND SHATZKES MODEL

The next level of complexity is a model developed by Mayadas and Shatzkes[159], [160] which is also an extension of the Boltzmann transport theory. The MS model accounts for the reflection and transmission of conduction electrons at the grain boundaries in polycrystalline conductors in addition to surface scattering. The MS model assumes that the grain boundaries in a thin film are oriented either parallel or perpendicular to the direction of the current flow. Electrons incident on the parallel grain boundaries are specularly reflected and, therefore, do not contribute to the resistivity size effect. However, grain boundaries that are perpendicular to the current flow are treated as internal surfaces. When a conduction electron collides with one of these grain boundaries, the electron can either be reflected or transmitted. The probability of reflection or transmission is quantified by a reflection coefficient, R. The reflection coefficient can take a value between 0 and 1. The reflection coefficient is usually fitted to experimental data. [158]

The important parameters for this model are the average, or in our case, the mean grain size, g, and the electron mean free path, λ. The reflection coefficient is usually combined with the grain size and electron mean free path to form a singular parameter, α. Where $\alpha = (\lambda/g)\, R/1-R$. The MS model describes the resistivity of a film as [158]

$$\rho_{MS} = \rho_i \left[1 - \frac{3}{2}\alpha + 3\alpha^2 - 3\alpha^3 ln\left(1 + \frac{1}{\alpha}\right)\right]^{-1} \qquad 6.4$$

For the limit of a small α value, ***Equation 6.4*** reduces to

$$\rho_{MS} = \rho_i \left[1 + \left(\frac{3}{2}\right)\left(\frac{\lambda}{g}\right)\left(\frac{R}{1-R}\right)\right] \quad 6.5$$

Using this model, the increase in resistivity due to grain boundary scattering is

$$\Delta\rho_{MS} = \rho_{MS} - \rho_i \quad 6.6$$

As can be seen, ***Equation 6.3*** and ***Equation 6.6*** have similar forms. In polycrystalline films, the effects of grain size and film thickness tend to be nearly equal or at least proportional. As a result, the resistance increase associated with the classical size effect in polycrystalline conductors can frequently be attributed to either scattering process or a combination of the two. The similarity in functional dependence has confounded much of the published work on resistivity size effects in polycrystalline thin films [158]

6.3 MATTHIESSEN'S RULE

One additional issue which must be considered for the quantitative modelling of the resistivity size effect is the applicability of Matthiessen's rule. Impurity, phonon, grain boundary and surface scattering are often included in resistivity modelling by Matthiessen's rule. Matthiessen's rule requires a simple addition of a constant surface or constant grain boundary resistivity contribution with the phonon contribution to provide a total resistivity [161]

Matthiessen's rule cannot be used to combine the resistivity contributions of the surface and phonon scattering as there is a significant interaction between the two mechanisms. A majority of the electrons which contribute strongly to the electrical current with isotropic scattering are those that have small values of z-axis momentum for an electric field oriented along the x-axis in the plane of the film. At temperatures where there is little to no phonon scattering, these electrons are relatively unaffected by surface scattering. When the temperature increases, increasing phonon scattering allows these electrons to be more frequently redirected to the surfaces, resulting in an increase in the surface scattering as phonon scattering increases. Meanwhile, in grain boundary scattering, the electrons with a low z-axis momentum that is responsible for the current flow are unable to avoid collisions at grain boundaries. As a result, phonon scattering, and thus temperature, has a small effect on this contribution to the film resistivity [161].

Since Matthiessen's rule is invalid for the combination of surface and phonon scattering, can it be valid for the combination of surface and grain boundary scattering? At low temperatures, there is an expected interaction between surface scattering and grain boundary scattering, as grain boundaries may serve to scatter electrons with momentum parallel to the externally applied field towards the surfaces, much like phonon scattering. This expectation assumes that the electrons reflected by the boundaries undergo diffuse scattering. Mayadas and Shatzkes account for this type of interaction in a model that combines the scattering effects of grain boundaries, external surfaces, and phonons in polycrystalline metallic films. This is referred to as the Mayadas-Shatzkes Surface model [161].

However, it is more common to assume that the surface and grain boundary mechanisms are independent. In this case, Matthiessen's rule can be applied. A combined model can be written as[161] ;

$$\rho_{Fuchs+MS} = \rho_i + \Delta\rho_{Fuchs} + \Delta\rho_{MS} \tag{6.7}$$

$$\rho_{Fuchs+MS} = \rho_i + \left(\frac{3}{8}\right)\frac{\lambda\rho_i}{h}(1-p) + \left(\frac{3}{2}\right)\left(\frac{\lambda\rho_i}{g}\right)\left(\frac{R}{1-R}\right) \tag{6.8}$$

This equation includes the strong interaction between phonon and surface scattering as well as the weaker interaction between grain boundary scattering and phonon scattering. [161]

6.4 Correction Factors for Cu (50 nm)/ Ta (7 nm)/ Si (100) & Cu (60 nm)/ AL_2O_3 (0001)

Real specimens are not infinite in either the vertical or the lateral direction. As such, sample geometry must be accounted for when determining sheet resistance. As such, correction factors are required to account for the influence of the sample boundaries. In the case of finite and arbitrarily shaped samples, the bulk resistivity is expressed as;

$$\rho = F\frac{\pi h}{ln2}\frac{V}{I} \qquad 6.9$$

F can separated into three separate geometric correction factors F_1, F_2 and F_3. F_1 accounts for the sample's thickness, F_2 accounts for the alignment of the probes in the proximity of a sample's edges, and F_3 accounts for the finite lateral width of the sample.

For both Cu (50 nm)/ Ta (7 nm)/ Si (100) & Cu (60 nm)/ AL_2O_3 (0001), the thickness of the conductive films (h) is in nanometres compared to the separation between the probes (s) which is 2.0 ± 0.5 mm. Incorporating these values into ***Equation 2.32*** gives a correction factor F_1 of 1. Likewise, the samples have an edge length (d) of 2 cm ± 0.1 cm, which, when incorporated into ***Equation 2.36***, provides an F_2 value of 1.0013. The final geometric correction factor, accounting for the lateral width of the samples, is more complicated to calculate. As such, the value of F_3 is taken from the Haldor Topsøe geometric factors in four-point resistivity measurement[98]. For the sample geometries under study here, F_3 is identified as 0.9319. Combing all three correction factors via the equation $F = F_1F_2F_3$ gives a value of F equal to 0.9325. This value is applied to all measured data for copper films on silicon samples and the sapphire substrates.

6.5 RESISTIVITY OF CU (50 NM)/TA (7 NM)/ SI (100)

The resistivity of the Cu (50 nm)/Ta (7 nm)/ Si (100) samples were plotted against etch round and shown in ***Figure 6.1(a)***. Between the As-Deposited and Round 0 data points, there is no etch process. However, there is an initial anneal. After Round 0, there is an etch between each processing point. From Round 0 to Round 3, the thickness of the film drops from 50 nm to 39.8 ± 0.3 nm. The change in thickness does not induce any change in the measured resistivity of the sample. Likewise, the resistivity of the copper film is far below what is expected for the intrinsic resistivity of copper. The low resistivity and invariance to processing found in this sample could be attributed to the tantalum and doped silicon substrate. Electrons that approach the Cu-Ta interface can scatter into delocalised states in the conductive adhesion layer. The intrinsic resistivity of tantalum varies between 20 μΩ cm to 200 μΩ cm depending on tantalum's structure[162]. With a narrow film of high resistivity, such as tantalum, electrons are likely to scatter back into the copper layer as a diffuse scattering event. This would lead to an increase in copper resistivity, provided it was the only available path. As such, an alternative path for electron conduction would have to exist. One potential pathway could be that the thickness of the tantalum is insufficient to deter electrons from moving into the doped silicon. The electron mean free path of tantalum has been measured experimentally to be 28 ± 1 nm[163]. If the mean free path of tantalum is approximately 28 nm, then the 7 nm thick could be insufficient to stop electrons from moving through the tantalum into the doped silicon. Therefore, electrons move from the injection site, through the Ta layer and into the doped Si. The doped Si is thick enough to allow both the influence

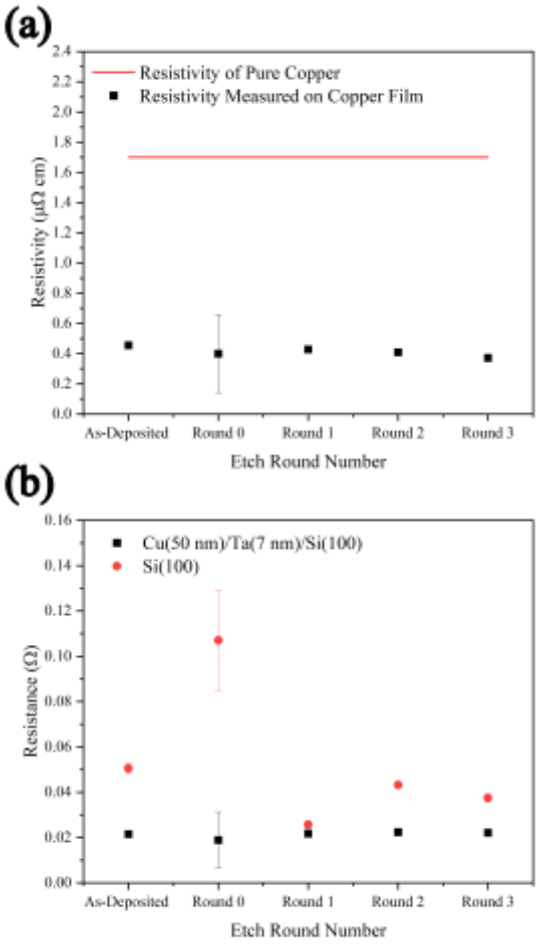

Figure 6.1: (a) Calculated resistivity taken from Cu (50 nm)/Ta (7 nm)/ Si (100) samples at different processing points.(b) Sheet resistance comparison of the samples with and without the 50 nm copper film and 7 nm thick adhesion layer.

of the surface scattering and grain boundary scattering contributions to become negligible. This could explain why the sample does not show any noticeable change in resistivity despite the variation of the thickness and the grain size via an etch-annealing process. To confirm the presence of the second pathway, a comparison of the sheet resistance with and without the copper film and tantalum adhesion layer was completed and is shown in ***Figure 6.1(b)***. Without the conducting films, the sheet resistance increases. However, the silicon is still capable of conducting without the copper thin film or adhesion thin film. This result provides evidence that a leakage current is capable of moving through the doped silicon.

That being said, when a metal is deposited onto a semiconductor, one of two types of contact can occur. These are Schottky or ohmic contacts. If a Schottky contact is created, an energy barrier will be created. As a result, the contact has an asymmetrical IV characteristic depending on the polarity of the applied bias. Both tantalum and copper have shown evidence of producing Schottky barriers[164], [165] when deposited on silicon. Alternatively, if an ohmic contact is formed, the voltage drop across the metal-semiconductor interface is negligible compared to that of the bulk semiconductor.

In our samples, the semiconductor used is a heavily doped, p-type silicon. When a metal contacts a p-type semiconductor, electrons flow from the metal into the empty states in the valence band. This results in the upward curvature of the Si bands such that the chemical potential of the semiconductor comes into equilibrium with the metal Fermi level. When an equilibrium is reached, there is a region which has been depleted of holes. As a result, there is a barrier for holes to reach the interface with the metal and recombine with an electron there. The height of the Schottky barrier for a metal/ p-type semiconductor interface can be calculated by;

$$\phi_{Bp} = \frac{E_g}{q} - (\phi_m - \chi_s) \qquad 6.10$$

Where E_g is the energy band gap, q is the electronic charge, ϕ_m is the metal work function and χ_s is the electron affinity of the semiconductor. As can be seen from ***Equation* 6.10,** the degree and polarity of the applied bias, as well as the degree of doping, have no effect on the barrier height.

Rather, these properties affect the width of the depletion layer formed by the Schottky barrier. The exact width of the barrier can be determined via;

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi} - V_a)}{qN}} \qquad 6.11$$

Here, $\varepsilon_s$is the dielectric constant of the semiconductor, V_{bi} is the contact potential V_a is the applied bias, and N is the dopant density. For a metal/p-type Schottky barrier, when the metal is the negative terminal (Forward bias), holes are attracted to the metal-semiconductor interface. This results in a reduced width depletion region, allowing current to pass. The opposite situation occurs when the metal is the positive terminal (Reverse bias).

Similarly, ***Equation 6.11*** shows that the degree of doping in a semiconductor has an inverse relationship with the barrier width. When the doping density is sufficiently high, the semiconductor can become degenerate. If the semiconductor is degenerate, the semiconductor behaves more like a metal as the barrier width is thin enough to be dominated by tunnelling processes. The exact details of the doped Si used by Intel in the production of these samples were not disclosed. However, the samples were produced with the intent to be studied under STM, where the requirement for samples to be sufficiently conductive to allow tunnelling between the tip and sample is well known.

Another possibility for the unusual conductivity in the copper on tantalum on silicon samples could be due to copper coming into direct contact with the underlying silicon in certain regions. This would create a competing pathway for electron injection into the silicon. There are two ways this situation could occur; firstly, if the tantalum adhesion layer is discontinuous, the copper would be in direct contact with silicon in regions of the sample. As of writing this thesis, no etch method has managed to completely remove the copper film and leave the tantalum layer intact. For this reason, the state of the deposited tantalum has not been evaluated. Alternatively, copper is capable of diffusing through tantalum at elevated temperatures. Further analysis would be required to determine if the copper is diffusing into the tantalum as a result of the annealing processes. This would require further studies using secondary ion mass spectroscopy[166], [167].

6.6 RESISTIVITY OF CU (60 NM)/ AL_2O_3 (0001)

The average sheet resistance of the Cu 60 nm on sapphire films plotted as a function of the etch anneal process is shown in ***Figure 6.2(a)***. As-Deposited represents the as-deposited film. Round 0 is an anneal round with no etching to prepare the surface. After Round 0, the sample is etched and then annealed again. This is the data point Round 1. As the etch-anneal progresses (Round 0 to Round 7), the sheet resistance increases. Immediately obvious from the AFM images shown earlier in ***Figure 5.15***, the etch-anneal process removes material from the film in such a way as to create holes. These holes mean the film is no longer continuous, and resistance will increase. Similar effects are seen during the dewetting[168] or electromigration damage[169] of thin films. In order to apply any resistance model to the data, the effects of the holes on the sample's resistance must first be addressed. To determine at which point the film becomes discontinuous, the fraction of exposed substrate in AFM images is plotted as a function of the etch-anneal process. The fraction of the sapphire substrate that was exposed due to hole formation was determined via pixel analysis of the AFM images using imageJ[170]. The result of

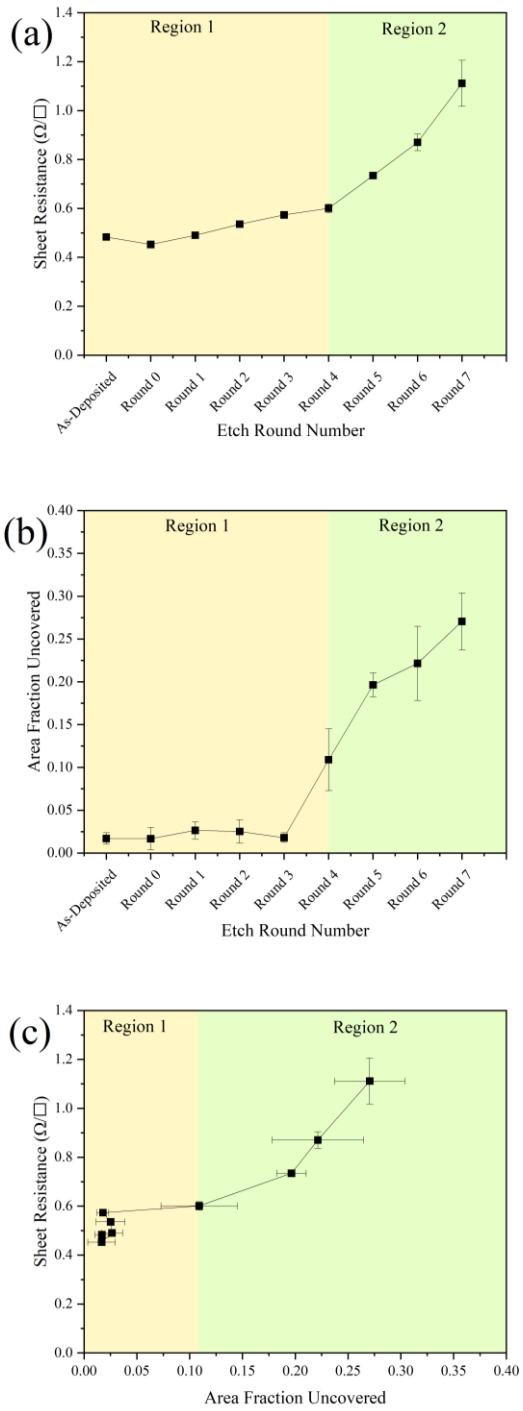

Figure 6.2: (a) Sheet resistance measurements taken from samples made in duplicate taken at different processing points. The sheet resistance values are split between two regions. Region I (yellow) represents the processing points where the film is continuous. Meanwhile, Region II (green) represents the processing points where the film is discontinuous. (b) The discontinuity of the film was determined by measuring the fraction of substrate visible in the AFM images taken at different processing points. At Round 5 the fraction of exposed substrate increases, indicating the film is no longer continuous (c) Sheet resistance plotted as a function of area of exposed sapphire in AFM images.

this analysis is shown in ***Figure 6.2(b)***. From the as-deposited film to Round 3, the fraction area of exposed sapphire appears constant with a mean of 0.021 ± 0.005. This small fraction of exposed substrate comes from hole defects present from the deposition process. After Round 3, the fraction of uncovered substrate increases with each round of processing. This increase in the fraction of exposed substrate comes from the etching away of material at the grain boundaries that have reached the substrate, creating holes. Evidence of this can be seen visually in ***Figure 5.15.*** Additionally, a line profile from ***Figure 5.15*** (d) and (e) have been extracted as ***Figure 6.3.*** The Round 3 sample shows notable etching at the boundaries; however, there is no AFM data to suggest that the boundaries have been completely etched away, exposing the substrate. Alternatively, as can be seen in the Round 4 sample (***Figure 6.3(b)***), there is evidence that grain boundaries have etched down to the sapphire substrate, creating a discontinuous film.

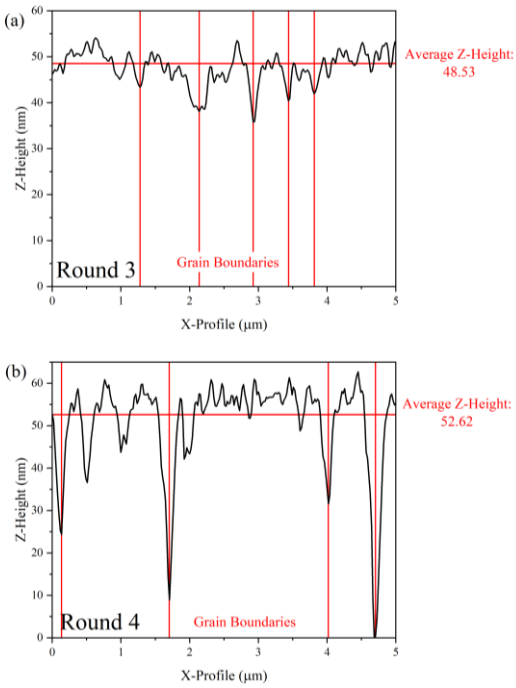

Figure 6.3: Line profiles extracted from (a) ***Figure 5.15 (d)*** *and (b)* ***Figure 5.15 (e)*** *as can be seen, one of the grain boundaries in the Round 4 line profile extends through the full depth of the film. This is evidence that by 4 rounds of the etch-anneal process, the film has become discontinuous.*

To test for a correlation between sheet resistance and the area fraction uncovered, the two are plotted against one another and are shown in ***Figure 6.2(c)***. In the early stages, the fraction of the film area occupied by holes is fixed while the resistance increases. The change in sheet resistance is, therefore, caused by something other than the hole features and is attributed to the reduction in thickness and damage to the grain boundaries due to the process steps. When the fraction of the film occupied by holes increases from the initial value of around 2%, then there is an exponential increase in the resistance. Therefore, measurements at the 4th etch process and above are influenced by the growing presence of the holes in the film. To simplify the model, Round 5 to Round 7 are not included in the modelling of the sample's sheet resistance using Fuchs-Sondheimer or Mayadas-Shatzkes. An important corollary to this is that any resistivity analysis of the film based on the initial

data where the hole fraction was fixed will necessarily yield an increased resistivity over that of the pure metal due to the presence of the holes in the film.

When applying a model to sheet resistance data, the intrinsic resistivity of copper (ρ_i) is taken to be 1.72 μΩ cm, and the mean free path of copper (λ)[32] is given as 39 nm ($3.9x10^{-6}$ cm). These are the values of intrinsic resistivity and mean free path for pure copper at room temperature (21 °C)[32]. As such, the influence of impurities on the film resistivity is not accounted for in these models. Note the sample thickness (h), average grain diameter (g), RMS roughness (ω) and ACL (ζ) are each determined using the AFM data from the respective samples. As such, these parameters are not considered variables for the models.

In thin film studies, typically the grain size and thickness are varied independently of one another to study the individual effects each variable has on the resistivity of a film. Unfortunately, for our process, both the sample thickness and the grain size are altered simultaneously. As such, detangling the independent influence of the grain boundaries and the surface is rather difficult. The copper samples used in these studies have grain sizes starting at 398 ± 255 nm. After several etch-anneal cycles, the grain size increases to an average of 785 ± 523 nm. If the reflection coefficients of the grain boundaries are low ($R \leq 30\%$.), then resistivity due to grain boundary scattering should be low, leading to a negligible resistivity contribution from grain boundaries[31]. On the other hand, the thickness of these films varies between 58 ± 5 nm and 47 ± 12 nm. These values are much closer to the mean free path of copper at room temperature. As such, surface scattering is likely to be a major contributor to the measured resistance of these thin films.

To test this, the resistivity of the samples, determined from resistance measurements versus the sample thickness, is compared to the Fuchs-Sondheimer (FS) model for surface scattering. The initial value at 58 nm corresponds to the resistivity measured after the sample had its initial anneal, while the value at 51 nm is the resistivity measured after 4 etch rounds. Irrespective of the value used for the specularity coefficient (p), the sample resistivity was still significantly higher than that predicted by the model.

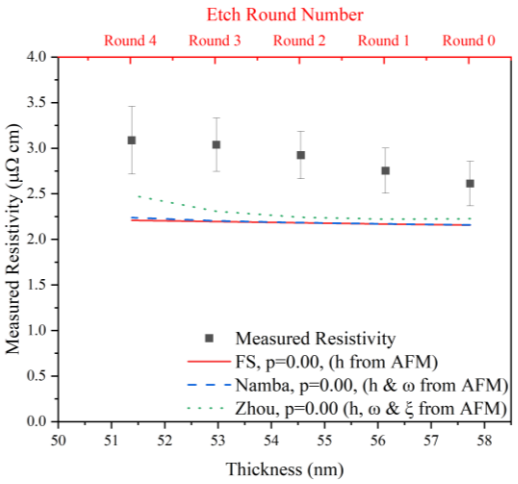

Figure 6.4: The measured resistivity of the Cu 60 nm on Al_2O_3 (squares) Vs thickness compared to the modelled resistivity based on the Fuchs-Sondheimer model (Red solid line), Namba model (Blue dashed line) and the Zhou model (Green dotted line).

As an example, the modelled resistivity of the sample using the FS equation in which all scattering events are assumed to be diffusive (p=0.00) is represented by the red, continuous line in ***Figure 6.4.*** Even at its largest contribution to resistivity, the FS model is unable to account for the total resistivity measured in the 60 nm of copper on Al_2O_3 samples. This result implies that there are other scattering sources at play, causing an increase in resistivity. Potential sources include grain boundary scattering, impurity scattering or point defect scattering. Since the values of mean free path and intrinsic resistivity used in this model are those of pure copper, there is no accounting for the presence of impurities within the film. Dilute impurities often increase resistivity per unit of impurity level[171]. For comparison, Lim et al. [172] evaluated the effect impurities had on the resistivity of copper films at varying thicknesses (5 – 1000 nm). In their analysis, films containing 0.0697% impurities could have an additional resistivity of up to approximately 0.54 μΩ cm from bulk.

The resistance of copper thin films has also been found to vary with exposure to oxygen.[173] Oxygen affects the copper film in two ways. Firstly, adsorbed oxygen on a smooth, clean copper surface disturbs the flat surface potential, causing the surface scattering to become diffuse[174], [175], [176], [177], [178]. This leads to a specularity coefficient of 0.00. The four-point probe analyses in this study were completed in air. As such, the formation of a copper oxide layer on the samples would have certainly occurred,

lending justification for the specularity coefficient to be maintained at 0.00. Secondly, the creation of an oxide layer on the film's surface causes atomic scale roughness on the copper surface while simultaneously consuming copper. This reduces the thickness of metallic copper film[7]. This decrease in the copper thickness was not accounted for in this modelling. As such, it could be partially responsible for the difference between the measured and modelled resistivity.

The current experimental model also ignores the role that the film-substrate interface plays in electron scattering. Since Al_2O_3 is an insulator, it has a negligible density of states at the Fermi level.[8], [175], [178] This means the copper electrons have no interfacial states to scatter into, promoting specular scattering events and providing higher copper conductivity. In order to determine the contribution from the Al_2O_3: Cu interface and the Cu: Air interface, the contributions of the two must be modelled separately. However, the thickness and roughness of the etched film make XRR analysis on the Cu on Al_2O_3 impossible.

6.7 ROUGHNESS DEPENDENCE OF ELECTRICAL RESISTIVITY

A drawback of the FS model is the fact it does not explicitly account for the role of surface roughness in surface scattering. The FS model treats the two interfaces of a thin film as completely flat and separated by a constant distance, h, with the effect of roughness assumed to be accounted for by the phenomenological specularity parameter (p), which varies from 0 to 1. For thin films that are 20 nm or thinner[7], [28], [179], surface roughness introduces variations in height that are a considerable proportion of the film's total thickness. This variation in thickness is not accounted for by the FS model, which leads to underestimations of the film's resistivity.

Multiple extensions to the Fuchs-Sondheimer model of surface scattering have been developed to include surface roughness as a contributor to resistivity[7], [28], [171]. One such example is the Namba[180] model. Namba modelled the resistivity increase resulting from the variation of film thickness as a result of surface roughness. As shown in previous chapters, this variation in the height of a surface is quantified by the RMS roughness (ω). The Namba model, therefore, expresses the change in thickness in terms of RMS roughness by the equation;

$$\rho_{Surface} = \rho_{FS} + \frac{3}{8}(1-p)\frac{\lambda\rho_i}{h}\frac{\omega^2}{h^2} \quad 6.12$$

Here, ρ_{FS} is the resistivity that results from a perfectly flat film given by FS. The effect of varying thickness is given by the second term in ***Equation 6.12.*** In this equation, roughness is treated as a secondary effect of the increase in resistivity due to decreasing thickness. As a result of this assumption, the Namba model often underestimates the resistivity increase seen in thin films[28].

A second approach to modelling roughness was developed by Zhou et al. [181]. In Zhou's model, surface roughness is visualised as a series of atomic height surface steps which cause discrete local scattering events. Each scattering event can increase resistivity. Between the steps are flat terraces, which can be treated as flat films. As a result, the total resistivity of a film is expressed by a sum of the flat film resistivity given by the FS model and a term that accounts for resistivity from scattering at steps. To make this model applicable to experimental data, Zhou expressed variation in surface height and the distance over which it occurs in terms of the RMS roughness (ω) and the autocorrelation length (ξ). Zhou's model is written as;

$$\rho_{Surface} = \rho_{FS} - \frac{3}{8}\frac{\lambda\rho_i}{h}\Delta\rho \quad 6.13$$

where

$$\Delta\rho = -4\sqrt{\frac{3}{2}}\frac{\omega}{\xi} \quad 6.14$$

Both the Namba model and the Zhou model of the sample resistivity were compared to the resistivity versus thickness data. The results of this comparison are plotted in ***Figure 6.4***, where the blue dashed line is the Namba model, and the green dotted line is Zhou's model. Like the FS model, both Namba and Zhou's models are closest to the experimental data when scattering at the surface is considered 100% diffuse. Neither model is capable of accounting for the total resistivity measured in the 60 nm copper on Al_2O_3 samples. That being said, Zhou's model shows a higher value of resistivity at each thickness compared to the other two models. The Zhou model also has a steeper increase in resistivity at the 53 nm mark, corresponding to the large increase in RMS roughness observed at this thickness, as seen in ***Figure 5.16***.

Comparison of each model with the experimental data as a function of processing step is shown in ***Figure 6.5***. In the experimental data, there is a decrease in resistivity as a result of annealing the as-deposited film (As-Deposited to Round 0). Annealing has two effects. Firstly, it promotes grain growth within the sample. Secondly, as seen in ***Figure 5.16***, annealing alters surface roughness. Comparison of the ratio of RMS roughness to the ACL length for the as-deposited film and the annealed film shows very little difference, with 0.024 for the as-deposited film and 0.026 for the annealed film. When the RMS roughness and autocorrelation length values provided in ***Table 5.2*** are input into the Zhou model using ***Equation 6.13,*** the modelled resistivities are 2.22 μΩ cm for the as-deposited film and 2.23 μΩ cm for the same film after the initial anneal (Round 0). The difference between these two values is negligible compared to the measured resistivities of 2.79 μΩ cm for the as-deposited film and 2.61 μΩ cm after the initial anneal. As a result, the decrease in resistivity is not entirely accounted for by a change in the surface roughness. This provides some support for the influence of grain boundaries on the film's resistivity.

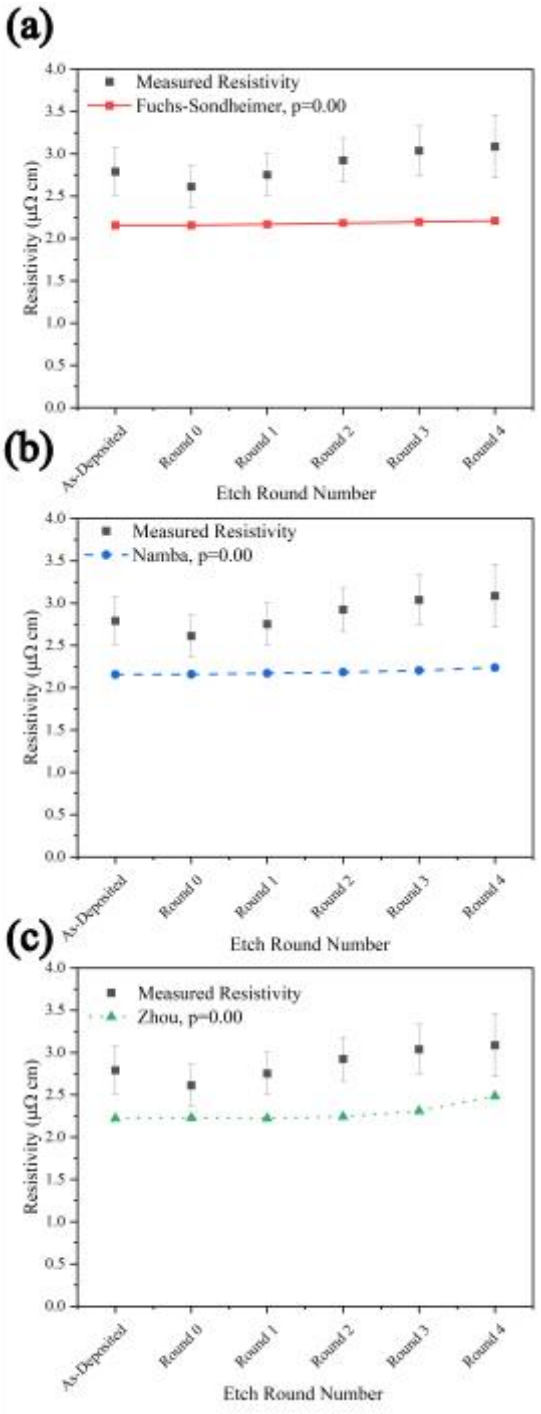

Figure 6.5: The measured resistivity of the Cu 60 nm on Al_2O_3 (grey squares) Vs processing point with (a) the modelled resistivity based on the Fuchs-Sondheimer model (Red squares with solid line), (b) The Namba model (Blue circles with dashed line) and (c) the Zhou model (Green triangles with dotted line).

At this point, it would be amiss to ignore the fact that the difference in resistivity between the As-Deposited and Round 0 process point is within the uncertainty of both measurements. As a result, there may not be a significant difference in resistance as a function of annealing. Considering this, further

four-point probe experiments with a smaller uncertainty are required. Considering this, the first change to the experimental design could be how the copper samples are produced. The copper on sapphire samples used in this study come from a single sample of 60 nm copper deposited onto a 50.8 mm in diameter sapphire wafer. This sample is then scored and cleaved by hand into 2 cm x 2 cm squares with an error of 0.05 cm at each edge. This results in samples with varying dimensions. As expressed in ***sub-section 6.4***, the exact dimensions of the sample influence the measured resistance and must be accounted for. As such, variation in the height and width between samples can introduce errors. For future experiments, the sapphire substrates should be diced using an automatic wafer dicing tool prior to the deposition of copper. For the Trifolium deposition tool, only 1-inch by 1-inch square samples are allowed. The increase in size of the sample may bring the influence of F_2 and F_3 to unity.

A second source of error in four-point probe experiments comes from misalignment between the probes. This is particularly relevant here as the four-point probe used has adjustable probes to allow for variation in the experimental setup. As such, probe alignment can vary between measurements, introducing uncertainty. To minimise this, the probes were aligned using deposited guide pads. Examples of these can be seen in ***Figure 2.8***. Though the deposited guide pads allow for relative alignment, there is still room on the pads to allow for error. For future experiments, maintaining the exact same probe positioning between measurements is imperative to minimising misalignment-induced uncertainty.

Table 6.1: Size effect models for surface scattering with their optimised parameters, the number of parameters that are user controlled and the residual sum of squared error (SSE).

Model Name	Model Parameters	Number of parameters	SSE ($\mu\Omega^2$ cm^2)
Fuchs-Sondheimer	p=0.00	1	2.8
Namba	p=0.00	1	2.7
Zhou	p=0.00	1	2.1
Mayadas-Shatzkes	R= 0.87	1	1.0
FS-MS	p=0.00, R=0.81	2	0.7
Namba-MS	p=0.00, R=0.80	2	0.5
Zhou-MS	p=0.00, R=0.78	2	0.3

To compare the fits of the models, the residual sum of square errors (SSE) is calculated. The SSE sums the variations of the model from the measured data set. The smaller this value is, the better the model fits the data. The sum of squared error is calculated via the equation

$$SSE = \sum_{i}^{n} \left(\rho_i^{Measured} - \rho_i^{Modelled}\right)^2. \quad 6.15$$

Here, n is the number of data points measured. For all three surface models, there are five data points available for comparison. These span from Anneal 1 to Anneal 5, as these were the process steps that involved a change in film thickness.$\rho_i^{Measured}$ is the experimentally determined resistivity and $\rho_i^{Modelled}$ is the modelled resistivity for the same measured parameters. Both the FS and Namba models result in extremely similar SSE values. The additional term representing the change in thickness of the film as a result of roughness does not appear to significantly improve the description of surface scattering compared to the FS model. On the other hand, the Zhou model shows a relatively lower SSE value compared to the other two models. Unlike Namba's model, Zhou's model considers the rate at which the surface height varies and the implication that has on the number of diffuse scattering events that can occur at the surface. The additional term representing the change in surface height per unit area appears to improve the description of surface scattering compared to the FS model and the Namba model. As such, the roughness effect on the surface specularity appears to be more influential in comparison to the variation in film thickness.

6.8 EFFECT OF GRAIN SIZE ON RESISTIVITY

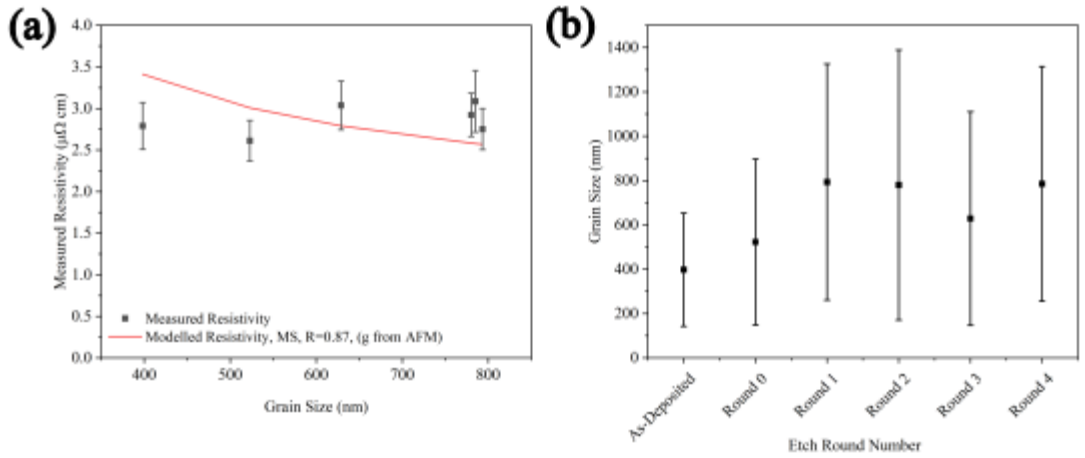

Figure 6.6: (a) The measured resistivity of the Cu 60 nm on Al_2O_3 (squares) vs grain size. The red solid curve represents the optimised MS model. The details of this model are summarised in Table 6.1. (b) The grain size versus etch round data for reference.

To test for a relationship between resistivity and mean grain diameter, the two measurements are plotted against one another. The results of this are shown in ***Figure 6.6.*** As can be seen from ***Figure 6.6***, there is no definitive increase in resistance with decreasing mean grain diameter. This is expected as the grain diameters are sufficiently large in these samples such that the rate of change in resistivity with grain diameter is negligible. Applying the MS model to this data produces a reflectivity coefficient of 0.87 at its lowest value of SSE (***Table 6.1***). Previous studies on copper films quote the reflectivity of individual grain boundaries to be anywhere between 0.016 and 0.7[31] depending on the grain boundary orientation. For film studies, the average grain boundary reflectivity is quoted between 0.25 to 0.49[9], [182], [183]. A potential source of such high reflectivity lies in the application of the model itself. Similar to the FS model, the MS model assumes sample resistivity is purely the result of grain boundary scattering as opposed to scattering at defects such as impurities or at the surface. In order to further improve the accuracy of this model, the intrinsic resistivity of the sample must be determined, and surface scattering must also be included.

The optimal value of the reflectivity coefficient determined for this data overestimates the reflectivity of the boundaries at 398 nm and 522 nm. These are measured on the film prior to any etch processing. Beyond this point, the MS model underestimates the resistivity of the samples. Noted in ***Figure 5.15***, as the etch develops, the regions surrounding the grain boundaries are depressed in height compared to the centre of the grains. The decrease in height could be thermal grooving as a result of the anneal and due

to an enhanced removal of material at the grain boundaries. By the 3rd Round and 4th Round mark, the surface shows clear holes along the boundaries. If the etch-anneal process causes the grain boundaries to be discontinuous, electrons would not be as capable of passing from one grain to another with each subsequent process round. This would explain the increase in resistivity for each round of the film and explain the difference in resistivity seen for data points that do and do not contain etching.

Within the study of surface scattering effects on thin film resistance, the impact of the degree of variation in film thickness is accounted for via the use of the RMS roughness. As expressed in ***Chapter 5***, the grain size of the copper on sapphire is a distribution rather than a single value. As such, the degree of variation of the grain size could also have an impact on the thin film resistance. For example, if two samples have a mean grain diameter of 50 nm but one has a wide standard deviation and the other a narrow standard deviation of grain sizes. The sample with a wider range of grain sizes has a proportion of boundaries well below 50 nm. This could lead to more grain boundary scattering events, increasing the measured resistance. When these values are evaluated using the Mayadas-Shatzkes model, the reflectivity coefficient could be inflated for the sample with a wider range of grain sizes. As a result, the two samples could have boundaries with the same degree of reflectivity, but the two appear different because the deviation in the distances between boundaries is not considered. As of the writing of this thesis, the author is unaware of a model that accounts for the effect of grain size distribution on thin film resistance.

6.9 SURFACE AND GRAIN BOUNDARY SCATTERING

To test if the reduction in thickness and increase in roughness could be responsible for the increase in sample resistivity noted when etching is introduced, the MS model is combined with each of the previously applied surface models by Matthiessen's rule and the results compared to the experimental data. The optimal model values are determined by the minimum SSE and are shown in ***Table 6.1.*** As can be seen from the table, the combined surface grain boundary models are a better fit for the data. However, this could be the result of having two fitting parameters as opposed to the single parameter used when each model is considered individually.

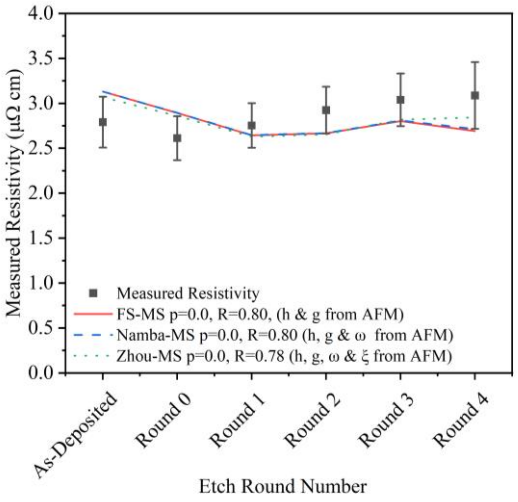

Figure 6.7: The measured resistivity of the Cu 60 nm on Al_2O_3 (squares) vs etch round. The red solid curve represents the optimised FS-MS model. The blue, dashed curve represents the optimised Namba-MS model and the green, dotted line represents the optimised Zhou-MS model. The details of each model are summarised in Table 6.1.

The optimal value for the Fuchs-Sondheimer – Mayadas-Shatzkes (FS-MS) model, the Namba-Mayadas-Shatzkes (N-MS) model and the Zhou-Mayadas-Shatzkes (Z-MS) model are compared against the experimental data in ***Figure 6.7***. All three models overestimate the resistivity of the initial film and the film after a single anneal. Alternatively, for processing points in which etching occurs, the modelled resistivity is systematically lower than the experimental data. The model results indicate that a single value of surface specularity and grain boundary reflectivity is incapable of describing the changing resistivity recorded in the 60 nm copper film on Al_2O_3 during the etch-anneal process. As stated during the evaluation of the MS model, this could be the result of etch-annealing making grain boundary discontinuous and thereby altering the perceived reflectivity for the duration of the etch process.

Of note, in ***Figure 6.7,*** the total resistivity of all three models decreases up to Round 1. The same trend is not observed in the experimental data. This could be evidence that the model is overestimating the influence of grain boundary scattering in explaining the thin film's total resistivity. If the decrease in resistivity at Round 0 is from the growth of the grains in the sample, then the same trend should be observed at Round 1 as the grains

continue to grow. Alternatively, between Round 0 and Round 1, the etch process used could cause sufficient damage to the boundaries to overshadow any decrease in resistivity obtained from larger grain sizes. Images of the grain boundaries via TEM[7], [171], [172], [184] cross sections, SEM cross sections[172] or STM could provide further insights.

Alternatively, measurable variables used for modelling, such as grain size distribution, thickness, RMS roughness and ACL, are determined via measurements taken over 8, 5 μm x 5 μm images per processing step. Since the samples are 2 cm x 2 cm in total area, a very small percentage of the overall surface is taken as a representation of the whole state of the sample. This allows room for bias in the measurable variables at different processing points. A strong example of this is shown in ***Figure 5.18***, where the edges of the sample have grain boundaries that are more continuous compared to those at the centre. In order to get a clear representation of the film, a proportional number of images at the edge and centre of the sample must be included in the analyses to make the measured variables truly representative. The measured grain sizes could also be further improved by verification by a supporting technique such as TEM[184].

To try and account for the change in the grain boundaries during the etch anneal process, the reflectivity parameter was allowed to vary for each data point as opposed to applying a single reflectivity parameter to describe the whole data set. The results of this is shown in ***Figure 6.8***. The numerical values noted on the trend lines are the reflectivity parameters that minimised the SE at each data point. In all three models, the reflectivity parameters for the As-Deposited and Round 0 data points are far lower than those for Round 1 onwards. Between Round 0 and Round 1, the first etch process is applied. These results indicate that the introduction of the oxidation-etch procedure notably damages the grain boundaries, increasing the perceived reflectivity of the grain boundaries. The decrease in the reflectivity coefficient seen at Round 3 is the influence of the smaller average grain size determined from the AFM images for these samples.

As stated in the previous subsection, according to film studies, average grain boundary reflectivity values for thin films are between 0.25 and 0.49[9], [182], [183]. By comparison, the values of grain boundary reflectivity determined by all three models are notably larger, even prior to any etching. The source of such high reflectivity could come from the application of the models. Similar to the application of just the FS or MS model, the combination models attribute sample resistivity to scattering at the free surface and grain boundary scattering. This means the scattering at defects such as impurities and scattering at the film-substrate interface are attributed incorrectly to either the free surface or the grain boundaries. This, in turn, could inflate the reflectivity values of the grain boundaries. To further improve the accuracy of this model, the intrinsic resistivity of the sample must be determined, and scattering at the film-substrate interface must also be included.

In summary, the resistivity changes measured during each round of the etch-anneal process could be modelled via a combination of surface scattering and grain boundary scattering, provided the reflectivity parameter for the grain boundaries is allowed to vary for each step of sample processing. The MS model

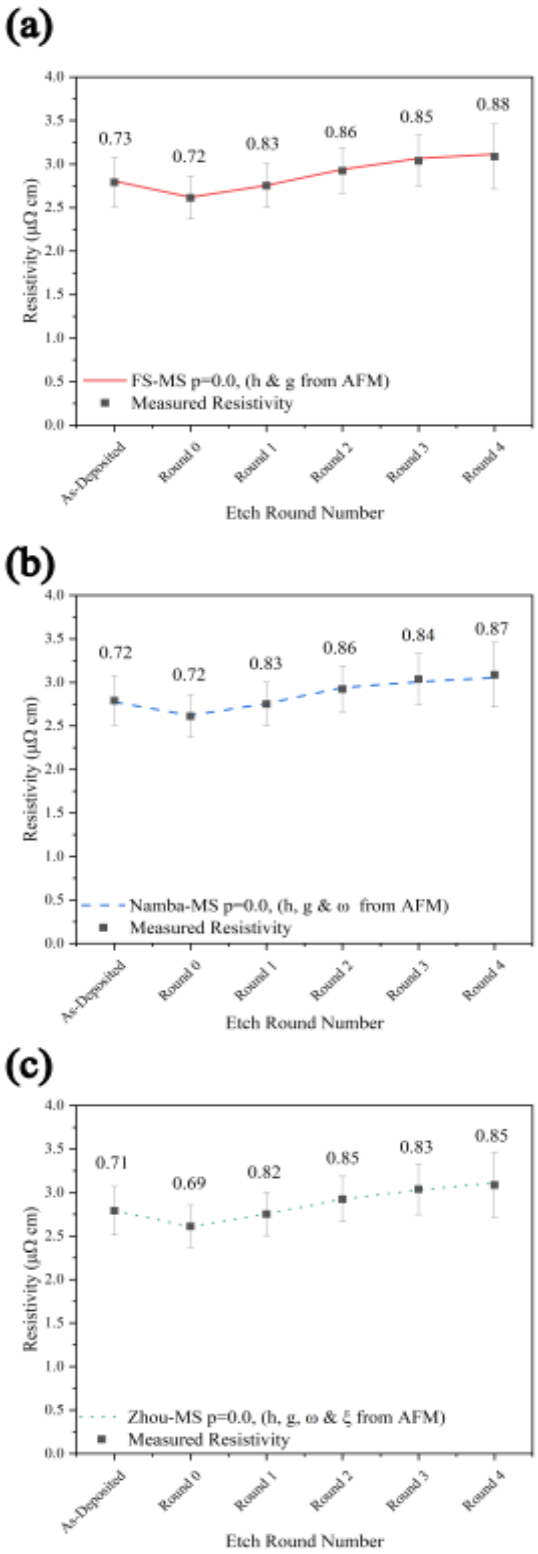

Figure 6.8: (a) The measured resistivity of the Cu 60 nm on Al_2O_3 (squares) vs etch round. The red solid curve represents the optimised FS-MS model. (b) The blue, dashed curve represents the optimised Namba-MS model and (c) the green, dotted line represents the optimised Zhou-MS model. The numerical value above each of the data points provides the reflectivity coefficient (R) that models the measured resistivity closest.

offers high values for grain boundary reflectivity. The large values could be due to the impurity contribution to resistivity being assigned to grain boundary scattering. To further improve understanding of the thin film's resistivity at each processing point, more sample information is required. To begin, the impurities present in the film and their influence on the overall resistivity must be accounted for[9], [171], [172]. Likewise, determination of the sapphire substrate's roughness[9], [185] would allow for further accuracy in the modelling of the surface contribution. More comprehensive measurements of the grain size, RMS roughness, and ACL could remove the variations detected from one processing point to another. Alongside this, supporting data taken by alternative techniques such as SEM and TEM could further support the values measured for input variables and allow for the effects of the etchant on the grain boundaries to be quantified.

7 CONCLUSIONS & FUTURE WORK

This thesis aimed to produce a 10 nm thin film predominantly consisting of restructured grain boundaries throughout the entire depth of the film with a starting material of 50 or 60 nm thick copper (111) thin films. Three separate etch processes were considered for thinning the thickness of interest. Of the three methods, the two-stage oxidation-organic acid etch provided the strongest control for material removal. Oxidation of the surface was completed by exposure of the copper to an oxygen plasma via a Diener PICO Barrel Asher. The subsequent oxide was removed via submersion in an organic acid, which preferentially removed copper-oxides over copper metal[143], [186].

The thickness of the film that can be removed depends on the thickness of the oxide formed on the surface. Copper, unlike aluminium, does not have a self-limiting oxide[187], [188]. This presents both a difficulty as well as an opportunity. In order to controllably etch samples, a consistent oxide thickness is required. Alternatively, oxide thickness varies depending on the sample state and oxidation conditions. For instance, the rate at which an oxide grows on a copper surface varies depending on the orientation of the sample surface[144], the size of grains in the sample[189], the temperature at which the sample is held and the method by which the sample is oxidised. In this study, the power used to produce the oxide layer was 200 W. This is the maximum power available on the Diener PICO Barrel Asher. To further control the thickness of the oxide, the effect of power and time must be explored.

Roughness evaluation of the two-step oxidation–organic acid etch process revealed that sample roughness increased with subsequent etching. The roughness introduced in the thin film samples was the result of the three-dimensional growth of the copper oxide on the copper (111) surface as a result of grain boundary preferential oxidation[189]. To create thin samples with known thickness and intact boundaries, the oxidation-etch process must not promote preferential oxidation at grain boundaries. The Diener PICO Barrel Asher used to oxidise the surface in this project does not direct the reactive oxygen neutrals and ions towards the sample. If the sample is biased in the presence of the plasma, high-energy oxygen ions would be directed at the surface. This could provide a method to make oxidation more homogenous over the surface. Previous studies using plasma oxidation as part of an etch process has shown that the use of plasma oxidation with an organic acid in the gas phase as an etchant has produced anisotropic etching on patterned surfaces[143],

[186]. However, none of these studies have evaluated the effect the process has on grain boundaries.

An annealing step, post etching, could help remove surface defects introduced by particle bombardment of the surface. Such processes are commonly used in STM post-sputter cleaning a sample. In this study, annealing was completed at 350 °C for 120 minutes under an inert atmosphere between oxidation-etch rounds. The time and temperature were both chosen to mimic the procedure used by Zhang et al. as closely as possible.[12] to minimise surface roughness. However, for an inert atmosphere, the same conditions promoted roughening of the surface. A more comprehensive study of the anneal conditions post etching is required to find the ideal time and temperature to minimise surface roughness.

An initial investigation into inducing grain boundary reconstructions in 60 nm copper films on C-plane sapphire was presented. The grains in these films were quite large, allowing for single boundaries to be imaged. The boundaries in these films appeared within valleys with depths in the nanometre range prior to any processing. Sputter-annealing rounds roughened the surface according to the root mean square roughness. This is contrasted with the film becoming smoother laterally according to the autocorrelation length. Further processing adjustments are required to allow the large step densities imaged on the cleaned surface to decrease such that the grain boundaries become accessible to be evaluated at the atomic scale.

The resistivity measured for 50 nm copper films on 7 nm of tantalum, which, in turn, was deposited onto a wafer of heavily doped silicon, had an average resistivity lower than that expected for pure copper. There are a variety of potential pathways that allow for conduction through the doped silicon. One such explanation could be that a thin layer of tantalum used as an adhesion layer may be insufficient to divert electrons from crossing into the doped silicon. Alternatively, the heavy doping of the silicon could make the Schottky barrier between the tantalum and the silicon narrow enough to allow tunnelling behaviour. Likewise, copper is capable of diffusing through tantalum at elevated temperatures. If the annealing processes used in this study allow copper to diffuse through the adhesion layer, an alternative conduction pathway to the silicon could be formed. Any of these processes result in conduction through the silicon substrate, making electrical

characterisation of the copper films impossible. Further study is required to determine why exactly the copper film is electrically connected to the substrate.

Alternatively, the measured resistivity of 60 nm copper films on C-plane sapphire at various points of the etch-anneal process could be modelled via a combination of surface scattering and grain boundary scattering models. The reflectivity coefficients determined for these samples are higher than would be expected. This was due to the impurities and hole features on the film being included as a part of the grain boundary effect. However, in the modelled films, both the area fraction of holes and the level of impurities remain constant.

The change in resistivity as a function of process time was best modelled when the reflectivity parameter for the grain boundaries was allowed to vary for each step of sample processing. The ability of electrical modelling to detect the state of the boundaries within samples containing large grains provides evidence that the four-point probe technique can be used to evaluate the electrical resistivity changes that reconstructed boundaries have on a thin film. To further this study, a sample with relatively small grains is required as larger grain sizes decrease the contribution grain boundaries have on total sample resistance. To try and achieve this, samples of 50 nm of copper deposited on 7 nm of tantalum, which are in turn deposited on silicon oxide, are being produced presently. These samples should have smaller grains while also being capable of being characterised by four-point probe experiments.

With a well-defined etch that minimises roughness, the next stage is to provide experimental evidence that the etched samples can contain grain boundary reconstructions and that these, in turn, improve film conductivity. To do so, STM can be employed to evaluate the boundaries and determine if the reconstruction has been induced. Two samples are required to test the effects the reconstructions have on sample resistance. The two must be processed near identically, with one sample containing the reconstruction while the other does not. For this, two samples will undergo the same etch-anneal processing. When the samples are at the desired thickness, one sample will be annealed to allow for the grain boundary to reconstruct. The inclusion of a surface roughness term in electrical models can account for differences in roughness from the final anneal. In the sample with reconstructed boundaries, the reflectivity coefficient should be lower. To further support this, local four-point probe measurements at single boundaries are described by Bishara et al. [34], [190].

can be utilised to measure the resistivity of individual boundaries before and after the induction of the grain boundary reconstructions.

Stress tests on comparable samples would also be required to test the stability of reconstructed boundaries against electromigration and stress voiding. For electromigration, stressing can be performed by applying a DC current to the test structures at elevated temperatures under an inert atmosphere. Failure times can be defined as the length of time required to increase line resistance between 1 and 10 % of the initial resistance value[191]. The samples can be analysed by AFM, STM, SEM, and TEM to determine the location of failures. The difference in the mean time to failure between samples with and without the reconstructed boundaries will provide insight into the electromigration stability of grain boundary reconstructions at 10 nm thicknesses.

Likewise, stress voiding can be evaluated using high-temperature storage testing. Here, test structures can be kept in a furnace at elevated temperatures. The thermal expansion mismatch between the film and the substrate causes stress. This stress allows voids to form. During storage, the electrical resistance of the line can be measured as a function of time. The test structure fails when a set increase in resistance is met. The difference in mean time to failure between samples with and without the reconstructed boundaries will provide insight into the thermo-mechanical stability of grain boundary reconstructions at 10 nm thicknesses [5].

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