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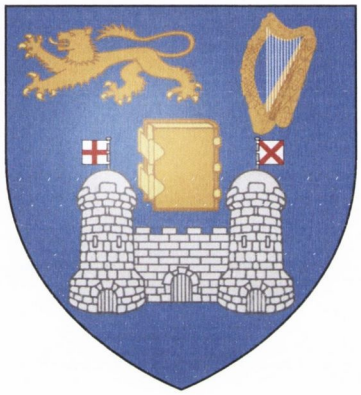
An Investigation of the Resistive Switching in Individual and Networks of Nickel Nanowires



A thesis presented to the University of Dublin,
Trinity College for the degree of Doctor of Philosophy
by

Alan P. Bell

Under the supervision of Prof. John J. Boland

April 2014

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Summary

Nickel/nickel oxide core-shell nanowires can be transformed from their native electrically insulating state to a conductive state by the formation of an atomic scale conductive filament bridging the oxide. This resistive switching can be utilised to store information; a conductive state can be thought of as ON or 1, and insulating, an OFF or 0 state. In this thesis we fabricated networks of nickel nanowires and subsequently contacted these networks using a two-step lithography. This contacting was required to enable electrical characterisation of the networks. Substrates were patterned with contact pads for electrical measurements, identification and alignment marks for electron beam lithography (EBL) using UV lithography. An e-beam sensitive resist, PMMA, was spin coated onto the substrate and windows in this resist were opened up using EBL. Windows with dimensions of approximately 50 x 300 μm were opened where the deposition of nanowires was desired. These windows allowed the control of the nanowire network placement and dimensions.

Nickel nanowires, with dimensions 10 μm x 60nm, dispersed in solution, were spay coated onto the substrates using an air gun. Following this spray coating the wires not contained within specified windows were lifted off due to the solvent dissolution of the PMMA on the substrate. These networks could then be contacted using EBL and subsequently electrically characterised.

At a nanowire-nanowire junction, an interface of nickel-nickel oxide-nickel exists. This interface acted as the location for the switching to occur. Various junctions were transformed to a conducting state, when a pathway of conducting junctions was made between electrodes of conducting junctions the network was ON. The wires within the network demonstrated an electrical fuse anti-fuse switching mechanism with electrical ON/OFF ratios of $> 10^7$ being realised. A length dependence on the initial transformation (FORM) from an OFF to an ON state was demonstrated with an independence of length for subsequent transformation (SET). Devices were cycled between an ON and OFF state 20 times and showed no significant degradation.

Individual nanowires were annealed in an ambient atmosphere and utilising the Kirkendall effect voids formed within the core of the wire. These voids were proposed to act as barriers to electrical transport along the wire. With individual wires being contacted segments within the wires separated by voids could act as memory cells. Electrical measurements were performed on the wires. However, the increased oxide thickness as a result of the previous thermal anneal made it difficult to form a conductive filament in the oxide. TEM was used to show the increase in oxide thickness of the nanowire.

Two types of memory switching in networks of nickel nanowires were demonstrated for the first time ever. One type is a memory effect, where the formation

of conductive filament remains after the cessation of an applied bias, the other type, a switching effect, requires the application of an applied bias. These two switching mechanisms were demonstrated in a nanowire network, opening up the possibility for a memory and switch element to be fabricated from the same material.

Finally, large scale nanowire networks were fabricated. These networks were fabricated without the requirement of the PMMA window. These larger networks opened the opportunity for the network conductivity to evolve. The smaller scale networks only offered a couple of potential pathways, whereas, the larger networks offered far more, this results in an evolving electrical behaviour with the material getting more and more conductive as sweeps were performed, something akin to a memristor. For the first time networks could be tuned to a certain conductivity by stimulating at high bias, then, when the desired conductivity value was reached the bias was removed and a conductivity value fixed. This conductivity evolution was also demonstrated in copper/copper oxide nanowires.

ABSTRACT

An Investigation of the Resistive Switching in Individual and Networks of Nickel Nanowires

Alan P. Bell

Under the supervision of Prof. John J. Boland

School of Chemistry & CRANN

NICKEL and its oxide are well known resistive switching materials. Sandwiches of nickel-nickel oxide-nickel can be transformed from their native insulating state to a conductive metallic state through an electrical stimulus. These devices typically require complex lithography, complicated material characterisation and electrical testing to verify operation. In this work, we present resistive switching in nickel nanowire networks. These networks are fabricated using a selective deposition technique developed to create network arrays. Device resistance on/off ratios of $\sim 10^7$ are obtained and these devices can be cycled repeatedly without obvious signs of degradation. These network channels have lengths approximately 2-5 times the average

length of nanowires used in the study. This ensures that individual wires do not bridge the contact electrodes.

Large scale networks, with dimensions approximately one order of magnitude wider and longer were also fabricated. These networks are electrically probed and can be transformed from a native off state to a conductive on state. However, due to the large scale nature of these networks they can evolve connectivity and increase their conductivity. This is due to the continuous switching of junctions within the network due to local resistive switching. This increase in network connectivity is due the large number of potential pathways bridging the channel. Each electrical sweep can activate more and more junctions, and lead to an increase in conductivity. As a result, these networks can exhibit a range of conductivity simply by sweeping voltage and activating an increased amount of wire-wire junctions. Once the desired conductivity is attained the device is electrically probed in a low bias regime and a defined resistance is observed. These networks are expected to have applications in memory, sensing and interconnects.

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I'm never gonna dance again, guilty feet have got no rhythm

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List of Abbreviations & Acronyms

DRAM	Dynamic random-access memory
SRAM	Static random-access memory
ITRS	International technology roadmap for semiconductors
FeFET	Ferroelectric field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NAND	Not AND
NEMS	Nanoelectromechanical systems
CMOS	Complementary metal-oxide-semiconductor
FeRAM	Ferroelectric random-access memory
MRAM	Magnetoresistive random-access memory
ReRAM	Resistive random-access memory
TEM	Transmission electron microscopy
SEM	Scanning electron microscopy
EBL	Electron beam lithography
PMMA	Poly(methyl methacrylate)
AAO	Anodic aluminum oxide
NiNW	Nickel Nanowire Network
NaOH	Sodium hydroxide
IPA	Isopropanol
HMDS	Hexamethyldisilazane
TMAH	Tetramethylammonium hydroxide
LRS	Low resistance state
HRS	High resistance state
RS	Resistive switching
CF	Conductive filament
NW	Nanowire
URS	Unipolar resistive switching
EDX	Energy-dispersive X-ray spectroscopy

1 Introduction

THE semiconductor industry is constantly striving for miniaturisation of feature dimensions, in both transistor and memory devices, whilst keeping fabrication costs down. Mass production of low cost functional nanomaterials as well as selective deposition of these nanomaterials is a research area of great current interest and with the promise to enable the continued miniaturisation of device features. These novel materials will need to exhibit the required properties and performance. For example; can these nanomaterials be switched between different resistance states, can the resistance be tuned, and are different memory switching mechanisms possible?

This thesis will address resistive switching in nickel nanowire networks. Thin film nickel oxide is already known to exhibit resistive switching; however, resistive switching in nickel nanowire networks has yet to be extensively investigated. Core-shell nickel nanowires containing a conductive nickel core and insulating nickel oxide shell will be employed to enable resistive switching. Resistive switching in a material allows for two distinct electrical resistance states, either low or high resistance, corresponding to an ON or OFF state. These two resistance states can also be considered a 1 or 0 in logic terms. We will demonstrate that resistive switching is observable in nanowire networks. This opens up the possibility for large area networks that can be electrically contacted without the need for expensive lithography and capable of possessing multiple resistance states. Important questions regarding the performance of nanowire networks and resistive switching will be addressed, e.g., on/off ratio of the devices, protocol for

selective deposition of the nanowires as well as electrode deposition and patterning for electrical characterisation.

Selective deposition of nanowires will be employed to accurately characterise nanowire networks. Initially, electron beam lithography will be employed to open a window in a PMMA film covering the substrate, which contains pre-patterned electrodes and alignment marks. This window will have defined dimensions and will be located at a desired location, and nanowires will be sprayed onto the substrate through the use of a spray gun. The PMMA resist will be removed and wires not adhering to the substrate will also be removed. Ideally only wires that were located within the window will remain. This method allows the accurate characterisation of nanowire network dimensions, as well as limiting possible leakage current through multiple pathways not defined within the network channel.

An investigation on the effects of annealing nanowires post spray deposition will also be presented. This study was prompted by the need to understand how to control the NiO thickness, which is critical in determining the conditions for resistive switching. In addition, at elevated temperatures evidence of void formation is observed in the core of these core-shell nanowires as a result of thermal annealing. We investigate whether these voids can be formed exclusively within the core of the nanowire and utilised as barriers to conduction to prevent cross-talk between memory cells contained within a single nanowire.

Before discussing device fabrication techniques or experimental results, a description of emerging memory technologies is presented, as well as the motivation behind the necessity for the development of these nanowire network materials.

1.1 Emerging Memory Technologies

Mature memory technologies will experience scaling and dimensionality issues in the next few years, see figure 1.1, and scaling to and below 14 nm will pose immense challenges.[1] Leakage currents and fabrication of high aspect ratio structures are the primary obstacles towards further miniaturisation.[2] However, there is a wealth of active

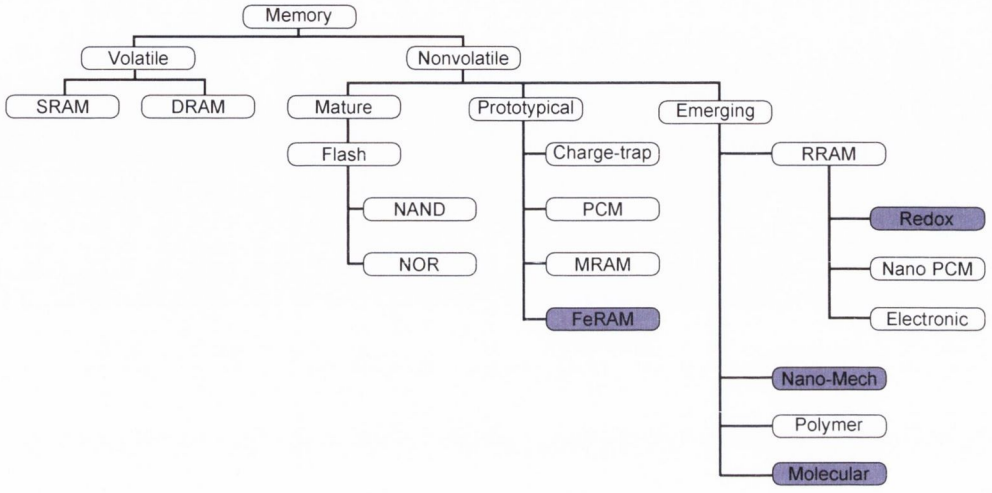

Figure 1.1: *Latest classification of memory type from ITRS.*

research in the area of emerging memory technologies. In order to be useful, these new memory technologies will have to meet performance criteria set out by International Technology Roadmap for Semiconductors (ITRS).[3] A continued shrinking of feature size, as well as the necessity for increased device performance are driving researchers away from well established memory technologies and towards emerging new material technologies, many of which were only discovered in the last 10 - 15 years. We will review these emerging technologies and examine their properties and potential as the next generation of non-volatile memory technology.

1.2 Memory Attributes

The ideal memory candidate should exhibit desirable characteristics such as; high density and read/write cycles, large ON/OFF ratio, low cost and power. Figure 1.1 illustrates the various categories of memory. The memories are divided into volatile and non-volatile, with non-volatile further separated into mature, prototypical and emerging. We will review those highlighted in blue in the next section.

Memory retention can be categorised as volatile and non-volatile. Volatile memory content is only retained through the use of a power source. In contrast, non-volatile memory can be retained for periods up to 10 years without the necessity of external power. The attractions of non-volatile memory are twofold; firstly, such technologies save energy since no external power is required to retain information, secondly, the time required for computers to boot up and shut down would be greatly reduced.

DRAM is an example of volatile memory; Read and Write memory operations both require short times, with embedded devices requiring nano-second time scales for read/write operations. Current device feature sizes for DRAM are approximately 90 nm, Samsung, one of the industry leaders have recently reported device features fabricated using 30 nm technology.[4] Memory retention time is a serious drawback, and in the absence of an applied bias the memory is retained for only 64 ms. In contrast, non-volatile memories have retention times of $>$ 10 years.

The present state-of-the-art non-volatile memory is flash memory. Flash memory contains two transistors separated by a thin oxide layer. If tunneling is achieved across the oxide the memory is in an ON state, where no tunneling takes place an OFF state results. However, flash memory suffers from operational constraints such as feature size reduction, leakage current as well as reduced on/off ratio and there are significant fabrication challenges involved in the further scaling of this technology. Flash also suffers from slow program speed ($\sim$ 10 µs), limited endurance cycles (10^4 - 10^5), high write/erase voltage (18 - 20 V), as well as complicated fabrication processes in which up to 10 mask sets are required.[5;6]

To replace flash memory, any proposed alternative technology needs to be superior in terms of scalability, cost and performance.

1.2.1 FeFET

A ferroelectric gate field effect transistor (FeFET) works on the same principle as a MOSFET device, with the exception that the usual gate insulator is replaced with a ferroelectric insulating layer. The addition of this ferroelectric layer enables the transistor to *remember* its state. A typical material employed as a ferroelectric layer is $SrTa_2O_6$.[7]

Device schematics are displayed in figure 1.2 (a). The information storage is realised by the two-state polarisation of this ferroelectric layer. The polarisation state is non-volatile. A writing process is performed by applying a voltage pulse (V_{GS}) between the gate and source electrode. This applied pulse needs to be greater than the coercive

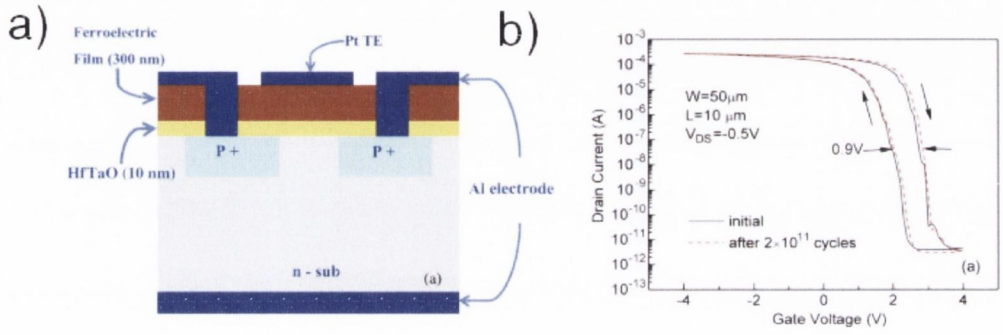

Figure 1.2: *(a) Schematic illustration of MFIS FET, (b) Electrical properties of device, I_D - V_{GS}.*[8]

field of the ferroelectric layer. As long as V_{GS} is greater than the coercive voltage of the ferroelectric layer a conducting channel will be formed. This conducting channel will persist where $V_{GS} = 0$, thus a bit will be stored. The device can be *reset* with a negative voltage pulse V_{GS}. I_{DS} - V_G characteristics are displayed in figure 1.2 (b). The applied drain voltage of -0.5 V is fixed, while the gate voltage is swept between $\pm$ 4 V. A clear memory window width around 0.9 V is visible as well as an on/off ratio of $\sim 10^7$. The excellent endurance properties of the device have been demonstrated,[8] with little difference in the V_G-I_{DS} curves after 2×10^{11} cycles.

Despite excellent performance, these device architectures pose the following challenges; any chemical interaction between the ferroelectric layer and the silicon substrate will result in device failure, a thick ferroelectric layer is required for data retention longer than the reported 37 days,[9] however, which in turn impedes device scaling below 14 nm. FeFETs are an attractive alternate memory architecture due to their quick read, write/erase times of 20 ns[10] and long term reliability with endurance cycles of greater than 10^{12} reported (compared to 10^4 for NAND flash).[11]

FeFET potentially offers an alternative to present memory technologies thanks to non-volatile data storage and non-destructive read operations. However, if the product is to be successfully commercialised, data retention times need to be increased and scaling issues need to be overcome.

1.2.2 Nano-electro-mechanical switches

Nano-electro-mechanical switches (NEMS) are based on the principle of a movable nano-sized beam or wire that can be positioned so as to complete or open an electrical circuit, corresponding to an ON or OFF state. NEMS benefit from both a near zero leakage current and zero sub-threshold voltage.[12;13] A potential shortcoming of the NEMS memory is the switching speed, depending on the initial conditions of the beam,

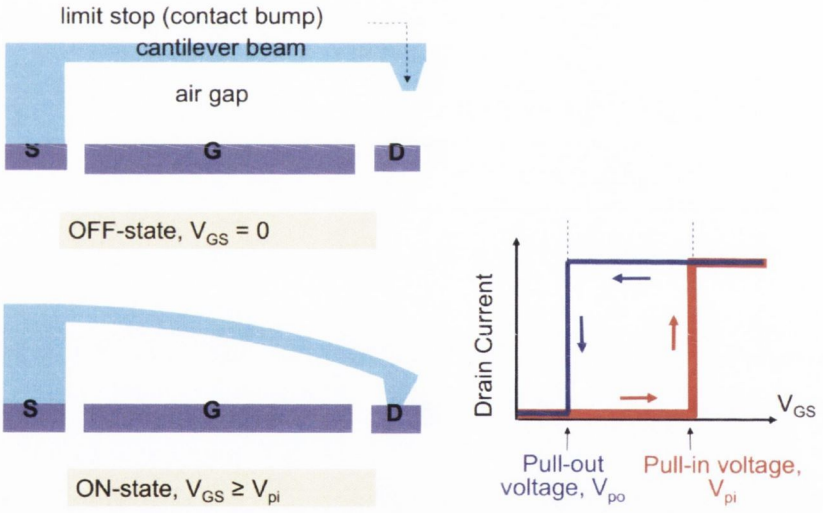

Figure 1.3: *Schematic operation of a NEMS, left, OFF condition obtained through non-contact, ON state obtained through application of gate-source bias greater than V_{PI}. The hysteretic nature of the system means either state is obtainable between V_{PO} and V_{PI}, only when $V_{GS} > V_{PI}$ or $V_{GS} > V_{PO}$ are ON and OFF states assured.*[14]

i.e. beam oscillation, following which a delay in turn-on can be experienced.[15] Contact issues between the beam and electrodes must also be considered, constant wear on the drain could have a detrimental effect on read/write cycle durability. Figure 1.3 displays

the operating principle behind a cantilever beam NEMS. The cantilever beam can be either fabricated through lithographic procedures or using an assembled nanowire. The beam makes/breaks contact between the source and drain based on the voltage applied between gate and source. V_{PI} is the pull-in voltage, this is the voltage required to deflect the beam onto the electrode. Conversely, V_{PO} is the pull-out voltage, applying this voltage will result in the beam losing contact with the electrode. An ON state is obtained when $V_{GS} \geq V_{PI}$, conversely, an OFF state results when $V_{GS} \leq V_{PO}$. The memory window for the device is between V_{PO} and V_{PI}, where both memory states are accessible.

The device reliability for long term operation is dependant upon the contact between the beam tip and the contact pad on the drain being robust and able to withstand over 10^8 switching cycles.

Tsuchiya *et al.*[16] have fabricated a silicon beam bridge, figure 1.4 (a), with both ends connected and the centre being deflectable based on the voltage being applied on the control gate. A load displacement curve in figure 1.4 (b) shows that approximately ± 500 nN are required to transform the device from one state to another. The free standing bistable silicon beams bending upwards (c) and downwards (d) can be observed.

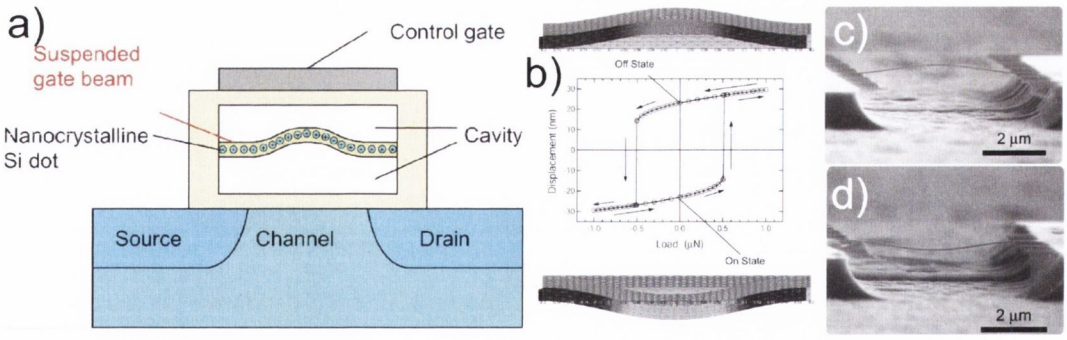

Figure 1.4: *(a) Schematic operation of NEMS memory device, (b) a displacement load curve showing operation of the device, with shape of the beam at the OFF and ON states corresponding to images above and below the plot respectively, (c) & (d) An SEM illustrating upward and downward-bent SiO_2 beams corresponding to an OFF and ON state respectively.*[16]

While there has been recent advancements in nano-electro-mechanical switches, notably by Feng *et al.*[17] , there are still numerous challenges to overcome before NEMS can be integrated into high density memory storage devices, notably; scaling issues below 14 nm, a high oscillatory pull out time, long settling time and tip contact issues. However, extremely small sub-threshold slopes $\sim$ 2-3 mV/dec[12] as well as a compatibility with CMOS fabrication methods offers potential that NEMS could be realised in the future as non-volatile memory, but only after these fabrication challenges have been overcome.

1.2.3 Molecular Memory Devices

If memory devices are to keep up with current scaling trends, realising memory elements with dimensions comparable to individual molecules is going to be required some time around the year 2025. Figure 1.5 displays channel length and feature size of transistors, and how these lengths have scaled over the last 40 years. The use of molecules as memory

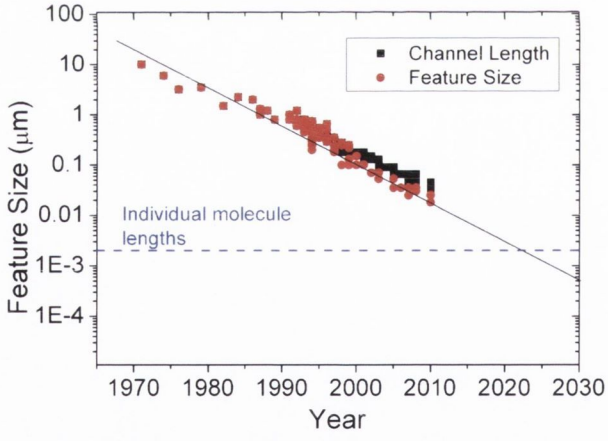

Figure 1.5: *Dimensions of channel length and feature size of transistors following Moore's Law.*[18] *Black line drawn as a guide to the eye. Molecular length scales will be reached in 2025 if present scaling laws remain valid.*

will require advances in fabrication technologies as well as a much better understanding of the electrical characteristics of the molecules themselves. A review in 2003 by Salomon *et al.*[19] of electronic transport measurements on organic molecules described how a simple

molecule, 1,8-octanedithiol, chemisorbed to two gold electrodes experienced a low-bias conductance spread of five orders of magnitude, this variance was dependant on the

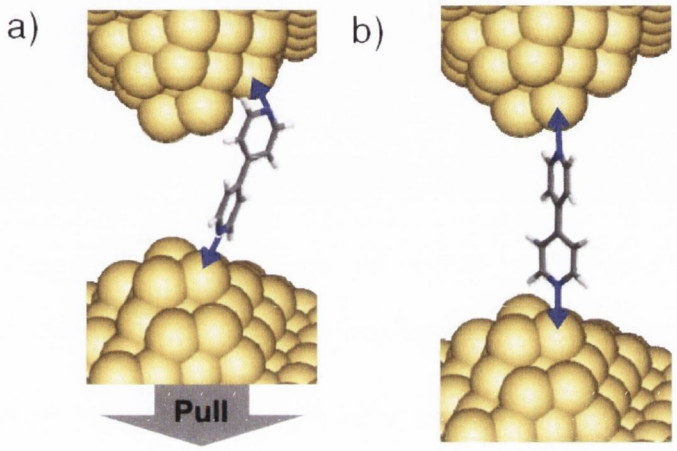

Figure 1.6: *Schematic illustrating the low resistance (ON) (a) and high resistance (OFF) (b) states in an individual molecule.*[20]

experimental method employed to contact the molecule(s). If molecular memories are to be introduced, a better understanding of the conductance of these molecules needs to be realised.

Despite the electrical characterisation challenges associated with probing molecules, resistance switching has been demonstrated in a *device* comprised of a single bipyridine molecule, figure 1.6, in which the molecule is compressed and stretched.[20] Rotaxane and nitrophenyl molecules also exhibit resistive switching and could be integrated into crossbar memory structures. However, in this case the switching mechanism is not well understood and an ability to fabricate electrodes to controllably contact the molecules is lacking.

Molecules may well be integratable into future memory devices, and if so, would be attractive due to the possibility of exploiting self assembly, low programming voltages and potentially cheap mass production of molecules all exhibiting identical dimensions. However, present fabrication technologies limits the development of molecular based memory.

1.3 State of the art in memory

Extensive research in Ferroelectric Random Access Memory (FeRAM), Magnetic Random Access Memory (MRAM) and Resistive random-access memory (ReRAM) is being performed. However, FeRAM and MRAM exhibit technological problems with regard to scalability. ReRAM does not suffer from these scaling issues. ReRAM demonstrates attractive characteristics, including, but not limited to; short read/write operation time and long retention times, large endurance cycles as well as multi-level storage. A summary of these properties is displayed in table 1.1. The short write/erase times exhibited in ReRAM memory are highly desirable for high performance memory technology.

Table 1.1: *Performance parameters for the fully scaled memories compared to the NAND flash scaled to the 16 nm technology generation, low performance qualities marked in red. Parameters obtained from ITRS*[9]

	NAND FLASH	FeFET	MRAM	ReRAM
Minimum F-scaling	16 nm	22 nm	7 - 10 nm	5 - 10 nm
Cell size	2.5 F^2	8 - 4 F^2	20 - 40 F^2	8-5 F^2
Multi-level	3 - bits/cell	NA	MLC 2 bits/cell	Yes
Write/erase voltage	18 - 20 V	0.6 - 0.2 V	$<$ 1.8 V	$<$ 0.5 V
Read voltage	0.1 - 0.5 V	NA	0.5 V	$<$ 0.2 V
Write erase current	Low	NA	$<$ 100 µA	0.4 µA
Write erase time	$>$ 10 µs	20 ns	$<$ 100 ns	$<$ 5 ns
Read speed	15 - 50 µs	20 ns	20 ns	$<$ 10 ns
Retention time	10 years	37 days	10 years	10 years
Endurance Cycles	10^4 - 10^5	10^{12}	10^{12}	10^{16}
Ease of integration	10 masks	NA	NA	NA

1.3.1 Perspective on ReRAM

In 1962 Hickmott[21] published the first paper on resistive switching, in which various metal-oxide-metal sandwiches were fabricated and their electrical properties investigated.

The results of this electrical characterisation are presented in figure 1.7. Large hysteresis was observed during a current voltage sweep when a 350 Å thick aluminium oxide layer is sandwiched between gold and aluminium electrodes. Pronounced negative resistance on the reverse sweep from V_{max} to 0 V was evident. As voltage is swept across the

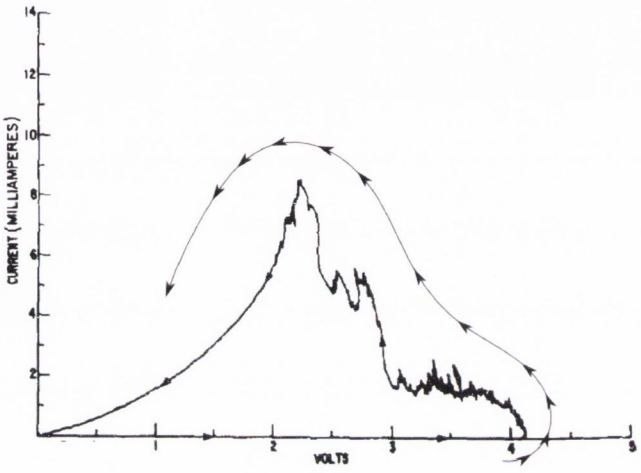

Figure 1.7: *Current volage characteristics of the establishment of a low resistance state in a 35 nm aluminium oxide film. Figure reproduced from Hickmott (1962).*[21]

oxide layer, and at $\sim$ 4.1 V an increase in current is observed, representing a reduction in resistance of the material. Lowering the voltage across the film results in an increase in current, and it is this increase that contributes to the negative resistance.

The present interest in resistive switching was stimulated by the works of both Beck *et al.*[22] and Asamitsu *et al.*[23], this interest is captured in a citation report charting the occurrences of *resistive switching* presented in figure 1.8. These citations represent investigations in numerous materials including binary and mixed valence oxides, such as TiO_2, NiO, $La_{0.7}Ca_{0.3}MnO_3$. The switching behaviour exhibited by these and all other materials can be categorised as being either unipolar or bipolar in nature.

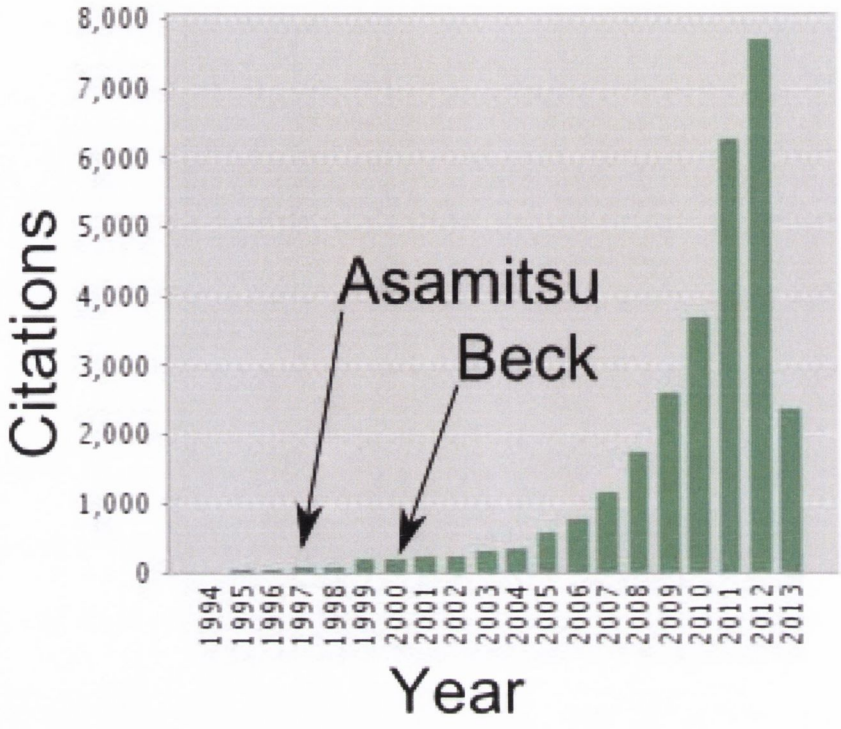

Figure 1.8: *Citations each year for resistive switching, citations downloaded from Web of Science, Thomson Reuters May 2013.*

1.4 Bipolar and unipolar resistive switching

Resistive switching is a physical phenomenon whereby a dielectric changes its resistance under the application of an electric field or current. The resistance change is non-volatile and reversible.

Resistive switching in transition metal oxides can be broadly described as either unipolar or bipolar.[24] Unipolar resistive switching is achieved with successive application of electric stress of either the same or opposite polarities. Bipolar resistive switching, in contrast, relies on the application of successive electric stresses of alternate polarity. The switching protocols are also different, with unipolar resistive switching requiring the application of a compliance current during the SET operation. However, the resistive switching classification becomes complicated in systems such as TiO_2, where both types of resistive switching have been observed.[25]

1.4.1 Unipolar resistive switching

In unipolar resistive switching, the switching effect is independent of the polarity of the voltage applied. SET and RESET operations can be performed at either a positive or negative bias. The operation of the device is presented in figure 1.9 (a). This switching is mostly observed in binary oxides, such as TiO_2,[26;27] NiO,[28;29;30] as well as SiO_2.[31] Initially the device is in a high resistance state and a FORMING operation is required. This FORM operation constructs the initial conductive filament, which is subsequently involved in switching operations. FORMING transforms the resistance of the device from a high to a low resistance state. The voltage is swept, and at a certain voltage an abrupt increase in the current is noted. The device is transformed from a high resistance OFF state to a low resistance ON state. The FORM operation is current limited to prevent a catastrophic break down of the dielectric. The device is now in an ON state. This state results in ohmic current-voltage characteristics at low bias. Resistance switching can now be realised. A RESET operation is employed to switch the device to an OFF state. RESET and SET operations are described in figure 1.9 (a). Subsequent SET and RESET operations can be performed. We will discuss these operations in more detail in the following section.

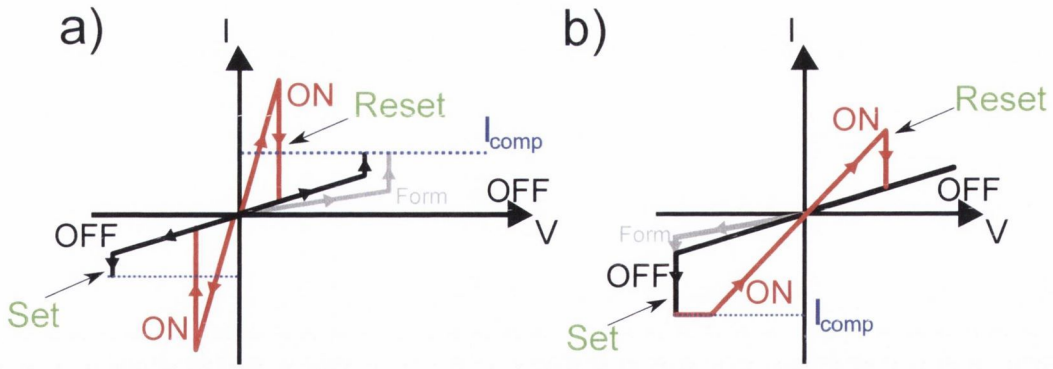

Figure 1.9: *(a) Unipolar resistive switching, set and reset operation take place at either polarity, with the set operation current limited. The subsequent reset operation typically takes place at a lower voltage.(b) Bipolar switching, set operation takes place on one polarity of the voltage and the reset operation requires the opposite polarity.*

1.4.2 Bipolar resistive switching

For bipolar resistive switching, the polarity of the voltage determines the resistance state of the sample. The characteristic current voltage curve of the device is presented in figure 1.9 (b). Initially the device is in a high resistance state. A FORM operation transforms the device to a low resistance state. This operation is similar to a SET operation, but differs in that the device is in a virgin state and has had no diffusion of charge across the insulating layer. Typically higher voltages are required to perform FORM operations rather than SET ones.

A subsequent positive sweep will result in the transformation to a high resistance state. This is referred to as a RESET operation. A subsequent negative current limited sweep transforms the device to a low resistance state. This is referred to as a SET operation. This type of switching behaviour is common in perovskite oxides, such as $SrTiO_3$:Cr[32] and $Pr_{0.7}Ca_{0.3}MnO_3$.[33] The driving mechanism for bipolar resistive switching typically is the electrochemical migration of oxygen ions.[34]

1.5 Unipolar resistive switching - conductive filament theory

A filamentary switching mechanism is typically proposed for most bipolar and unipolar resistive switching materials. The initial forming step is responsible for the first filament formation. Recent studies by Kwon *et al.*[35] clearly show the formation and rupture of conductive filaments to be the major switching mechanism in metal oxide resistive switching systems. In this conductive filament model, the formation and rupture of conducting paths in the oxide layer is responsible for the observed resistive switching.[36;37] Metal filaments are generated in the insulating oxide layer by field assisted diffusion. These defects subsequently bridge the oxide and a conductive filament is formed. Metal filaments are formed as a result of field assisted electromigration of oxygen ions. Figure 4.2 displays schematically the growth, rupture and setting of conductive filament with the accompanying current voltage operation displayed below. At and above a certain bias, the initial formation of conducting pathway(s) occurs inside the oxide. It is highly likely that a large number of nuclei for conductive filaments are formed initially, but

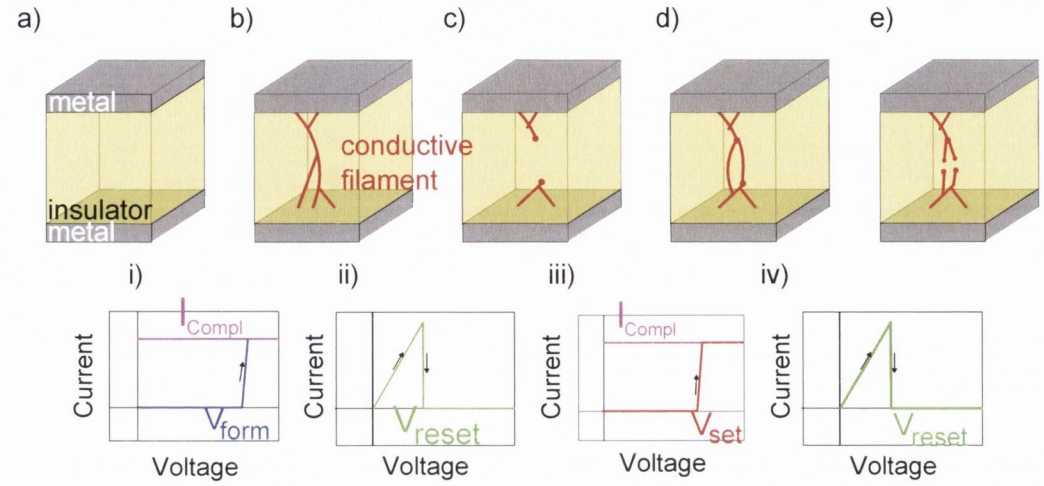

Figure 1.10: *Schematic of filament formation (a) - (e), corresponding current-voltage curve (i) - (iv). (a) metal-insulator-metal in virgin state, (i) current-voltage operation to form device, an abrupt increase in current indicates filament formation, (b) after forming operation, the insulator is bridged by a conductive filament, (ii) reset operation to transform device from an ON to OFF state, compliance is removed and voltage is increased, an abrupt decrease in current indicates filament has been ruptured, (c) schematic of filament rupture, note that only a discontunity in filament is observed, a large portion of the filament remains, (iii) set operation to transform device from OFF to ON state, a compliance current is applied and voltage is ramped up until an abrupt increase in current is noted, (d) filament formation has occurred and device is ON, (iv) reset operation to return device to OFF state, (e) filament rupture.*

once the oxide is bridged by a single filament, the rest of the conductive filaments stop growing.[38]

The FORMING operation is current limited to prevent the breakdown of the insulating oxide. The voltage required for this forming step is typically larger than the subsequent SET operations. After the forming process, the device can be switched between a high resistance state and a low resistance state by applying voltage pulses of different amplitudes. To transform the device from a conductive, low resistance state to an insulating, high resistance state a RESET operation is required. Unlike FORM and SET

operations no current compliance is applied. Voltage is swept and a large current is passed through the filament. Rupture of the filament occurs due to the high current and power passing through. As a consequence of this conductive filament rupture, the device is transformed from a low resistance, ON state, to a high resistance, OFF state.

The device can be transformed from an OFF state to an ON state with a SET operation. Before performing a SET operation a current compliance is again applied. The voltage is swept until an abrupt increase in current is noticed. This increase in current is as a result of the formation of filament pathways. These newly formed conductive pathways connect to the initially formed pathways and a metallic filament once again bridges the insulating oxide and the device is in a low resistance or ON state. The voltage required to FORM the device is generally larger than the SET voltage. Despite both operations transforming the device from an OFF state, the FORM operation requires the formation of a conductive filament spanning the full width of the oxide, whereas the SET operation is only bridging a small gap where the previously formed filament had ruptured.

Redox reaction and accompanying oxygen loss are believed to occur at the anode of nickel oxide resistive switching device.[38] Nickel oxide is a *p*-type semiconductor, and, as a result, hole injection is the majority carrier. Oxygen loss occurs at localised areas where holes are injected. When oxygen ions are lost by the redox reaction at the anode interface, nickel interstitials ($Ni_i^{''}$) can be formed through the following reaction:

$$NiO \rightarrow Ni_i^{''} + 2e^{-} + 1/2O_2(g) \tag{1.1}$$

these $Ni_i^{''}$ ions drift towards the cathode, whereas, the electrons generated simply drain off to the anode. When Ni_i generation becomes severe enough, they agglomerate and form metallic filaments.[36;39] NiO has no stable sub oxide phase; therefore, it is highly likely the conductive filament is formed from percolated Ni atoms.

However, as has been reported, the relative resistance ratio for filamentary nickel, defined at the ratio of resistance at 300K and 5K, is 1.6.[40] The relative resistance ratio for pure nickel is 29.67[41] and indicates the likely presence of a defective, impure metallic conducting filament in nickel oxide based ReRAM devices.

1.6 Thesis Summary

In this introductory chapter we have motivated the need for new memory types and have introduced various memory strategies as well as resistive switching mechanisms, Chapter 2 will detail the equipment used in this thesis and Chapter 3 describes the fabrication procedure of resistive switching nickel nanowire networks. Chapter 4 will introduce nickel nanowire networks and their resistive switching characteristics. Chapter 5 presents the modification of nickel nanowires by thermal anneal, including the observation of the Kirkendall effect which enables defect introduction and the modification of nanowires. Chapter 6 highlights the controllability of switching mechanism in nickel nanowire networks and potential switching devices. Memristance like evolutionary behaviour of both large-scale nanowire networks and short channel copper oxide nanowire networks is presented in Chapter 7.

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2

Techniques and Measurements

ELECTRON based microscopes are crucial in this work not only for the fabrication of nickel nanowire based ReRAM devices, but also to enable the analysis of the composition and directionality of the nanowire network. Nanowire networks will be spray coated onto insulating substrates. These networks will be fabricated using a combination of optical and electron beam based lithography to enable electrical characterisation. Electrical characterisation will be performed in an ambient environment using a electrical characterisation probe station.

2.1 Introduction to electron microscopy

Since its invention in 1931, the electron microscope[1] has been used in a wide variety of applications, ranging from imaging the interior structure of biological cells[2] to crystallographic information of nano-sized objects.[3]

The limited resolution attainable by light microscopes (which have a diffraction limit of approximately 200 nm) was the driving force for the development of electron microscopes. This resolution limit was realised in the late 1920s using optical microscopes. The transmission electron microscope (TEM) was the first electron microscope; it was developed by Knoll and Ruska in Germany in 1931.[1] A schematic of the original microscope is presented in figure 2.1 (left). An image of a modern TEM is displayed in

figure 2.1 (right), remarkably, the overall design of the TEM has hardly changed in the subsequent 80 years.

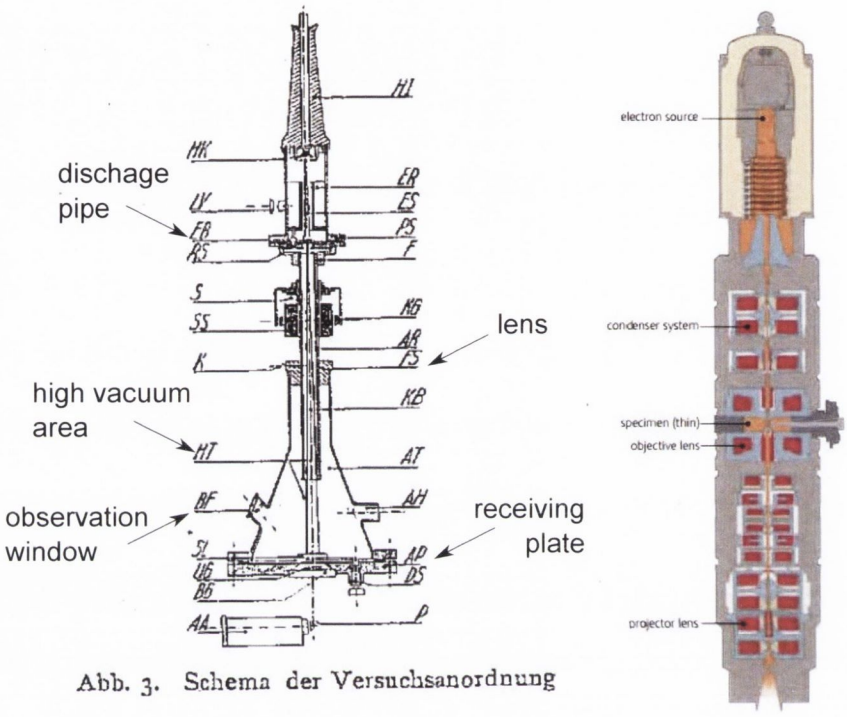


Figure 2.1: *(left) Diagram of first constructed TEM in 1931,*[1] *(right) Schematic of FEI Titan*[4]

The first published description of a scanning electron microscope (SEM) was reported in 1935.[5] In 1942 Zworykin described the first functional SEM with a resolution of 50 nm,[6] however, it was not until 1965 that the first commercial SEM was manufactured.[7] This early SEM had a resolution of 10 nm, representing an order of magnitude better resolution than the most advanced optical microscopes available at the time.

Electron microscopes operate on an almost identical principle to optical microscopes, except that beams of electrons are used to image the specimen; rather than photons. An electron microscope accelerates electrons from a source towards the specimen. This beam is focused using apertures and lenses, before interacting with the sample. In-

teractions with the specimen occur and are sensed by detectors in the chamber and transformed into an image.

Two different types of electron microscopes have already been introduced in this chapter, namely SEM and TEM. The main difference between SEM and TEM is how the images are generated. In SEM electrons are accelerated towards the specimen, much like as in TEM, however the interactions result in back scattered electrons and secondary electrons being generated and detected away from the specimen. TEM generates image with electrons travelling through the full thickness of the specimen. This requires the specimen thickness to be small enough to permit electrons to fully travel through its thickness, a requirement not imposed for SEM. The operation of the SEM and TEM will be described in sections 2.4 & 2.5. We will now describe the various types of electron guns used in these electron microscopes.

2.2 Electron Gun

Three types of electron sources are used in electron microscopes; tungsten, lanthanum hexaboride (LaB_6) and field emission gun. The most important performance characteristic of an electron source is brightness. Brightness is directly related to current density and ultimately determines resolution, contrast and signal-to-noise capabilities of the microscope. A comparison of electron sources is presented in table 2.1.

Table 2.1: *Electron sources and their characteristics*

Source	Brightness [$A/cm^2.sr$]	Source size	Energy spread [eV]	Vacuum [mbar]
Tungsten	$\sim 10^5$	~ 25 µm	$2-3$	$\sim 10^{-6}$
LaB_6	$\sim 10^6$	~ 10 µm	$2-3$	$\sim 10^{-8}$
Thermal field emitter	$\sim 10^8$	~ 20 nm	0.9	$\sim 10^{-9}$
Cold field emitter	$\sim 10^9$	~ 5 nm	0.22	$\sim 10^{-10}$

Field emission guns offer brightness properties three orders of magnitude better than tungsten or LaB_6 sources. However, this increased performance comes at a cost; field emission guns are most expensive and require a lower vacuum pressure to operate.

2.2.1 Tungsten and LaB_6 guns

The Tungsten and LaB_6 source is a V-shaped filament contained within a Wehnelt cap, displayed in figure 2.2. Electrons are emitted from the point of the filament. A positive

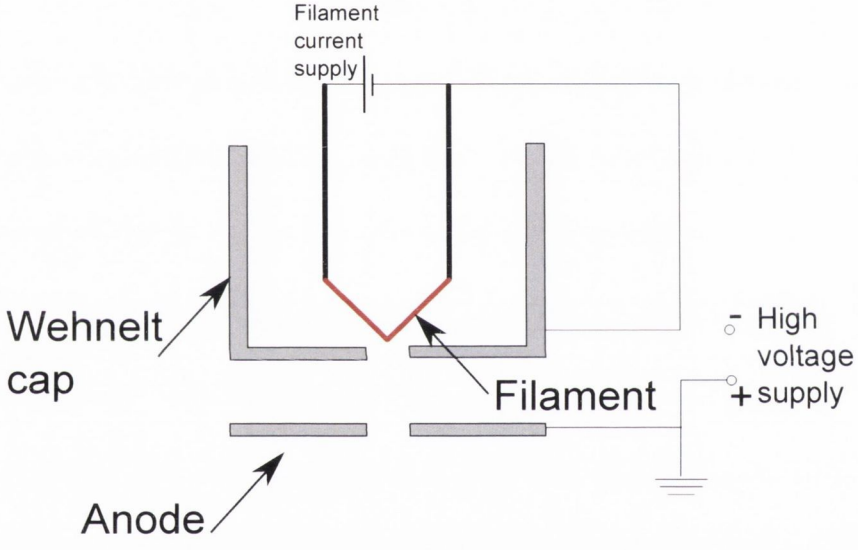


Figure 2.2: *Schematic of Electron Gun.*

potential is applied to the anode, and the filament is heated until a beam of electrons is produced. These electrons are accelerated by the positive potential on the anode plate. Electrons accumulate in the space between the filament tip and the cap, and this ensemble of electrons is referred to as the space charge. These electrons can move through a small hole in the Wehnelt cap and move down the column of the microscope to be utilised for imaging, analysis or lithographic purposes.

2.2.2 Field emission gun

Field emission guns are the most expensive type of electron source, but provide the best imaging and analytical characteristics. High resolution TEM requires the use of a field emission gun. The higher brightness and beam current provided by field emission guns produce finer electron beams with higher currents; qualities that enable better resolution. Two different types of field emission sources can be selected, namely, cold field and thermal field emission. Cold field guns offer higher brightness, however, unstable beam currents and a requirement to flash the tip regularly in the case of cold field guns to remove contaminants make thermal field emission sources a more attractive option. Thermal field emission sources do not suffer from these draw backs, and, as a result are found in the majority of modern commercial electron microscopes. For TEM, as noted by FEI,[8] a tungsten electron source is recommended for magnifications 40-50 kX, a LaB_6 for 50-100 kX, and only for magnifications $>$ 100 kX is a field emission gun the recommended electron source.

2.3 Electron-specimen interactions

2.3.1 SEM interactions

Image formation in an SEM is dependant on the acquisition of signals from electron-specimen interactions. These interactions can be split into two categories; elastic and inelastic interactions. A schematic of the interactions is displayed in figure 2.3. Elastic scattering occurs due to deflection of the incident electrons by the specimen's atomic nucleus or shell electrons. This interaction results in negligible energy loss during the collision, and large angle change of the electron trajectory. Electrons that are scattered by more than 90° are called back scattered electrons (BSE) and are used for image formation of the specimen. Heavier elements backscatter electrons more than light elements and appear brighter in images. This technique can be used for relative elemental analysis.

Secondary electrons are produced when an incident electron excites an electron in the sample and loses most of its energy in the process. The excited electron undergoes

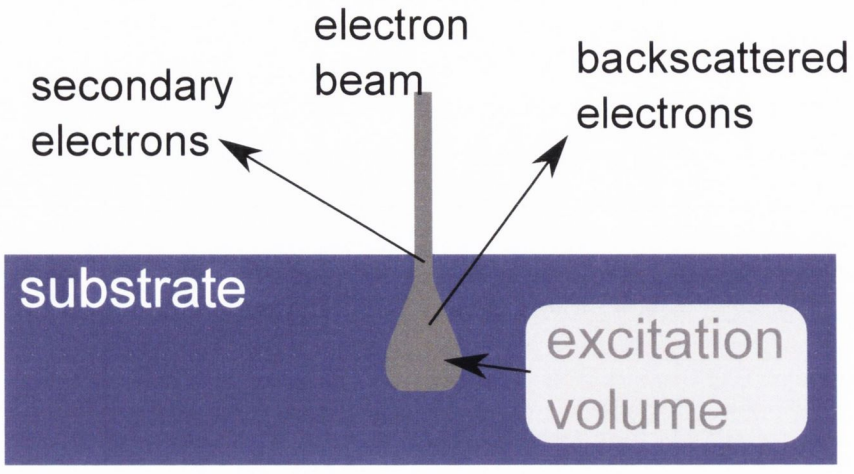


Figure 2.3: *Interaction volume in a specimen upon irridation with electron beam.*

both elastic and inelastic collisions until it reaches the surface, where the electron, if it possesses sufficient energy can escape. Owing to their low energy ($\sim$ 10 eV) only secondary electrons near the surface, from a depth of about 20 nm, can exit the specimen and be detected. This results in surface sensitive images, with enhanced secondary electron yields at edges or protrusions leading to increased brightness or an *edge effect*.

2.3.2 TEM interactions

Three different beam-specimen interactions are observed in TEM, namely, unscattered electrons, elastically scattered electrons, and inelastically scattered electrons.

Electrons that experience a relatively small amount of interactions with specimen are transmitted electrons. The transmitted electron count through the specimen is exponentially proportional to the specimen thickness. Electrons scattered elastically by atoms in the specimen follow Bragg's Law, $n\lambda = d\sin\theta$, where n is the order of diffraction, λ is electron wavelength, d atomic spacing and θ the angle between the incident electron beam and scattering planes. Electrons of a given energy $\mathcal{E}$ have a de Broglie wavelength according to the equation $\mathcal{E} = \frac{hc}{\lambda}$. For example, electrons with an accelerating voltage of 100 kV will have a wavelength $\lambda = 4$ pm. The angle θ is determined by the geometry of the beam and specimen angle. The scattered electrons

can be collated using a magnetic lens to form a pattern of spots. These spots correspond to the orientation and the structure of the specimen illuminated by the electron beam. This technique can yield information on orientation and atomic layer spacing.

The final type of electron interaction in a TEM is inelastic scattering. Inelastically scattered electrons interact with specimen atoms, so energy is lost through excitation of plasmons, electronic transitions, x-rays or photon emissions. These electrons are utilised for electron energy loss spectroscopy, and yield information on atomic composition, chemical bonding and surface properties through the analysis of angles and energies of scattered electrons using an electron energy analyser.

2.4 SEM - operation

SEMs use an accelerating voltage between 0.05 and 30 kV for the electron beam. A schematic of an SEM is shown in figure 2.4. The electron beam is collimated through electromagnetic lenses, focused via objective lenses and scanned across the surface. This beam is rastered across the surface, and secondary and back scattered electrons are produced as a result of beam interactions with the specimen. Surface topography information is obtained with this method, as well as elemental composition contrast using back scattered electrons. SEM is not capable of providing crystallographic information; another drawback of the technique is the deposition of contamination during imaging, especially at high magnification. Contamination within the chamber is typically caused by hydrocarbons from the pumps used to attain high vacuum as well as general use. The deposition is a result of the electron beam striking the hydrocarbon chains, breaking the backbone and causing carbon deposits to accumulate at the point on the specimen where the beam is located.

SEMs also require the specimen to be conductive to produce a clear secondary electron image. Insulating and biological samples are typically sputter coated with either carbon or gold/palladium before imaging to prevent charging. The conductive material is sputter coated onto the specimen to ensure uniform complete coverage. The differences between sputtered and evaporated material will be addressed in section 3.2.2.

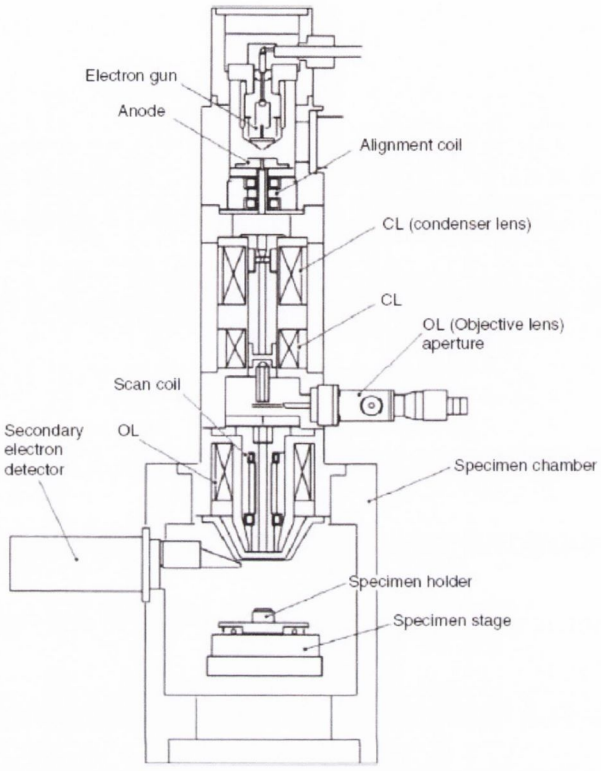


Figure 2.4: *Diagram of an SEM (Courtesy of JEOL, USA).*

Other methods to alleviate specimen charging exist, such as specimen tilting, variable pressure or low kV imaging. However, metal coating remains the most popular technique to enable imaging of non conductive specimens.

2.5 TEM - operation

TEM is a microscopy technique where a beam of electrons is directed toward a sample and only transmitted electrons are detected. Samples for TEM imaging need to be ultra thin, typically less than 100 nm. The sample needs to be thin enough to allow electrons penetrate the sample and be observed by a detector. Higher kV electron beams do allow for thicker samples, but the higher beam energy can also result in damage to the specimen. These thickness requirements are not an issue for imaging nanoparticles and

nanowires. Such nanomaterials can simply be drop cast onto a Si_3N_4 grid and imaged without any complicated sample preparation as their dimensions already satisfy thickness requirements. After passing through the specimen, transmitted electrons are collected and focused by the objective lens and a magnified image of the specimen is projected by the projection lens onto the viewing fluorescent screen at the base of the chamber.

TEMs operate at high voltages, typically 80 - 300 kV. The FEI Titan TEM being used in this study, is operated at 300 kV which corresponds to an electron wavelength of $\sim$ 2 pm. Figure 2.1 (right) shows a cross section of a modern TEM along with all lenses and apertures. The entire electron path from source to camera must be under vacuum, typically 2.5×10^{-9} mbar.

2.6 Electron beam lithography

Electron microscopes can be utilised not just for imaging, but also as a lithographic tool. Electron beam lithography (EBL) is one of the key fabrication techniques that enables the creation of patterns at the nanoscale. Electron based lithography has the advantage over optical based methods that smaller feature sizes can be realised. EBL involves irradiating a substrate with electrons, after is has been covered with a uniform thin film of electron sensitive material. This thin film is called a resist and it is this material that is modified during the exposure to electrons. There are two categories of resist; positive and negative. In the case of positive resists, the material is removed post development after the electron beam exposure, whereas for negative resists the material remains. The subtleties of the two categories of resists will be discussed further on in the chapter.

An increased interest in EBL started in the late 1960s[9] with a push to explore the dimensionality limits of fabrication. This work reduced dimensions of microelectronic fabrication to the nanometre scale. As early as 1979 sub 10 nm features were produced using electron beam lithography.[10] Interest in EBL has now extended beyond the semiconductor industry to an interdisciplinary field consisting of engineering, biology, chemistry and physics.

EBL can be performed in an SEM with either a tungsten or LaB_6 based filament or a field emission source. Tungsten and LaB_6 filaments benefit from higher attainable beam current compared to a field emission gun, however, field emission guns have longer source lifetime and lower current drift, both critical for successful EBL. Most SEMs can be converted to perform EBL with the addition of beam blanking plates in the column of the SEM and a computer to interpret the design files and control the beam. These blanking plates deflect the beam and serve to turn on and off the beam depending whether or not the pixel is required to be exposed.

2.6.1 Sample Preparation

Before any exposures take place the substrates must be prepared for EBL. Thorough cleaning is performed to ensure no residual contaminants remain. Firstly the type of resist needs to be decided, positive or negative. Positive resists are employed where metal deposition is going to take place after e-beam exposure. Negative resists are commonly used where etching processes are required. All the resist-based work in this thesis employed positive resists.

Once the type of resist has been chosen, the concentration of the resist in the solvent is important. The concentration of resist has a direct bearing on the resultant thickness of the deposited resist layer. If the resist is too thick, resolution will be compromised. However, a resist that is too thin can also provide difficulties with metal lift-off later in the fabrication process. The thickness of the resist can be further tuned by varying the spin speed during the process of coating the substrate with resist. Typical resist thickness for EBL range from 5 - 1,000 nm depending on application and fabrication requirements.

The resist spin speed also needs to be carefully considered. A slow spin speed will result in a thicker resist layer that will not have uniform thickness. A non-uniform resist layer will result in varying doses being required to fully expose the resist. A spin speed that is too fast can result in the substrate not being uniformly covered, and as a result, metal deposition will stick to the substrate and result in a failed process. Both situations are unacceptable for successful lithography, so optimisation is required. Upon completion

of resist spinning the resist is baked to remove residual solvent and to remove any strain in the film.

2.6.2 Exposure and electron interactions

During EBL exposure electrons penetrate the resist and undergo various scattering events. These scattering events and their implications will be explained in this section. As the electrons involved in EBL pass through the resist forward scattering events occur. The scattering is through small angles and broadens the initial beam diameter. Electrons penetrating through the resist into the substrate occasionally undergo back scattering. The back scattered electrons, as seen in figure 2.3 cause the so called proximity effect,[11] where the dose the pattern receives is affected by electrons scattering from nearby sites.

The forward scattered electrons can broaden the beam profile as a result of small angle scattering events. The increase in profile is given by the formula $d_f = 0.9(R_t/V_b)^{1.5}$, where R_t is the resist thickness and V_b is beam voltage. For a 15 kV beam and resist thickness 150 nm, the beam profile is widened by 29 nm. This beam profile widening has an important processing advantage for subsequent metalisation and lift-off. An undercut results due to forward scattering in the resist profile, and negates the necessity for a bilayer resist to assist in subsequent metalisation and lift-off.

The secondary electrons, as seen in figure 2.3, result of the slowing down of incident electrons. The secondary electrons have energies between 2 and 100 eV. These are the electrons that contribute to the majority of the resist exposure processes. The back bone chain scission of PMMA e-beam sensitive resist is realised by these electrons. They have little contribution to the proximity effect; however they do contribute a widening of the beam by about 10 nm. Certain high energy secondary electrons can have energies up to 1 kV and can contribute to the proximity effect in the range of a few 100 nm.

2.6.3 Accelerating voltage

The choice of accelerating voltage selected for EBL is critically important. Typically, the clearing dose will be inversely proportional to beam accelerating voltage. The clearing dose is the minimum dose required to clear the full thickness of resist after development. A high accelerating voltage will have the smallest interaction area in the resist, which is ideal for the fabrication of small features. However this will also require the highest dose. Figure 2.5 displays a simulation of electron scattering trajectories using the CASINO

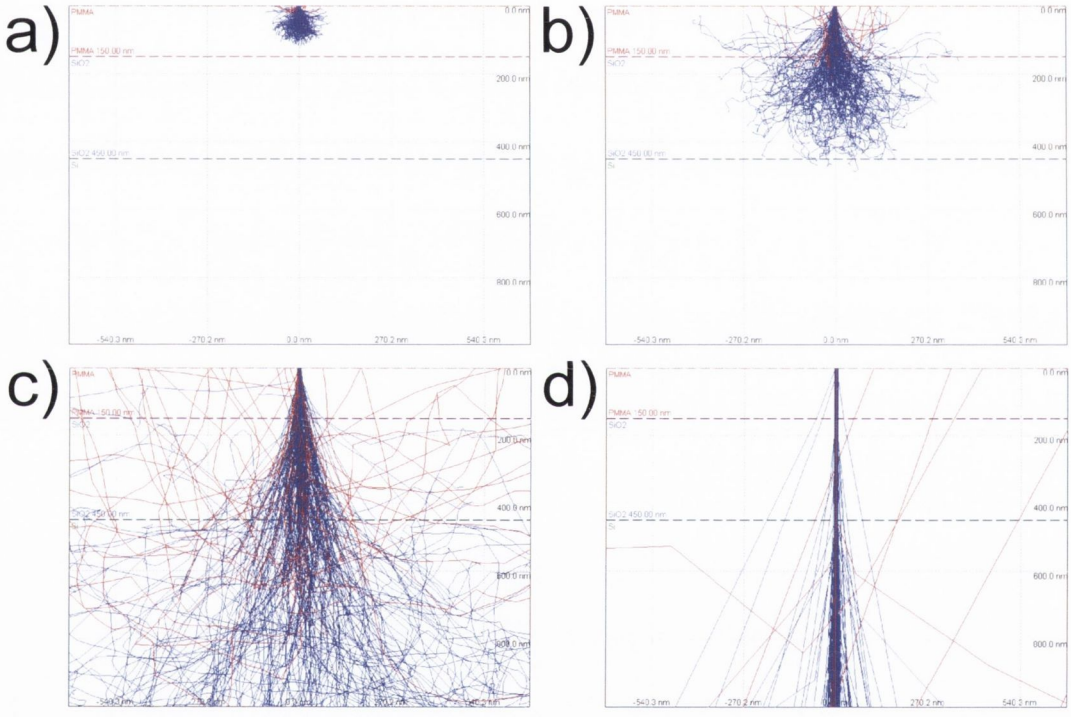


Figure 2.5: *Monte Carlo simulation using CASINO of beam energy in 150 nm of PMMA on 300 nm of SiO_2. (a) 2 keV beam showing electrons have not reached bottom of resist, making lithographic procedures impossible, (b) 5 keV beam large interaction area in the resist results in this beam voltage unsuitable, (c) 15 keV showing much smaller interaction area, the triangular nature of the beam interaction area is noticeable. This effective undercut is advantageous for metal lift-off, (d) 100 keV shows much smaller interaction area. However conventional SEM-EBL systems are not able to supply such high beam voltages.*

simulation package.[12;13] The sample is chosen to be 150 nm of PMMA on 300 nm of SiO_2 and bulk silicon below. Each simulation shows an area 1 μm deep into the substrate. Figure 2.5 (a) has an accelerating voltage of 2 keV and the electrons can not penetrate the bottom of the resist. This indicates that 2 keV is unsuitable for EBL. In figure 2.5 (b) the electrons for 5 keV accelerating voltage penetrate to the bottom of the resist, however, a large interaction area with the resist would make the fabrication of fine features being almost impossible. A suitable accelerating voltage is 15 keV and the electron trajectories are present in figure 2.5 (c). There is a small interaction area of the beam with the resist and an undercut of the resist is noted. Specialist EBL systems use 100 keV and figure 2.5 (d) presents the effective interaction area. The beam interaction area is smallest of the 4 accelerating voltages considered, and, offers the greatest chance to achieve smallest feature resolution. However this technology was not available for this study. Table 2.2 highlights the different characteristics of high and low accelerating voltage.

Table 2.2: *Relationship between Accelerating Voltage and Resolution*

Accelerating Voltage (kV)	1 2 3	10 15 20 25	30
Resolution	Low	$\Longrightarrow$	High
Charging	Little	$\Longrightarrow$	Much
Contamination	Much	$\Longleftarrow$	Little
Effects by disturbances	Large	$\Longleftarrow$	Small
Image quality	Soft	$\Longrightarrow$	Hard
Secondary electron signal	Strong	$\Longrightarrow$	Weak

2.6.4 Alignment

Mix & Match lithography, a fabrication strategy using a combination of more than one lithographic technique, has gained acceptance as a valuable strategy for reducing costs and increasing productivity in the semiconductor industry.[14] This technique takes advantage of quick, coarse, parallel based lithographic technologies, e.g. UV lithography, and fine, serial, flexible lithographic technologies, e.g. EBL and in addition gas injection system based methods, such as electron beam induced deposition and ion beam induced deposition of materials, particularly metals.

Typically, UV lithography is employed to fabricate larger features, such as, contact pads for electrical measurements and alignment marks to assist in multilayer lithography. The choice of metal for these features is important. Firstly, the metal should be inert. Gold or palladium are suitable and reduce the risk of tunnel barrier formation between the UV lithography metal and subsequent EBL defined features. Secondly, the metal should have high atomic weight and provide good contrast in an SEM. Metals like chromium and copper offer poor contrast, and as a result, are unsuitable for alignment marks.

Aligned lithography involves three specific alignment procedures. The substrate should be initially coarsely aligned to the x and y axis of the EBL system. The beam is then driven to a specific location on the chip, typically the edge of a alignment mark, and the coordinates are read. The beam is subsequently driven to a different location on the same axis and again the position is read. The EBL software then works out the angular correction and implements the correction.

A more precise alignment correction can now be performed. This alignment procedure is performed by imaging selected areas within the writefield and then defining the position of the alignment marks within the window. The EBL system calculates the xy offsets, rotation and shift based on alignment results. Upon completion of the alignment procedure, the system is ready to expose the desired pattern. However, the beam current needs to be read in order to ensure that the correct dose is delivered. A Faraday cup in the sample holder enables the beam current measurement.

Exposure Dose

The clearing dose is the number of electrons that are required to fully alter the resist so as to enable the removal of the resist during development at a later stage. The exposure dose can be expressed in terms of a dot dose, a line dose or an area dose. These three can be thought of in terms of 0, 1 and 2 dimensional doses respectively. The beam has a certain interaction area, $\mathcal{A}$, when exposing the resist. As the beam is rastered across the substrate, it has a certain step size and dwell time, and these are the parameters that define the dose.

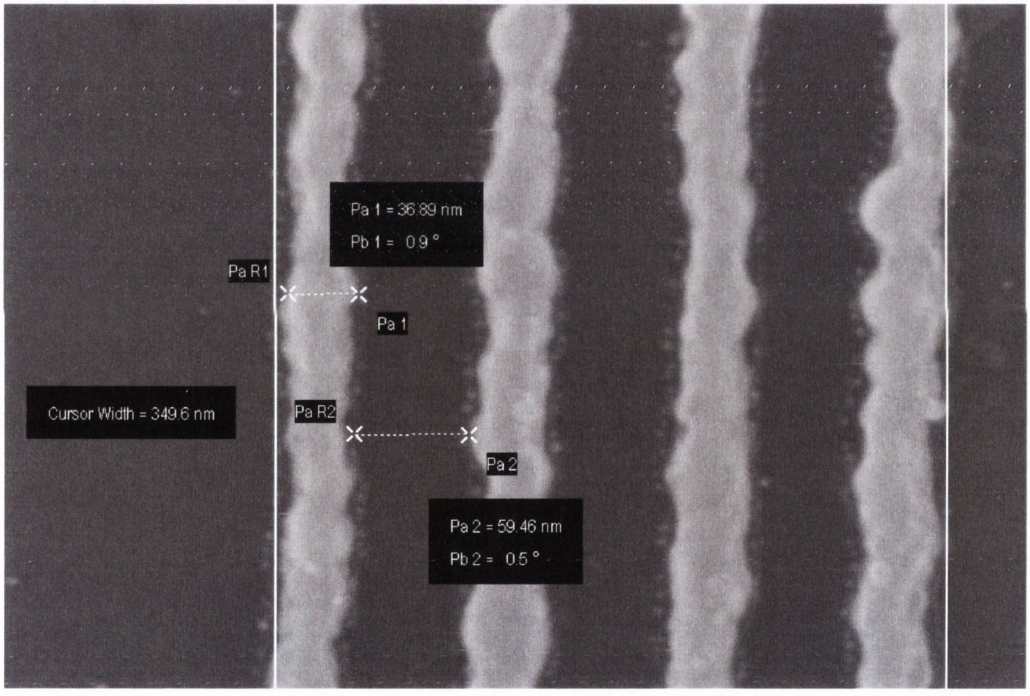
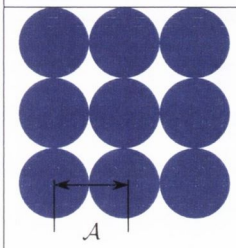
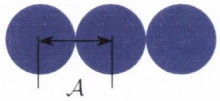


Figure 2.6: *Metal lines fabricated with PMMA and subsequent metal deposition. Line widths of sub 40 nm have been realised.*

Step size and dwell time are user defined, but due to the system limitations they have minimum values. Step size is linked to the writefield size and dwell time is limited by the blanker hardware to 400 ns. Table 2.3 outlines the different concepts of dose for areas, lines or dots. Exposure dose at a specific point, or pixel, is the product of the beam current and the dwell time. Ideally the beam current remains constant, so it is the

Table 2.3: *The different concepts of dose for areas, single pixel lines or dots.*

Area Dose	Single Pixel Line Dose	Dot Dose
$I_{beam} \times T_{dwell} / s^2$	$I_{beam} \times T_{dwell} / s$	$I_{beam} \times T_{dwell}$
		

dwell time that is adjusted to get the desired dose. The exposure times are calculated once the beam current and dose are given. The spot size is the electron beam diameter at the sample. Small spot size yields higher resolution.

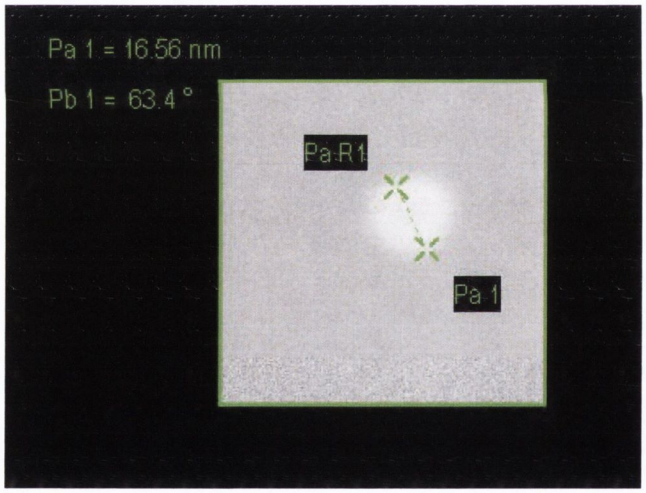


Figure 2.7: *Contamination spot burnt on resist.*

The aperture of the SEM affects the beam current. The smallest apertures result in the lowest beam current. The relationship between lens aperture and resolution is shown in table 2.4. 10 µm apertures are used for small scale features. Metal lines of width 40 nm are easily realised with most EBL systems. Those presented in figure 2.6 were fabricated using a Zeiss SUPRA SEM, with a Raith Elphy Plus attachment.

Table 2.4: *Relationship between Objective Lens Aperture & Resolution*

Apature size (μm)	120	60	30	20	10	7.5
Depth of Focus	Shallow	$\Longrightarrow$				Deep
Resolution	Low	$\Longrightarrow$				High
Specimen Current	High	$\Longleftarrow$				Low

For the fabrication of contact pads and larger features a 30 μm aperture is used. For the purpose of standard EBL lithography in this work, values of 15 kV accelerating voltage, 10 μm aperture, spot size $\sim$ 15 nm after 5 secs spot burning, working distance 5 mm, and beam current 25 pA were used, see figure 2.7. Larger contact pads were fabricated using the following values: 8 kV accelerating voltage, 130 $\mu C/cm^2$, 30 μm aperture, spot size $\sim$ 25 nm after 5 secs spot burning, working distance 7 mm, and beam current 220 pA.

2.7 Conclusions

The operation and principle of electron microscope has been presented in this chapter. A brief introduction to electron beam lithography has demonstrated the working principle behind this patterning technique. In the next chapter we will discuss the fabrication steps involved for a nickel nanowire network ReRAM device as well as obtaining dispersed nanowire solutions.

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3

Fabrication of ReRAM NiO nanowire networks

METALLIC and semiconducting nanowires have recently garnered a lot of interest in the research community due to their unique physical properties.[1] Nanowires are quantum confined in two dimensions and unconfined in the third dimension along the length of the wire. This confinement results in an electrical conduction behaviour that is different from that of their bulk counterparts. These interesting properties have led to the use of nanowires in the area of electronics,[2;3] optics,[4] magnetic storage devices[5] and sensing.[6] Much of the early interest from these one dimensional nanomaterials was concentrated on miniaturisation of magnetic recording media.[7;8;9;10] In 1994 giant magnetoresistance properties were found in Co/Cu multilayered nanowires electrodeposited in nanoporous polymer templates.[11] This electrodeposition technique is not limited to magnetic/metallic nanowires, compound semiconductor nanowires such as, Bi_2Te_3[12] and CdTe,[13] have also been synthesised.

Here we will focus on Ni nanowires and networks. Electrodeposition of nickel nanowires was first reported in 1975 by Kawai.[14;15] The use of anodised aluminium oxide (AAO) templates provided a high yield of nanowires, with typical pore densities in the AAO of 10^8 - 10^{10} pores/cm^2. We will demonstrate that the novel fuse anti-fuse transport mechanism in nickel nanowires can be utilised to realise a two state resistive switch. The first step in the process of realising these devices is nanowire synthesis and extraction from the AAO template. Once extracted from the AAO template and

dispersed in a suitable solvent, the wires are stable for months and do not have to be used immediately.

Silicon with an insulating thermally grown oxide (300 nm) was used as the substrate for device fabrication. This thermally grown oxide prevents any leakage current through the conducting bulk silicon substrate during electrical characterisation. Alignment marks and contact pads will be defined in resist using a UV lithography step followed by e-beam enabled metal deposition, schematic which is shown in figure 3.1 (a). A second lithographic procedure will be performed to open areas where nanowire deposition is desired, figure 3.1 (b). This step is essential to ensure transport is only possible through a specific section of nanowires. The presence of a uniform film of nanowires covering the substrate could allow transport over a large number of uncontrolled pathways. Nanowires were then sprayed onto the substrate, as shown in figure 3.1 (c). The conduction paths can be controlled by this selective deposition method, something that would not be possible in large area networks. Finally, a third lithographic step, figure 3.1 (d), is required to contact the nanowire networks for electrical characterisation.

3.1 Nanowire Extraction

Nickel nanowires contained within an AAO matrix were purchased from `nanomaterials.it` (Milan, Italy). The nanowires were created by electrodeposition of nickel in an anodic aluminium oxide template, which possesses a uniform tubular parallel structure with a conductive gold back layer. Nanowire extraction from the AAO involved the removal of the conductive gold film by using a swab dipped in *aqua regia*. Removal of the AAO template was achieved by placing the membrane in a solution of sodium hydroxide (NaOH) 1M for 90 minutes and sonicating for a further 2 minutes. The nanowires were concentrated in one location using a strong magnet outside the glassware to attract the wires together. The NaOH, used to dissolve the AAO, was decanted and replaced by isopropanol (IPA). The dispersion of nanowires and solvent was centrifuged at 500 rpm, the supernatent IPA was removed and fresh IPA reinfused. The dispersion was agitated and the centrifugation and IPA washes processes were repeated two more times. This

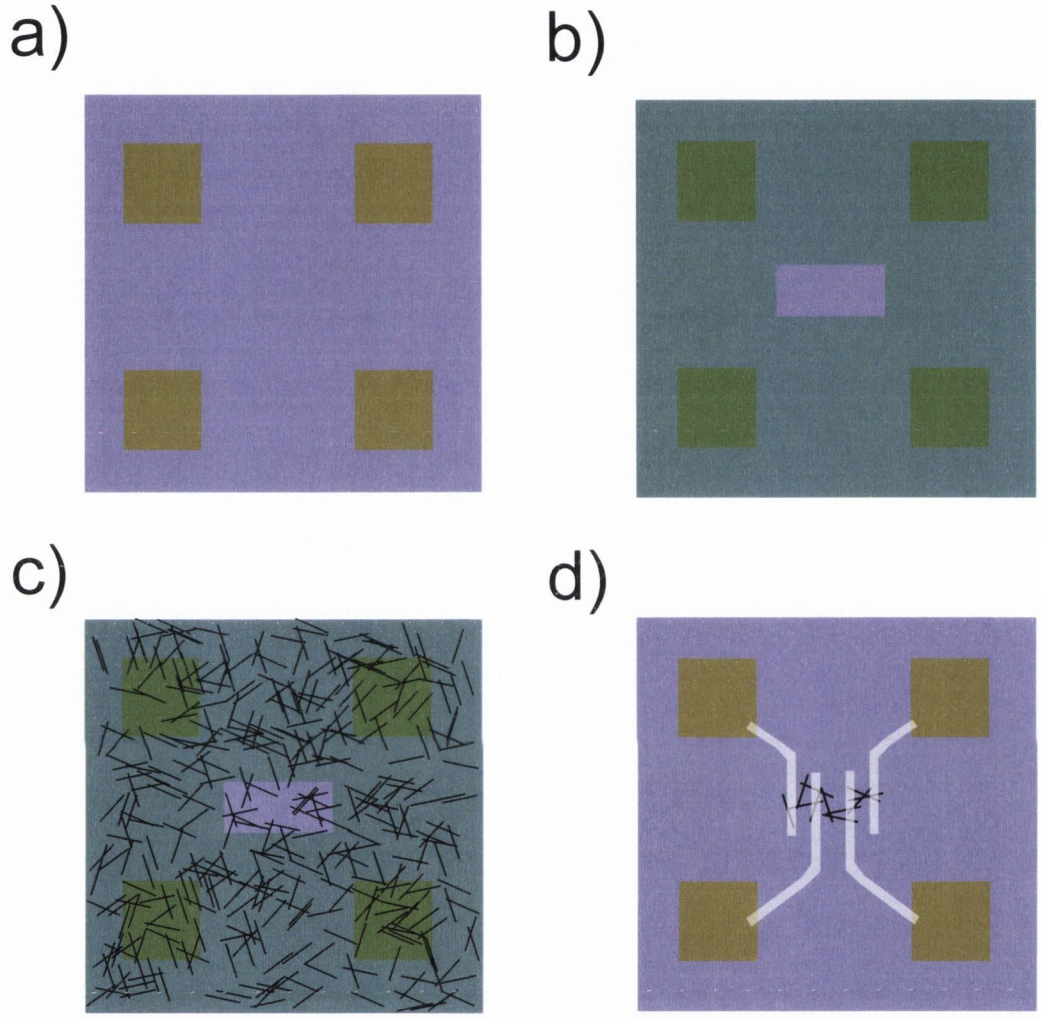

Figure 3.1: *(a) contact pads fabricated using UV lithography, (b) window opened in resist to receive nanowires, (c) nanowires spray deposited, (d) contacts fabricated using electron beam lithography.*

multi-step washing ensures a good quality dispersion of nickel nanowires and reduces the possibility that residual NaOH could remain and affect the uniformity of the nanowires. The final concentration of nanowires in solution is approximated from the initial quantity of nanowires contained within the membrane, assuming a minimal loss of nanowires in the extraction process, the final concentration of nanowires in solution is $\sim$ 1 mg/ml.

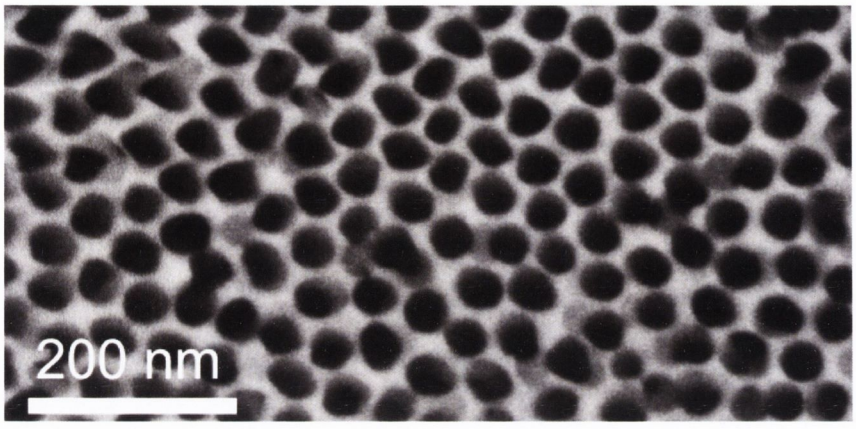

Figure 3.2: *Typical SEM plan view of the as-prepared AAO template with NiNW contained within the pores.*

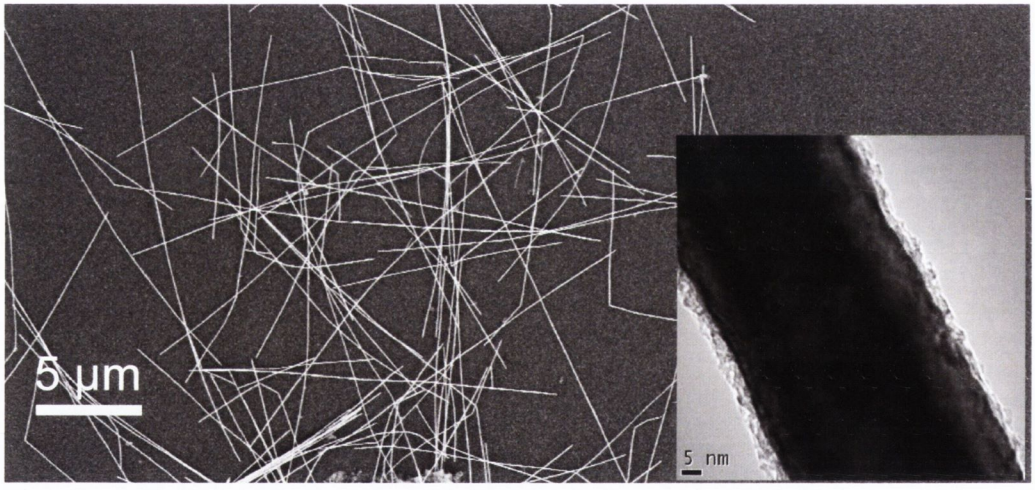

Figure 3.3: *SEM showing NiNW dispersed in IPA on silicon oxide substrate. Average wire length is 10 µm and diameter 60 nm. Inset TEM of single NW. The dark nickel core and brighter nickel oxide shell are clearly visible.*

The average length and diameter of the nanowires was determined by drop casting 5 µl of nanowires in solution on a 1 $\times$ 1 cm silicon substrate and performing an SEM inspection, see figure 6.5. The average length and diameter of the wires was analysed using ImageJ software, and values of 10 µm and 60 nm respectively were acquired. A

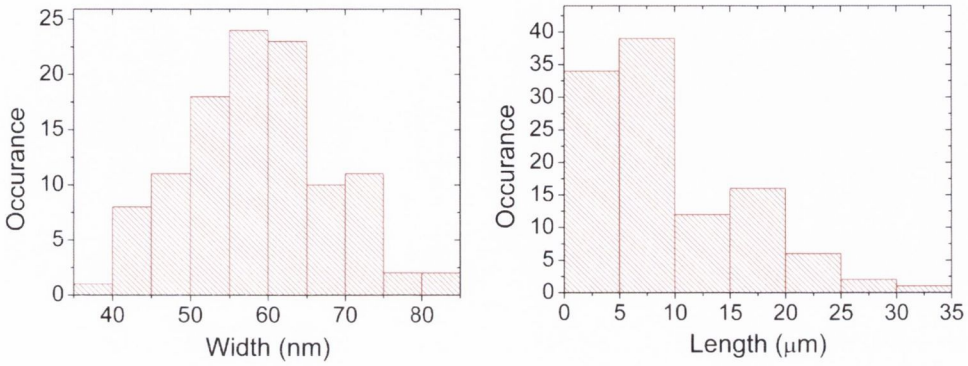

Figure 3.4: *Distribution of nanowire (left) width and (right) length.*

size distribution plot of the width and length of the nanowires is displayed in figure 3.4.

3.1.1 Elemental composition confirmation

In light of the nanowires being purchased from an external vendor, quality checks of the materials composition were performed to confirm the elemental composition of the nanowires. Analysis was performed in STEM mode in an FEI Titan TEM. EDX and EELS were performed using a 300 kV beam. These techniques will be used to confirm the composition of the wires as nickel and the shell as nickel oxide. Two areas were selected for analysis, one area in the shell and one the core.

Figure 3.5 shows a STEM image of nanowire being analysed. Minimal signal is observed in the EDX acquired on the shell of the wire, figure 3.5 lower left. However, the EELS signal, figure 3.5 lower right, shows two distinct peaks at 543 eV and 852 eV to eject electrons in the O K and Ni L shell respectively.

The core of the nanowire is now analysed using the techniques described previously. The EDX signal, figure 3.6 lower left has distinct peaks at 8.2, 7.5 and 0.85 keV corresponding to the presence of nickel and a peak at 0.5 keV corresponding to the presence of oxygen. The EELS scan, figure 3.6 lower right, has a clear prominent peak at 852 eV, again corresponding to the O K edge, however, the O peak is washed out by the

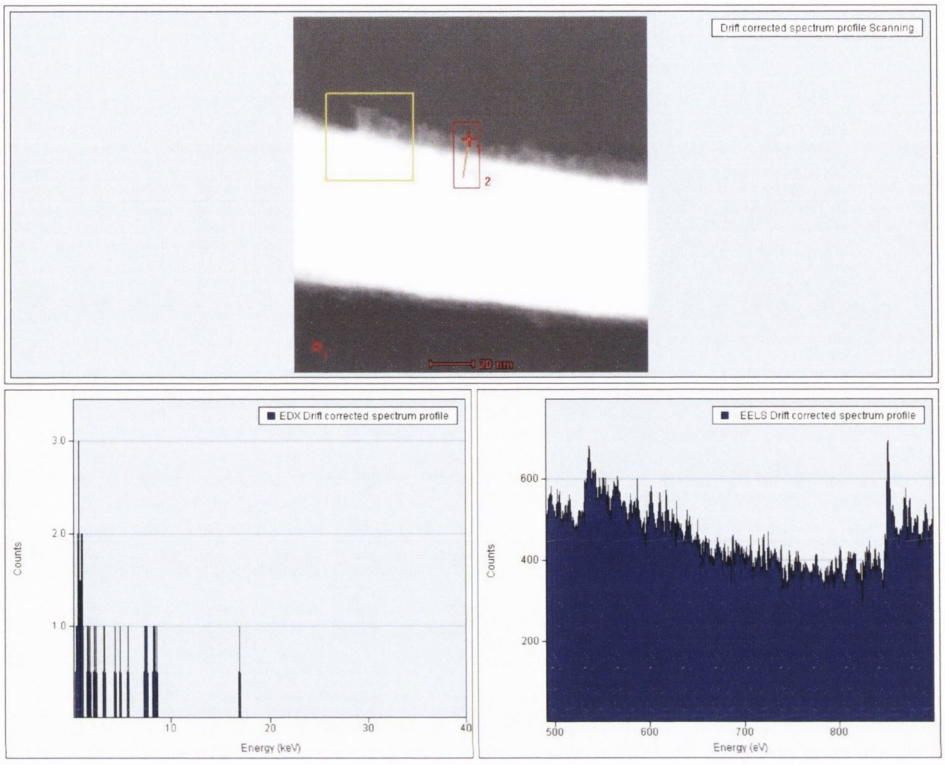

Figure 3.5: *EDX and EELS spectra of the shell of the nanowire. The red cross in the STEM image indicates the location of the acquired spectra.*

presence of nickel in the core of the wire. These measurement do however confirm that the wire consists of both nickel and oxygen as had been confirmed by the manufacturer.

3.1.2 Nanowire Deposition

The formation of random networks of nanowires requires a deposition method that ensures high uniformity of coverage, but yet achieves randomness of wire directionality and minimal drying effects. Various methods exist to deposit nanomaterials on substrates, such as, drop casting, spin coating and dip casting,[16;17;18] however, these methods have drawbacks. Drop casting suffers from capillary forces during drying that attracts the nanowires together and results in ring like deposits.[19;20] Spin coating does not suffer from drying effects, however, this method does not result in many wires remaining on

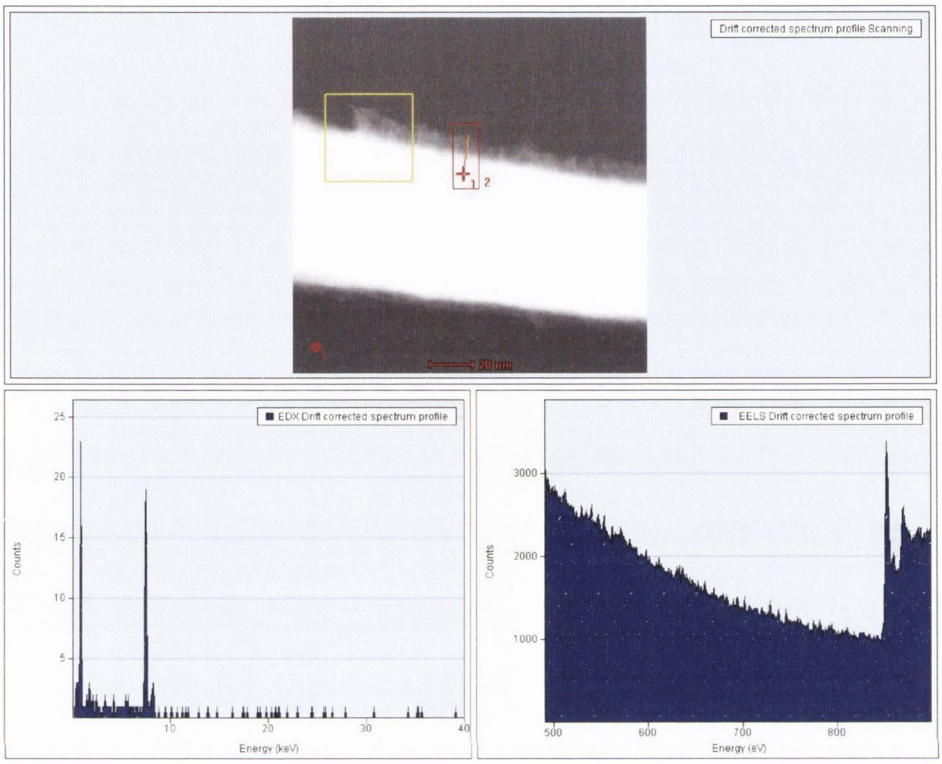

Figure 3.6: *EDX and EELS spectra of the core of the nanowire. The red cross in the STEM image indicates the location of the acquired spectra.*

the substrate, possibly as a result of the majority of the wires being (relatively) large distances away from the substrate during the spinning process and not effectively adhering to the substrate.

Spray coating offers a solution to the obstacles of uniform nanowire deposition by minimising drying effects.[21] Spray coating is a very simple technique and is wafer scalable. A spray gun and a compressed nitrogen source are the two components required for this method. The spray gun contains a 3 ml reservoir where the solution to be sprayed is dispensed. The spray gun was connected to a supply of compressed nitrogen, whose pressure is tuned with the use of a regulator. The airgun has a fine nozzle where the solution is ejected, and the nozzle is only 200 µm in diameter to ensure small droplets are produced. The nozzle is closely monitored to prevent the buildup of nanowires which could effect or potentially prevent the uniform spraying of nanowires.

3.2 Device Fabrication

A combination of UV and electron beam lithography is used to contact the network of nickel nanowires and provide contact pads to perform electrical measurements.

3.2.1 UV-Lithography

Throughout this thesis, where electrical measurements are performed, contact pads to enable probing were fabricated using a combination of UV-lithography and metal deposition. This section describes the steps involved in UV-lithography process.

UV light, sourced from a Hg lamp with wavelength 365 nm, is irridated through a chrome-coated quartz mask. Where there is no chrome present, light is transmitted through the mask; the UV light alters the resist, making it soluble in developer. Where there is chrome present the light is reflected and the resist is not altered. We will now detail the processes involved in UV-lithography.

Wafer cleaving 4" diameter (100) heavily doped silicon wafers were purchased from University Wafer, Boston, MA. A 300 nm thermally grown oxide was present on the top side. The wafers were 500 μm thick. The wafers were cleaved into 2 x 2 cm coupons to be compatible with lithographic processes and equipment available in this study. On the back side of the wafer, in a direction parallel to the (100) plane, a small 5 mm nick was scratched into the surface. With the wafer clamped by two large area tweezers, stress was applied parallel to the nick. A cleave fracture propagates down the wafer and a clean cut results. This method ensures minimal damage to the substrate, high yield and low probability of contaminants from the silicon dust that would otherwise result from top cleaving.

Surface preparation The cleaved chips were immersed sequentially in acetone and IPA for 5 minutes each, whilst being subjected to sonication. This removed any dust particulates and soluble organic contaminants. The presence of any dust particles on the substrate adversely affects the resist coating step.

Resist Coating The cleaned chip was mounted onto the spin coater. An applied vacuum ensured the chip did not become dislodged during resist coating. For a 2 x 2 cm chip, $\sim$ 200 µl of resist is dispensed. S1813 (Microchem, MA) positive resist is used for the UV lithography. The resist is dispensed drop-wise onto the substrate. Once the substrate was completely covered, the spin cycle was initiated. A 5 second 500 rpm dispense is followed by a 5,000 rpm spin for 45 seconds spin. Upon completion, the chip was briefly inspected for so called *shooting stars*, which are resist imperfections that occur as a result of contaminants that originated either on the substrate or in the resist bottle. The final resist has a thickness of $\sim$ 1.5 µm. In some instances, a 1:1 solution of IPA:HMDS (hexamethyldisilazane) can be spin coated on the substrate prior to resist spinning to improve adhesion.

Pre-bake The substrate was placed on a hotplate at 150 °C for 75 seconds to remove remaining solvent and to harden the resist. The resist only becomes photosensitive after this bake cycle.

Mask alignment The photomask is a piece of quartz with chrome on one side that defines the desired pattern. These openings allow UV light through and modify the resist on the substrate below. For the highest resolution, the mask must be as close as possible to the substrate.

Exposure The mask, substrate and resist were irridated with UV light (λ = 365 nm) via the UV lamp in an OAI mask aligner. The exposure time is important; too long and the resist will be over exposed, not long enough and the resist will not be fully removed and metalisation will not be possible. If the UV lamp is not properly focused, sloped resist walls will result, figure 3.7 (a) displays an example of sloped resist. This sloped resist will result in a failed metalisation. Ensuring the lamp is focused is a very important requirement.

Development For positive resists, such as S1813, development of the resist removes the regions exposed to UV light. S1813 was developed in 2.38 % TMAH (tetramethylammonium hydroxide) for $\sim$ 25 seconds and rinsed in flowing DI water. Vertical, straight, resist walls should remain. This resist profile ensures a discontinuity in

the metal film after metalisation. Angled resist sidewalls, figure 3.7 (a), result in failed lift off. The desired, vertical sidewall profile is displayed in figure figure 3.7 (b).

Metalisation Typically 5/30 nm Ti/Au metal was deposited in a Temescal FC-2000 e-beam metal deposition tool. Evaporation rates of 1 Å/sec are employed.

Resist lift-off Gently heated acetone, typically 45 °C, is used to remove the resist. Samples are washed in IPA and dried in flowing N_2. Details of metal deposition and subsequent lift-off are provided in the next section.

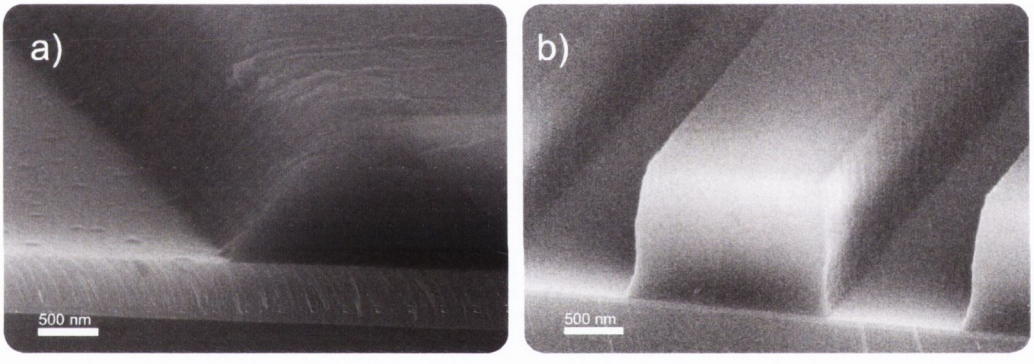

Figure 3.7: *(a) Angled resist sidewall, (b) Vertical 90° resist sidewall.*

3.2.2 Metal Deposition

Several methods exist for metal deposition, two of the most popular being evaporation and sputtering. Evaporation is a line-of-sight based material deposition technique, figure 3.8 (a). The advantage of this method over sputtering is that the walls of resist do not

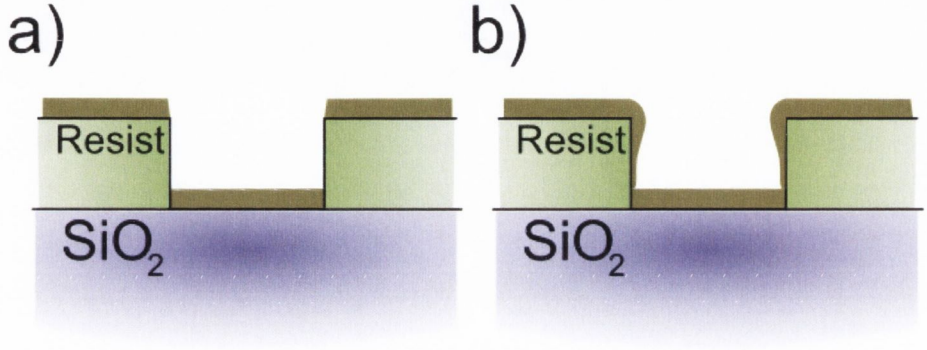

Figure 3.8: *(a) Schematic of metal evapouration, note no metal coverage on resist sidewalls, (b) sputtering showing evidence of metal buildup on sidewalls.*

receive any material during deposition. Sputtering is a widely used technique for metal coating of insulating samples to be imaged in an SEM, as it is a uniform deposition technique. Uniform coverage of substrate and resist sidewalls, figure 3.8 (b), results in so called *rabbit ears* on the edges of metal features. These rabbit ears can cause discontinuities between metallic features in multi-step lithography; an example of such discontinuity is displayed in figure 3.9. These discontinuities can result in an electrically open circuit and failed electrical characterisation. Consequently, all metal deposition involved e-beam evaporation using the Temescal FC-2000 system.

Sample mounting Substrates to receive metalisation were mounted onto a home built chip holder and placed in chamber of the deposition tool.

Vacuum The deposition chamber is pumped down to a pressure of $\sim 1 \times 10^{-6}$ mbar. At this pressure, metal deposition can commence. Metal deposition rates of 1 Å/sec were used to obtain uniform film thickness, to minimise the grain size of the metal, and also to avoid introducing excess surface roughness. 5 nm of titanium

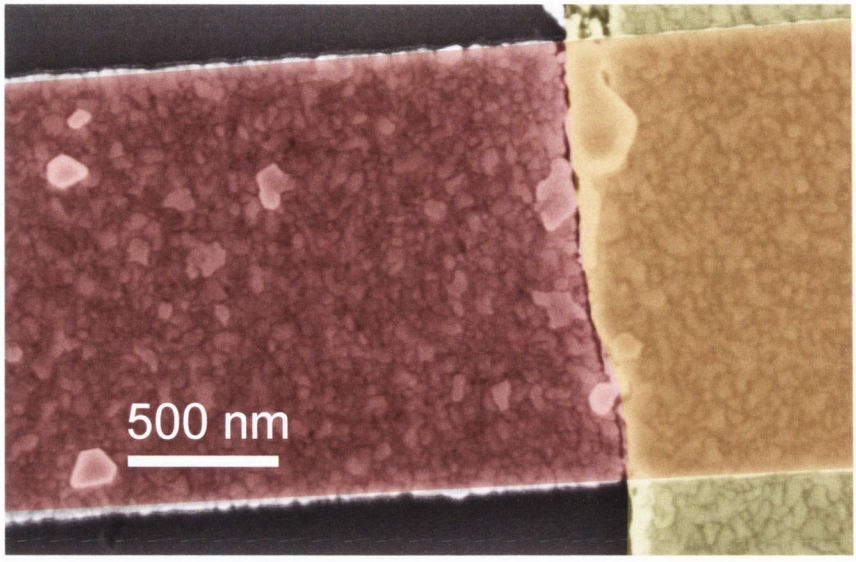

Figure 3.9: *Interface between UV-lithography defined electrode (yellow) and an EBL defined electrode (red). Discontinuities between the electrodes are evident.*

and 40 nm of gold (99.999%) were deposited. The 5 nm of titanium served as an adhesion layer between the silicon oxide and gold. Gold was used as the top metal since the presence of an electrically insulating oxide layer would act as a tunnel barrier and inhibit conduction between the bottom contact pad electrodes and subsequent EBL defined electrodes.

Lift-off and sample clean Lift-off was performed in warm acetone for 30 minutes, and, once complete, substrates were washed in IPA, figure 3.11 (a). The large feature sizes of UV lithography means that it is visually possible to observe when the lift off process is complete. A 3 minute oxygen plasma was performed following lift off to remove any residual resist polymer and any organic contaminants. An optical image shows the finished pattern, figure 3.10 (a), along with the schematic of the dimensions of the pads and alignment marks, figure 3.10 (b). An SEM image of a set of 4 contact pads and alignment markers is displayed in figure 3.10 (c), with the schematic of the pads and alignment markers displayed in figure 3.10 (d).

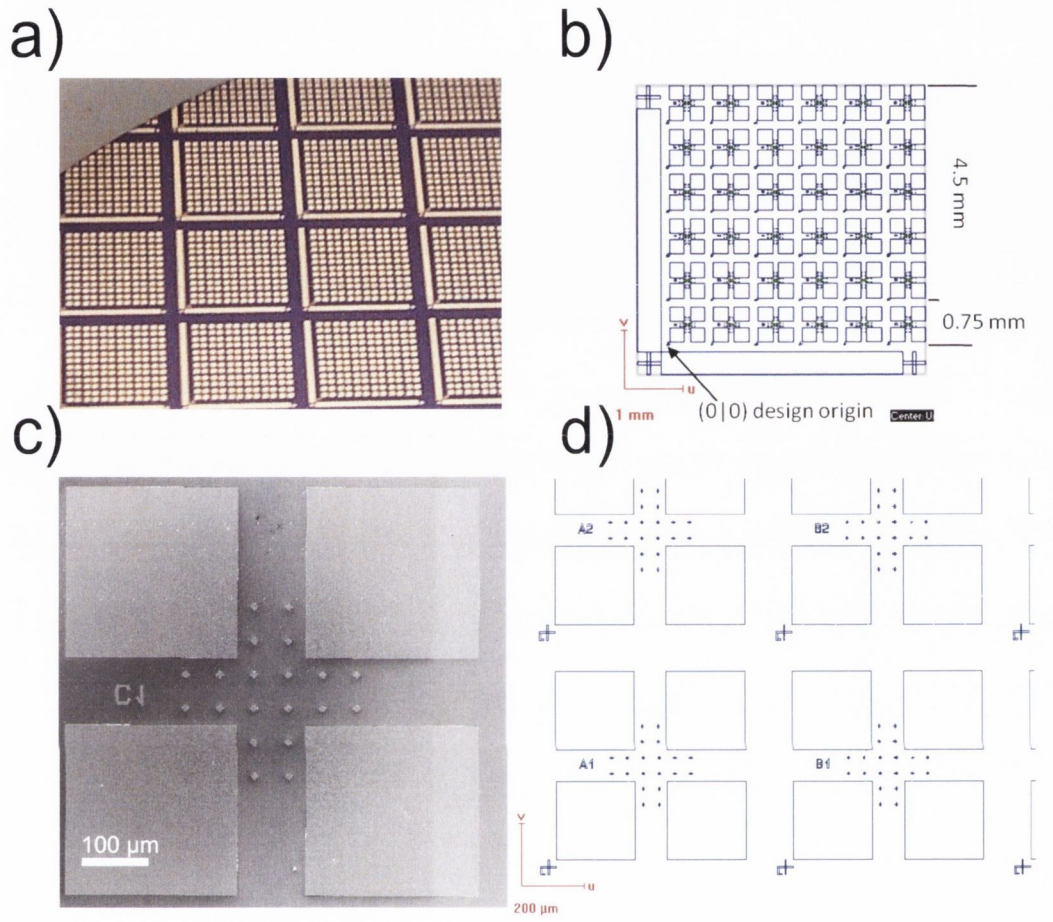

Figure 3.10: *(a) Optical image of substrate post UV lithography and metal deposition, (b) Schematic of the dimensions of the contact pads and alignment markers, (c) SEM inspection of the contact pads and alignment markers, (d) corresponding schematic of individual sites.*

3.2.3 Electron Beam Lithography - selective deposition

A combination of electron beam lithography and nanowire spray coating were employed to selectively deposit nanowires on a site specific area. Electron beam lithography was performed on a Zeiss Supra 40 SEM (Carl Zeiss) with a Elphy Plus (Raith) beam blanker. Firstly, windows were defined in PMMA e-beam resist. This enabled nanowires deposition in a predefined area. Spray coating was subsequently employed to deposit nanowires

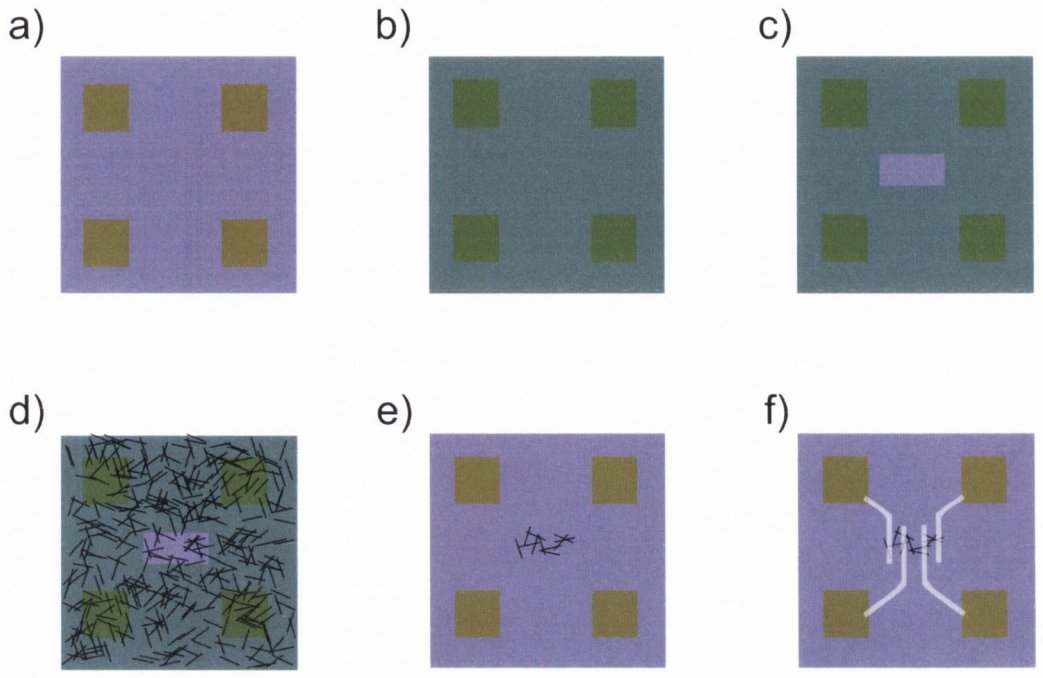

Figure 3.11: *(a) Large contact pads fabricated using UV lithography, (b) PMMA resist spin coated onto substrate, (c) EBL performed to open window to receive nanowires, (d) nanowires spray coated on substrate, (e) resist lifted off,* letterbox *of nanowires remain, (f) nanowires contacted to enable electrical measurements.*

onto the substrate and resist. Resist lift-off in acetone then removes any nanowires not adhering to the substrate. Nanowires remain where there was no resist, adhesion between the wire and substrate results in a *pseudo* negative resist pattern transfer of the wires, i.e. where the e-beam exposed the resist, nanowires remain.

Substrate Cleaning Substrates were sequentially washed in acetone and IPA, each for 5 minutes. To ensure the already fabricated contact pads and alignment markers remain adhered to the substrate, no sonication is employed during the cleaning process. Substrates are removed from the IPA and dried in a stream of N_2 gas.

Dehydration Bake A 3 minute 200 °C dehydration bake prior to resist spinning ensures no residual water remains on the substrate.

Resist Coating The chip was mounted on the spin coater. Vacuum suction ensures the chip remains on the spinner during the process. Approximately 200 µL of PMMA A3 was dispensed drop-wise onto the substrate. A 5 second dispense spin at 500 rpm ensures good coverage of the resist and a 3,000 rpm spin for 45 second ensures a uniform film of PMMA results. The thickness of the film can be tuned by altering the percentage of PMMA in the solvent or increasing/decreasing the spin speed.

Resist Baking The substrate is baked at 180 °C for 3 minutes, figure 3.11 (b). This baking serves two purposes; firstly it removes any residual solvent, secondly by baking the PMMA above its glass transition temperature of 100 °C it allows the PMMA chains to rearrange and release stress generated in the film during spin coating. An exposed and developed PMMA film will change its shape if there is any residual stress in the film from the spin coating process.[22]

EBL The substrate was transferred to the SEM chamber for EBL. Once vacuum was achieved, the beam current was read. Typical values for 10 kV and 10 µm aperture are 22 pA. The beam was finely focused to ensure well defined features. Confirmation of a finely focused beam was achieved by *burning a spot* on the resist for 5 seconds. An example is shown in figure 3.12. A sub 20 nm well rounded spot indicated a well focused beam that lacks stigmation. Exposure parameters of 10 kV accelerating beam voltage and dose 130 $\mu C/cm^2$ were used to expose windows of 50 $\times$ 200 μm^2. The exposed resist was removed by development of the resist in a solution of 1:3 MIBK:IPA for 40 seconds and IPA for 10 seconds, figure 3.11 (c). Resist windows now exist and the substrates are ready to receive nanowires.

3.2.4 Spray Coating

An art gun was employed to perform the nanowire spray coating, figure 3.13 (Evolution model, `www.germanairbrush.com`). For the spray coating of substrates, a nitrogen pressure of 1.5 bar was applied to the spray gun, a nominal distance of 5 cm was kept between substrate and spray gun. The spraying was performed in $\sim$ 100

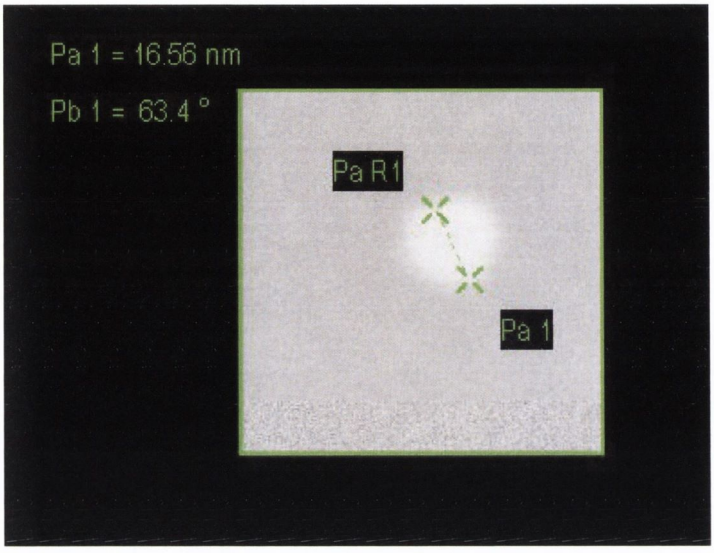

Figure 3.12: *Sub 20 nm contamination spot on PMMA.*

µl bursts. There was a delay of about 2 seconds between each aliquot of dispersion. This delay ensured any residual solvent had evaporated before the subsequent dispersion deposition, and hence, reduced the risk of any drying effects, such as clumping of nanowires. Inspection of nanowire networks was performed using an optical microscope in dark-field mode. Lift-off of the non-adhering nanowires could be performed once a satisfactory concentration of nanowires was present on the substrate. Lift-off in hot acetone removed any nanowires not adhering to the substrate, figure 3.11 (e).

3.2.5 Electron Beam Lithography - device contacting

Metal contacts to the nanowire networks were fabricated using EBL. The procedure is slightly altered from the selective deposition protocol. The substrate cleaning and preparation steps are identical. However the resist and exposure procedure were slightly altered to ensure nanowires do not become dislodged. PMMA A6 resist was used in place of PMMA A3. Resist spin-coating at 3,000 rpm resulted in a resist thickness of 150 nm whereas; A6 gave a resist thickness of 400 nm. The extra thickness of the A6 resist permitted a thicker film of metal to be deposited. For effective metal lift-off the

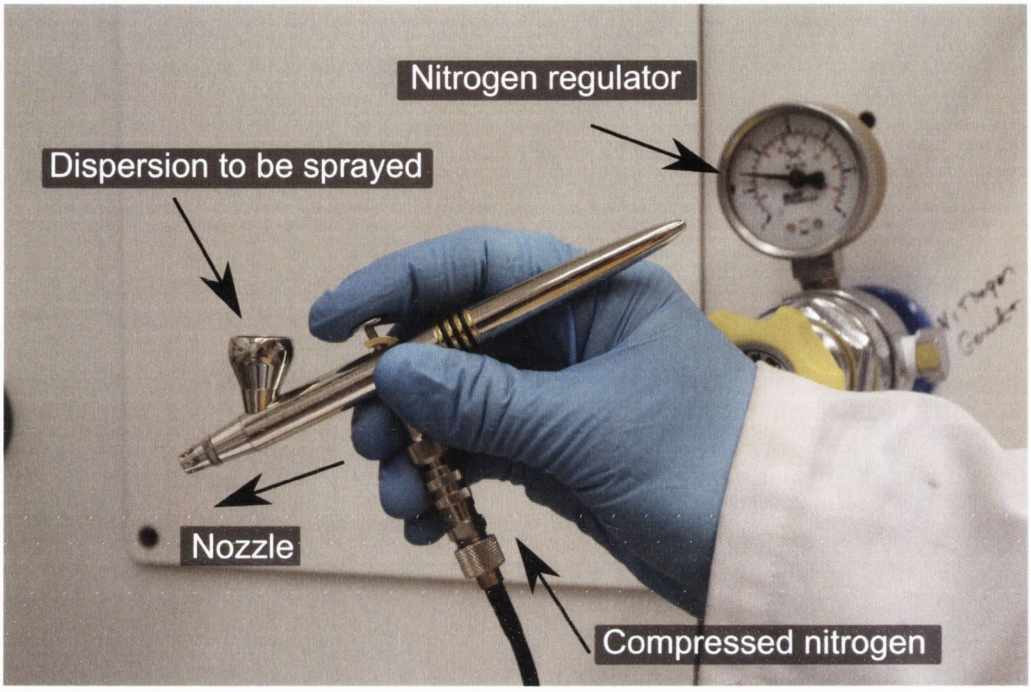

Figure 3.13: *Image of spray gun.*

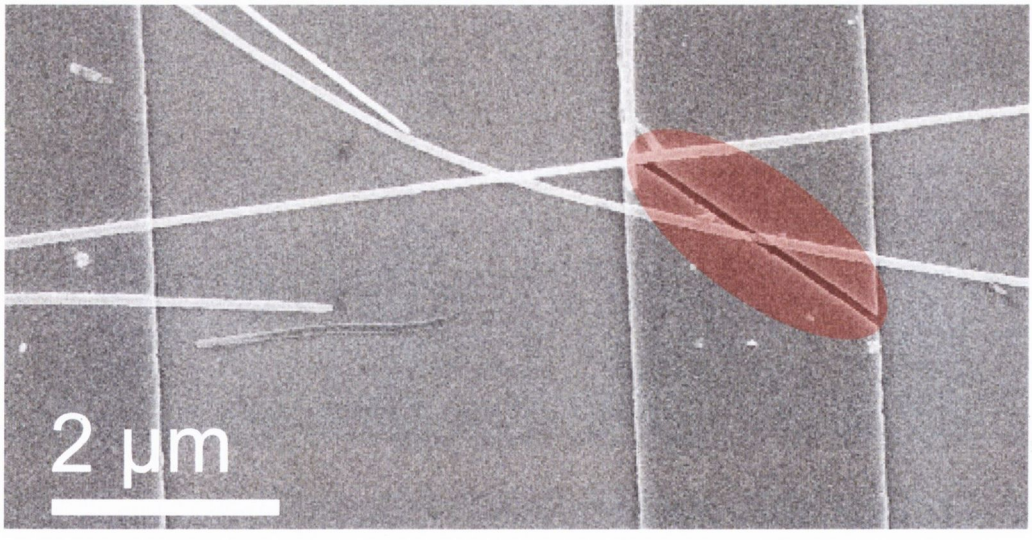

Figure 3.14: *Discontinuity in electrode due to lift-off of nanowire. This lithographic failure can be prevented by depositing more metal, this fully encapsulates the nanowires.*

thickness of the metal should not exceed half the thickness of the resist.[23] The increased electrode thickness ensured the wires were encapsulated within the metal, and as a result, did not become dislodged from the electrodes, which can cause a discontinuity in the electrode, as displayed in figure 3.14.

EBL was performed using a dose of 300 $\mu C/cm^2$ and an accelerating voltage of 10 kV. Electrodes with various spacing ranging from 10 µm to 100 µm were fabricated. After exposure, substrates were developed in 1:3 MIBK:IPA solution for 45 seconds and washed in IPA for 10 seconds before being dried in a stream of N_2 gas.

Metal deposition took place in a Temescal FC-2000. Nickel was deposited at a base pressure of 1×10^{-6} mbar and a rate of 1 Å/second. Lift off takes place in heated acetone for 1 hour. Substrates are then removed and washed in IPA and dried with N_2. No further processing steps are required and the nanowires are ready to be electrically characterised.

3.3 Electrical Characterisation

Electrical characterisation of the nanowire networks was performed on a Karl Suss probe station, figure 3.15. All measurements were performed in ambient conditions. Tungsten needles, tip diameter $\sim$ 20 µm, attached to micromanipulators enabled precise probing of the metallic contact pads, figure 3.15 (b). An optical microscope with x10 and x50 magnification assisted in locating specific contact pads. DC voltage was sourced with a Keithley 2400 sourcemeter. The readout of the current was obtained with a home built LabView program with a Keithley 2000 system, 3.15 (c).

Current limiting compliance, to prevent dielectric breakdown during the forming and set process, was manually entered into the sourcemeter. For all measurements the voltage was swept with the current measured. The voltage starts at zero volts, sweeps up to $+V_{max}$, back to zero, to $-V_{min}$ and back to zero. The quantity of data points to be acquired was defined in the LabView program as well as the dwell time on each data acquisition point.

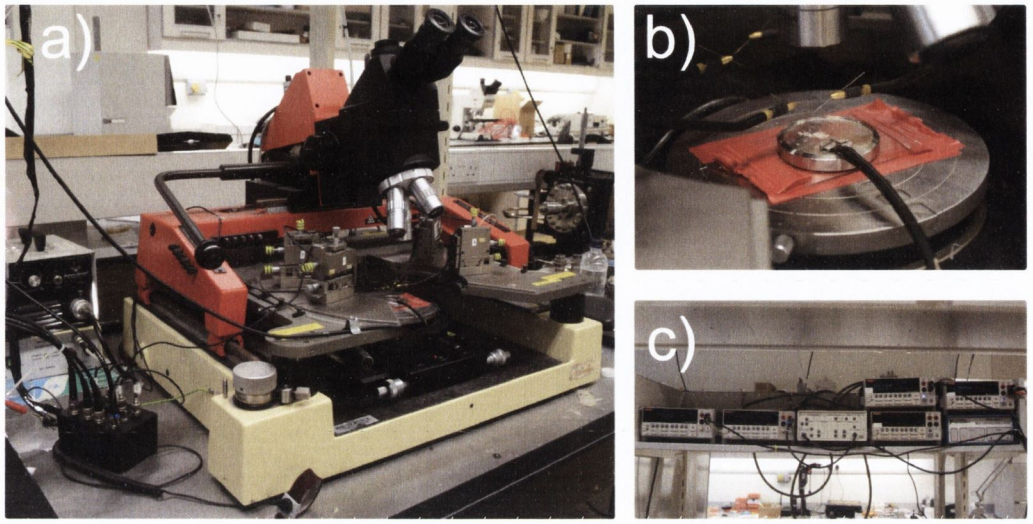

Figure 3.15: *4 probe, electrically isolated Karl Suss probe station.*

Here in this chapter we have introduced the techniques and processes involved in fabricating nickel nanowire network devices. The next chapter examine the electrical characteristics of these nickel nanowires networks, such as SET and FORM length dependance and ON/OFF ratios of the devices.

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4

Electrical characterisation of nickel nanowire ReRAM devices

THIS chapter presents an investigation on the electrical resistance switching behaviour of nickel nanowires in a sparse network. The FORM, RESET and SET operations associated with the operation of these networks as memory devices are described, as well as the dependence of the device operation on the distance separation between the electrodes for that device.

4.1 Introduction

The requirement for increased computation speeds necessitates the development of next generation of memory storage devices that offer a significant increase in performance over present generation static/dynamic/flash random access memories. This requirement entails higher switching speed, smaller dimensions, and hence, higher density memory, greater endurance, as well as lower cost and lower power consumption. Several technologies have emerged as potential candidates, however, Resistance Random Access Memory (ReRAM) offers properties that best match the characteristics of the ideal next generation memory. These memory devices are comprised of a multi-layer sandwich of metal-insulator-metal. The insulator acts as the switching material and contains the metallic filament that enables the switching between OFF and ON states. ReRAM devices have already shown excellent performance, highlights include: operation

currents below 50 μA[1], 10^6 set/reset operations,[2] 10^{12} reading cycles,[2] data retention time $> 10^6$ s[3] and switching time $\sim$ 10 ns.[4]

ReRAM operation is based on a resistance switching phenomena in which the reversible growth of a conductive metallic filament creates a bridge across the non-conducting oxide to form a connection between the two metal electrodes in the planar device. Switching is induced by the applied electric field which causes metallic atoms from one electrode to electromigrate across the insulating region to create a filament that switches the resistance from a high resistance state (HRS) to a low resistance state (LRS).

Although resistive switching (RS) behaviour has been observed for over 50 years,[5] a full understanding of the mechanisms involved is still lacking. Various types of switching phenomena have been reported, but the exact mechanism appears to depend on the nature of the oxide and the electrodes. These mechanisms include, but are not limited to: trap charging in the oxide,[6] space charge-limited conduction processes,[7] Joule heating,[8] and electrodeposition.[9]

A variety of materials have been used in ReRAM based devices, these include perovskite-based oxides,[10;11;12;13] chalcogenides,[14;15;16;17;18] and transition metal oxides, including TiO_2,[19] NiO,[20;21] Nb_2O_5,[22] Al_2O_3,[23] CoO,[24] SnO_2,[25] and Ga_2O_3.[26] This work will concentrate on the conductive filament formation in nickel oxide core-shell nanowire networks. In contrast to earlier reports, which involve planar device geometries, we focus on the development of ReRAM devices based on random nanowire (NW) networks. This approach has the advantage of straightforward fabrication, but not requiring the complex lithography used in conventional sandwich devices, as well as offering the potential for higher ON/OFF ratios, with minimal leakage currents necessary for memory applications.

4.2 Unipolar resistive switching characteristics

Networks of nickel nanowires contacted by metal electrodes make up the ReRAM devices. Each wire-wire junction is comprised of an insulating metal-oxide-oxide-metal junction.

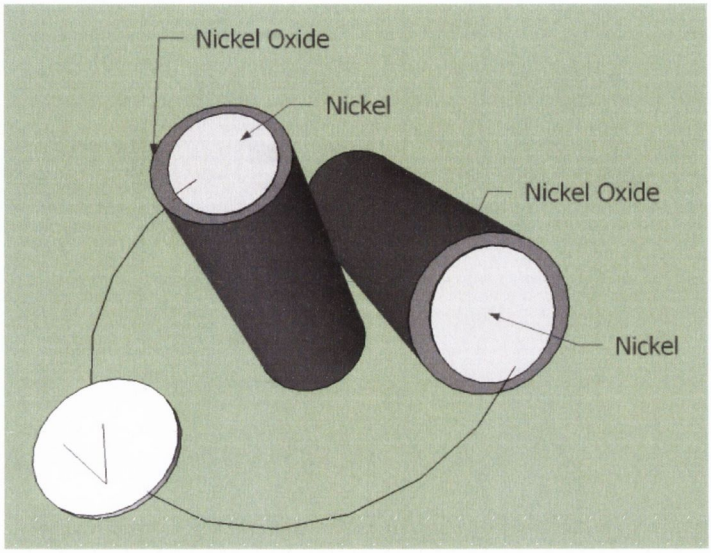

Figure 4.1: *Schematic of a crossed nanowire-nanowire junction. To complete the circuit a conductive filament needs to the bridge the two shell layers of insulating oxide.*

A schematic of a wire-wire junction is displayed in figure 4.1. Figure 4.2 is reproduced from chapter 1 and provides a description of various memory operations.

Each of the wire-wire junctions spanning the channel need to be switched to a LRS for the overall device to exhibit a LRS. As fabricated devices comprised of core-shell nickel nanowire based networks are in the HRS. These devices need to be FORMED to attain a LRS. The FORMING process is described in the following section and involves the establishment of a collective set of conductive filaments (CF) bridging the full width of the oxide, whereas, subsequent set operations refer to the rejuvenation of one or more CF in this bridging path.

4.2.1 FORM operation

An important first step in the activation of any ReRAM device is the FORM operation. FORMING is the initial step to transform the device from a HRS to a LRS. FORMING is achieved by applying a compliance current to the sourcemetre, a Keithley 2400. The compliance current limits the maximum current that can flow across the device. The selected current compliance value is important, since selecting too low a value and

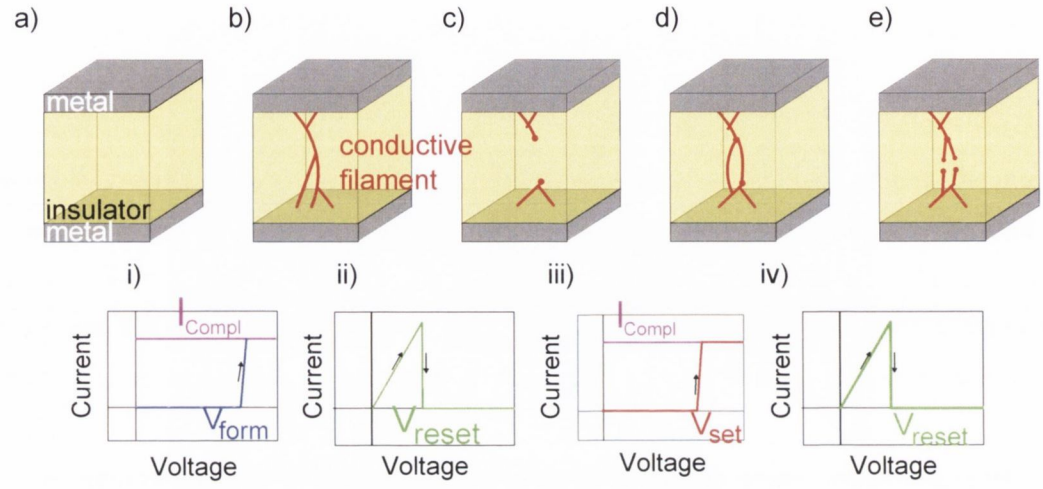

Figure 4.2: *Schematic of filament formation (a) - (e), corresponding current-voltage curve (i) - (iv). (a) metal-insulator-metal in virgin state, (i) current-voltage operation to form device, an abrupt increase in current indicates filament formation, (b) after forming operation, the insulator is bridged by a conductive filament, (ii) reset operation to transform device from an ON to OFF state, compliance is removed and voltage is increased, an abrupt decrease in current indicates filament has been ruptured, (c) schematic of filament rupture, note that only a discontunity in filament is observed, a large portion of the filament remains, (iii) set operation to transform device from OFF to ON state, a compliance current is applied and voltage is ramped up until an abrupt increase in current is noted, (d) filament formation has occurred and device is ON, (iv) reset operation to return device to OFF state, (e) filament rupture.*

threshold resistive switching* will be observed, too high a value and catastrophic breakdown and even melting of the nanowire will be observed. The current voltage curve in figure 4.3 (a) shows a sudden rapid increase associated with the forming process. An SEM image of the device is shown in figure 4.3 (b). Two nickel electrodes are observed at the exterior of the nanowire network and enable electrical characterisation of the device. A compliance current of 5 μA was applied to the source meter. The voltage was swept between the two electrodes at a rate of 0.5 V/s. The abrupt jump in current

*Threshold resistive switching has only one stable resistance state at zero bias, a HRS, but switches between HRS and LRS states at finite bias, and will be presented in Chapter 6.

represented a transition from a pristine HRS ($\sim$ 182 MΩ) to a LRS (1.6 MΩ). The transition occurs 8.15 V, which is referred to as V_{form}. This initial FORMING step is required to establish conductive filament(s) through the nickel nanowire network, which involves formation of metal filaments bridging the insulating oxide. Subsequent READ and RESET operations can now be performed.

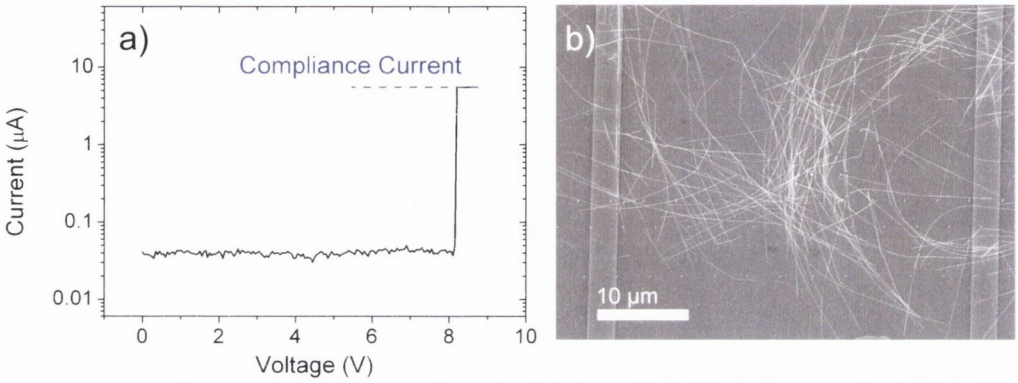

Figure 4.3: *(a) FORMING characteristics a 40 μm long channel of nickel nanowires, the y-axis is a log scale (b) SEM image of device used for electrical measurements in figures 4.3 (a), 4.4, & 4.5.*

During the FORM operation, conductive filament form and bridge the insulating oxide at each nanowire-nanowire junction spanning the conducting paths between the electrodes. This results in a distance dependence behaviour of the forming voltage. This length dependence will be investigated in Section 4.4. As the separation of the channels increases, there is an increase in the number of wire-wire junctions that need to be switched on. We expect to see a length dependence of the FORMING voltage on the electrode separation.

4.2.2 RESET operation

The RESET operation transforms the device from a LRS to a HRS. The exact mechanism of the filament rupture is not fully understood. One possibility is that the conductive

filament rupture is due to a thermal effect, i.e., heat assisted ionic diffusion or joule heating.[27;28]

For larger ReRAM cells, $\geq 1 \times 10^{-9}$ m^2, the RESET operation induces large currents in the conductive filament, but the remaining insulating layer is not subject to these. In the case of nanowire networks, small contact areas are involved and as a result of these high current densities, wire failures may occur in some instances.[†]

To accomplish the RESET operation, and transform the device from a LRS to a HRS, one or more conductive filaments needs to be ruptured. As opposed to the SET and RESET operations, no compliance current is applied and the voltage is swept until an abrupt decrease in current is observed. Voltage is ramped at a rate of 50 mV/step and 0.5 V/s. The low bias resistance is 5.6 kΩ and at a voltage of 3.3 V an increase in resistance to 60 MΩ is observed, figure 4.4 (a). V_{reset} is noted as 3.3 V.

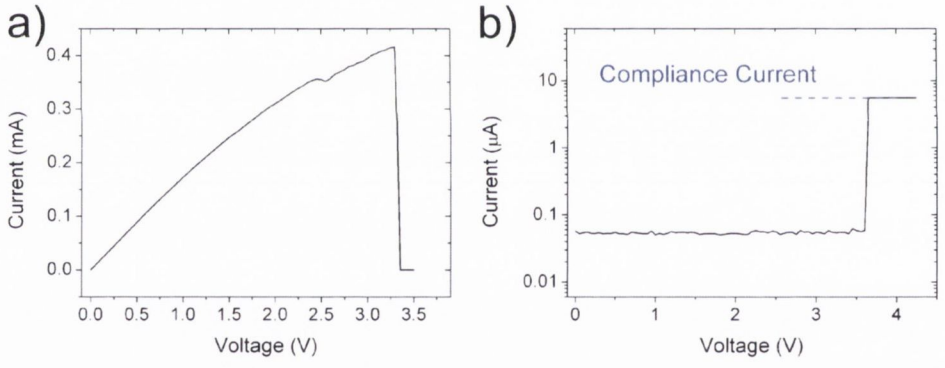

Figure 4.4: *RESET (a) and SET (b) operations, with the SET operation shown on a log linear plot.*

While sweeping the voltage to perform a RESET operation, a temporary deviation from the LRS is often observed, an example of this deviation is displayed in figure 4.5. The origin of this fluctuation in the resistance of the metallic filament contributing to the LRS is unclear. One possible explanation is the diffusion of metallic nickel atoms away from the conductive filament, which is followed by an enhanced electromigration

[†]contact area for two crossed nanowires at 90° in contact is 2πRD,[29] where R is the radius of the nanowire and D is the separation, we obtain a contact area of 56.5 nm^2. This combined with a reset current of 400 μA results in a current density at the contact point of 7.2 A/μm^2.

due to the high E field which subsequently restores the filament. In figure 4.5 a RESET operation is displayed; at a voltage of 0.8 V an increase in the resistance of an order of magnitude is observed, and the device returns to the original LRS value at 1.2 V.

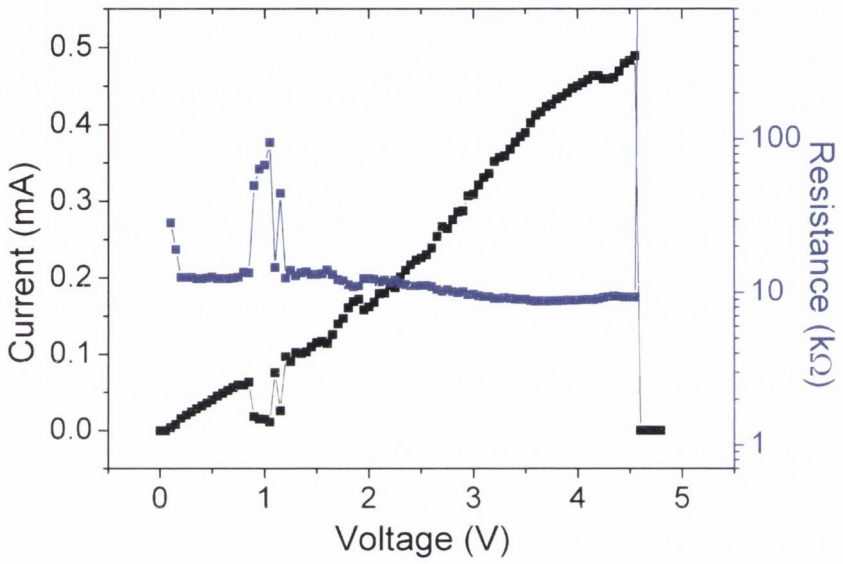

Figure 4.5: *Reset operation of a nickel nanowire ReRAM device. Current is plotted on the left axis, and a resistance value is plotted on the right axis using a log scale.*

A definitive reason for these brief fluctuations in resistance is unclear; however future work in this area will concentrate on *in situ* TEM analysis while performing switching operations. This will enable the real-time monitoring of conductive filament formation and rupture.

4.2.3 SET operation

After a RESET operation the device is in an OFF state, returning it to an ON state requires a SET operation. SET operations are similar to forming except that typically $V_{set} < V_{form}$. A schematic that provides a possible explanation is displayed in figure 4.6 (a & b). However, in the event of nanowire failure, figure 4.6 (c), the pathway of conduction is altered and the necessity of a new conductive pathway results in a

new forming step taking place. The change in the conductive path way can result in

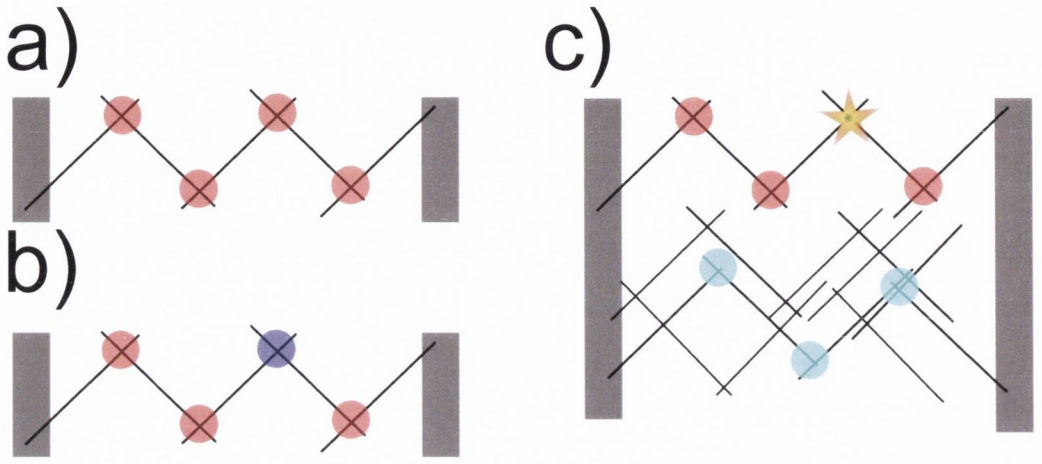

Figure 4.6: *(a) the initial form has to construct a conductive filament in 3 wire-wire junctions, indicated by red circles, (b) the following SET operation only has to construct a conductive filament in a single wire-wire junction, indicated by a blue circle, (c) in the event of a catastrophic failure of a nanowire, indicated by a yellow star, an alternate pathway is found, however new wire-wire junctions have to be set, resulting in V_{set} being increased.*

subsequent SET operations requiring a higher voltage than the initial V_{form}. The SET operation requires a compliance current of 5 μA to prevent catastrophic failure of the device. A SET operation, figure 4.4 (b), returns the device to a LRS, V_{set} is 3.6 V.

4.3 Memory Window of HRS and LRS

The memory window of a device is the ratio between the two memory states, HRS and LRS. The larger the memory window, the lower the chance of mis-reading the state of the device. A nanowire network device was repeatedly cycled between ON and OFF states. A plot of HRS and LRS resistance is shown in figure 4.7. The HRS shows little fluctuation throughout the duration of the cycles. The only cycle to cause a *mis-read* was due to a failed filament rupture in a RESET process. There are two possible causes; either the filament ruptured and SET in the process of removing the applied bias, or there

was a second conductive filament partially or completely bridging the oxide. However, upon the next SET-RESET operation the device returned to normal operation. There

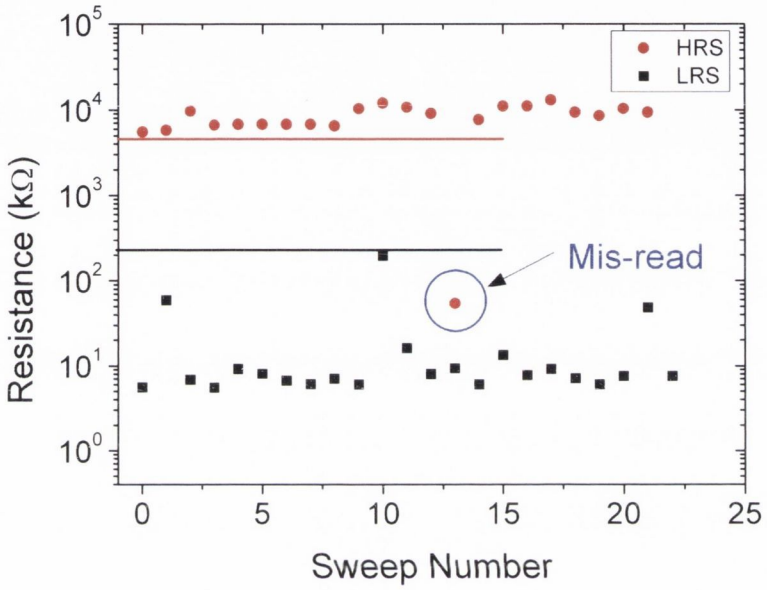

Figure 4.7: *The switching resistance at a read-out voltage of 0.3 V.*

are also three occurrences when the device is in a LRS but deviating from the LRS average. This is likely caused by poor filament formation. Even with these mis-reads there is still a large difference between the average LRS and HRS. The black and red lines in figure 4.7 show an operating window of approximately one order of magnitude.

The actual magnitude of the window between the LRS and the HRS was obtained by performing low bias current-voltage measurements. Initially the device was in a LRS, black curve in figure 4.8, and had a resistance of 1.45 kΩ. 20 sweeps were performed in order to verify the metallic nature of the filament. The device was RESET and was in a HRS. Low bias IV measurements were performed and no current was detected, indicating the current is sub pico amp.‡ In order to verify that the device had not catastrophically

‡Such low currents are not obtainable in the SET process due to limitations on the pre-amp attached to the source meter

failed, a SET operation was performed and indeed the device returned to a LRS with a resistance of 2.2 kΩ, as indicated by blue curves in figure 4.8.

The measured resistive switching curves are shown in figure 4.9. The figure shows the typical unipolar resistive switching behaviour of NiO and are typical of reported values in the literature.[27;30;31] Little deviation is observed from V_{set} and V_{reset} over the course of 20 cycles, indicating that the same pathway is contributing to the conductance channel. The FORMING voltage is significantly larger than any of the SET voltages, indicating many wire-wire junctions were transformed into a LRS during the form step. The SET voltage at 3.5 V is the approximate value we obtained for single wire-wire junctions.

4.4 Investigation into length dependence for FORMING and SET voltages

In order to verify the FORMING and switching properties of nickel nanowire networks four different channel lengths were fabricated. Varying the channel length of the nanowire network should result in an increased FORMING voltage. This increase in FORMING voltage should scale with the inter electrode distance for a given electrode width. The

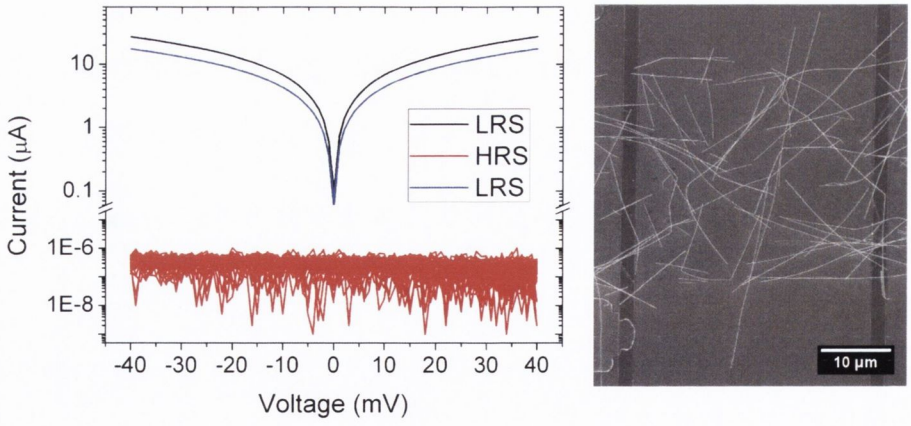

Figure 4.8: *Low bias log-linear plots of ReRAM device. All measurements were performed 20 times. (right) SEM image of device*

expectation is that the SET voltage for the varied channel length should remain independent of electrode spacing, if the formation of a conductive filament involves the repair a single nanowire/nanowire junction.

4.4.1 Device Fabrication

Nickel nanowires were fabricated in the same manner as those described in section 3.2.5, however the channel spacing is varied. Channel lengths of 10, 20, 30 and 40 μm are fabricated on the nanowire networks. The approximate density of nanowires in the channel was kept constant. The V_{form} and V_{reset} values are plotted in figure 4.10, along with linear fits of the respective data. There is a minor difference in slope between the two sets of data. The V_{set} data shows weak distance dependence, a linear fit describes the data as 0.05 V/μm + 3.2 V. This result is in agreement from the SET data presented in figure 4.9, where the SET values are centred around 3.5 V.

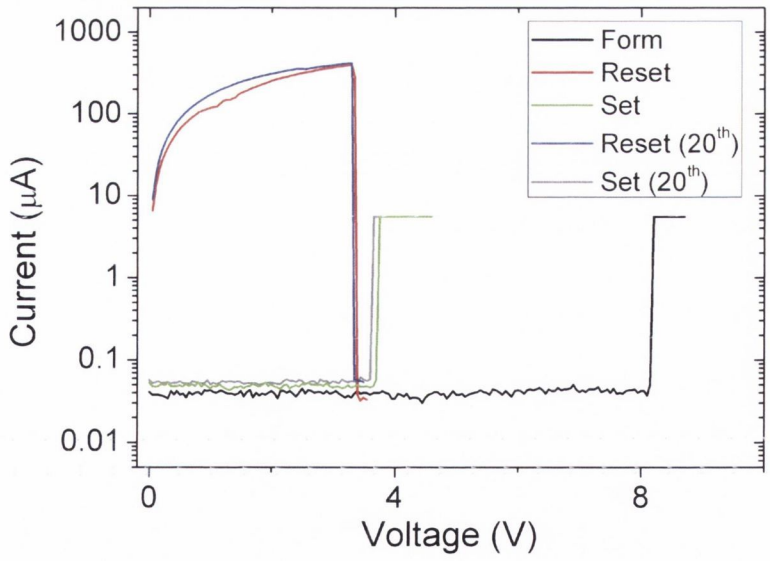

Figure 4.9: *Normal switching behaviour of typical device. Current voltage measurements are shown on a log-linear scale. Set and reset operations after 20 sweeps are shown. No degradation of device is observed.*

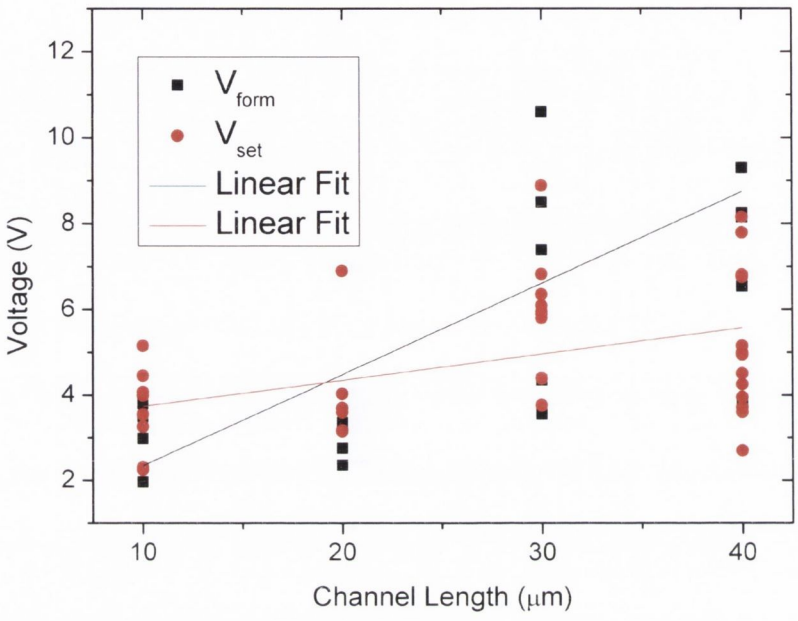

Figure 4.10: *V_{form} and V_{set} values for four different channel lengths. Linear fits are plotted for the respective values.*

The V_{form} values increase at a rate of 0.16 V/μm + 1.1 V. The increase distance dependence can be attributed to the requirement for conductive filament formation in each nanowire-nanowire junction, whereas, a SET operation only requires conductive filament formation in a single wire-wire junction.

The higher V_{set} value in the 20 μm channel data-set can most likely be attributed to a nanowire catastrophically failing in the previous reset operation and the subsequent SET operation requiring the formation of a new pathway.

4.5 Individual Nanowire Resitive Switching Data

A pair of crossed nanowires were contacted to verify resistive switching was occurring across the nanowire-nanowire junctions. This was achieved using a novel directed self

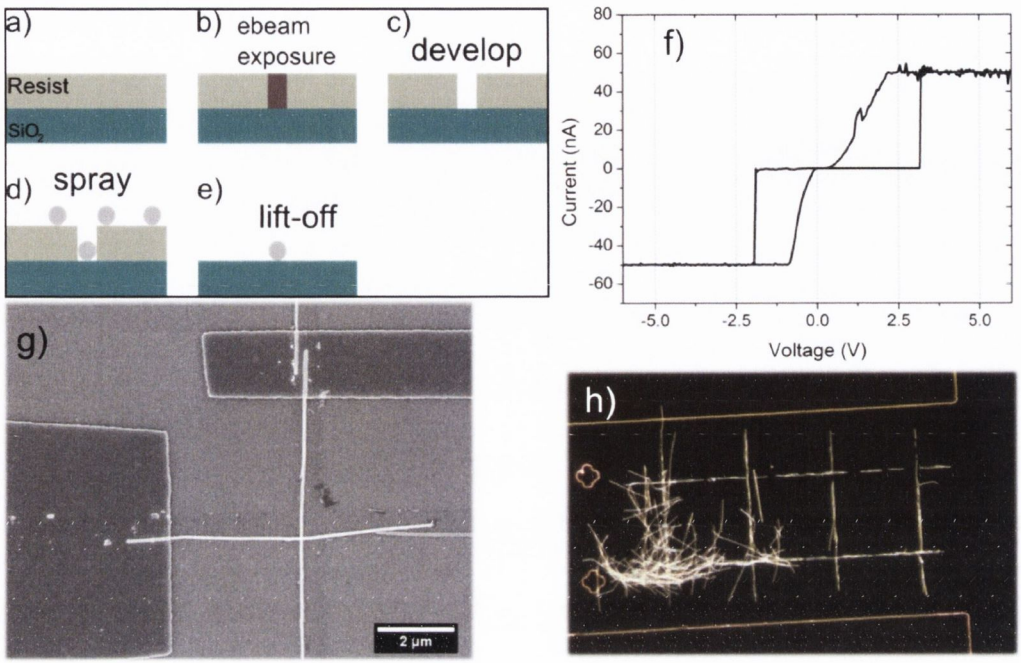

Figure 4.11: *(a) - (e) Schematic showing steps required to achieve nanowire directed self-assembly, (f) FORM curve of the device, (g) SEM of crossed wires , (h) Optical image showing wires in darkfield mode*

assembly technique. Substrates identical to those presented so far were used to perform measurements, these contained pre-patterned electrodes fabricated using UV lithography.

PMMA resist was spin coated onto the substrates. EBL was then performed to open crossed trenches where nanowire deposition was desired. Ideally nanowires would bridge the crossed area of the resist. These trenches were just wider that the diameter of the batch of nanowires used, $\sim$ 100 nm. After developing the resist, figure 4.11 (c), a depression in the resist remained, nanowires could then be sprayed onto the resist covered substrate, figure 4.11 (d). The resist could be removed by an acetone wash, where wires adhered to the substrate in the trench they remained, those on top of the resist were removed in this step. A subsequent EBL step and metalisation were performed to contact the wires and enable electrical characterisation.

A FORM operation is displayed in figure 4.11 (f) shows an abrupt increase in current at 3.2 V. This FORM voltage of 3.2 V is similar to the SET voltage observed for a

nanowire network in figure 4.4 (b) of 3.5 V, indicating that during the SET operation only one nanowire-nanowire CF is being rejuvenated. An SEM image showing the device is presented in figure 4.4 (g) along with a darkfield optical microscope image in figure 4.4 (h).

4.6 Conclusions

Nickel nanowires were deposited on insulating silicon substrates and contacted for electrical characterisation. Using a current limited voltage sweep, the network could be transformed from a high resistance state to a low resistance state. The devices exhibited a large on/off ratio, or memory window, of 7 orders of magnitude at low-bias. After 20 on/off cycles the devices showed no signs of degradation. A distance dependence on the initial SET operation or FORMING of the device was shown as well as a smaller distance dependence for SET operations.

The next chapter will investigate the modification of nickel nanowires using ambient thermal annealing. Rather than nanowire networks, resistive switching in individual nanowires will be investigated.

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5

Controlled oxidation of nickel nanowires for in wire ReRAM cells

5.1 Introduction

THE necessity to keep up with the scaling requirements of Moore's Law requires smaller and smaller nanometre regime sized features to be fabricated. As the limit of present lithography methods are being approached, a departure from top down to bottom up fabrication of devices will be required. Chapter 3 described the fabrication of ReRAM devices based on nickel nanowires spray coated onto a substrate, and subsequently contacted by metal leads and their electrical properties characterised and presented in detail in Chapter 4. These memory devices exhibited footprint dimensions spanning tens of microns. Whilst understanding the switching mechanisms and electrical characteristics exhibited by networks of nickel nanowires is of great interest to the resistive switching research community, these large dimensions preclude the device from ever being mass-producible and wafer scalable. To address this scalability issue, controlled oxidation of individual nanowires will utilise the Kirkendall effect[1] in nickel nanowires to enable fabrication of ReRAM cells with sub-micron dimensions. The Kirkendall effect is the motion of the interface between two metals or materials that occurs as a result of the difference in diffusion rates of the atoms that comprise these materials. The Kirkendall effect has garnered much attention recently with regard to its role in the modification of nanomaterials.[2;3;4;5;6]

The first experiment to demonstrate this effect was performed by Kirkendall in 1942[7] and the result was confirmed in an independent experiment in 1947.[1] Copper and brass were used as the diffusion couple in these early experiments. The metals were welded together and subjected to elevated temperatures. A movement of the brass-copper interface was observed, in which zinc diffused into the copper faster than copper into the brass. Excess migration of atoms can give rise to void formation near the interface and within the fast diffusion medium.[8;9] As recently as a decade ago, the Kirkendall effect was considered to be an undesirable phenomenon. Formation of Kirkendall voids deteriorates the adhesion strength of bond-pad interfaces and may cause wire bond failure in chip carriers. These problems can be avoided by the introduction of a diffusion barrier material such as tantalum. However, in 2004 chemists applied this void formation mechanism to selectively generate hollow nano-structures.[2] This synthetic route offers great potential for fabrication of hollow structures in various material systems, structures that have applications in areas such as drug delivery,[10] plasmonics[11] or bioencapsulation.[12] Here we will use this methodology to introduce voids into nickel oxide nanowires to assist in the isolation of resistive switching cells.

In 2011, González *et al.*[3] published work showing exceptional control and selectivity for spherical, cubic and cylindrical topologies. A combination of galvanic exchange and Kirkendall growth were employed to realise various topologies. The results of this work are displayed in figure 5.1. Here we adopt a different procedure, rather than using a wet chemistry approach, diffusion of nickel atoms will be achieved exclusively using a dry thermal process. As has previously been reported,[5;13;14] void formation in nickel nanowires occurs when nanowires are subjected to thermal annealing in an ambient atmosphere.

The mechanism for void formation by heating in ambient is shown in figure 5.2. For nickel-nickel oxide core-shell nanowires, figure 5.2 (a) shows that the faster diffusion of the nickel atoms out into the oxide will generate vacancies in the core. These vacancies ultimately interact and accumulate in the core of the nanostructure, figure 5.2 (c). This vacancy accumulation gives rise to the formation of a hollow void in the nanowire; figure

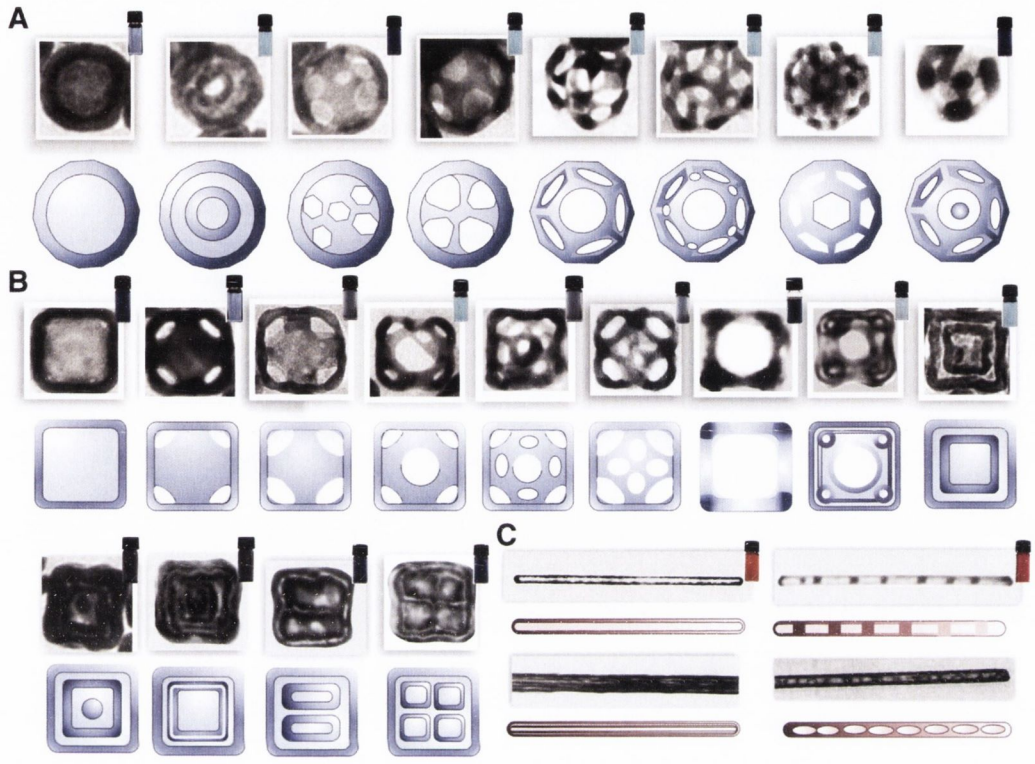

Figure 5.1: *Various nanoparticle modifications using the Kirkendall effect, with (a) spherical, (b) cubic and (c) cylindrical topologies. The schematic of the desired structure is below the accompanied TEM image. Reproduced from the work of González* et al.[3]

5.2 (d).[15] We believe this is the first attempt to alter nanowires using the Kirkendall effect and to subsequently characterise their properties electrically.

The bulk of this chapter will focus on the deposition of nickel nanowires onto insulating substrates, figure 5.3 (a), controlled thermal annealing of nickel nanowires, figure 5.3 (b), and subsequent lithographic contacting, figure 5.3 (c). Metallic electrodes will be fabricated on the wires to enable electrical characterisation of the oxidised wires and the voids contained therein. EDX and TEM will be used to characterise the structural and material properties of the nanowire and voids.

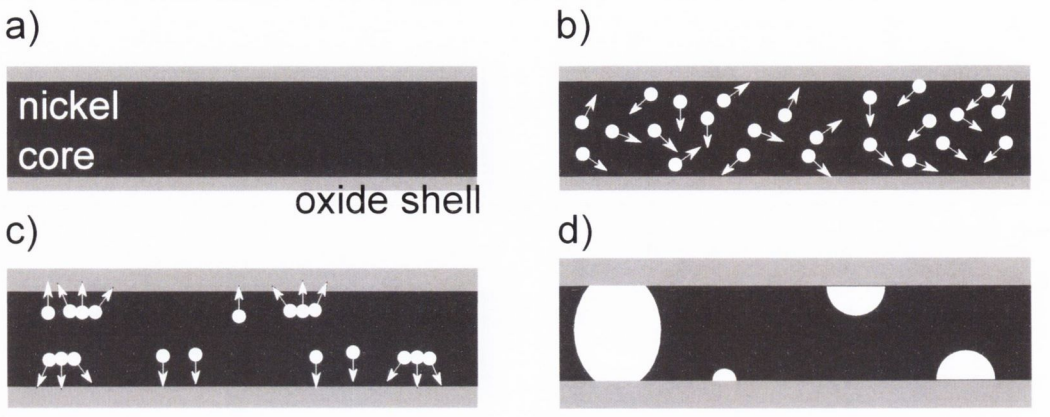

Figure 5.2: *Schematic showing diffusion and agglomeration of voids during anneal, note an increase in the shell oxide thickness during anneal process.*

5.2 Ambient Annealing

The desired topology for ReRAM cells is contained within a single nickel wire involves the formation of voids in the metallic core to create individual isolated discrete sections of conductive and switchable material, while at the same time ensuring the oxide shell remains intact. The core of the wire acts as the conductive element, with the insulating shell acting as the switching material. The presence of the voids in the core of the wire prevents leakage along the length of the wire separating and isolating memory elements from each other.

This void-core based structure in the core of the wire is attained through a thermal anneal in ambient atmospheric conditions. A highly dilute 5 µl solution with nanowire concentration of 0.1 mg/ml of nickel nanowires was drop cast on silicon coupons 1 × 1 cm that had been subjected to an oxygen plasma prior to any nanowire deposition to remove any contaminants on the substrate.

Thermal annealing of the nanowires was performed in a Carbolite 800 Afterburner ashing furnace, figure 5.4. All anneals took place in an ambient atmosphere with no gas flow. The wires were subjected to various annealing temperatures, ranging from 350 to 600 °C, and times varying from 3 to 120 mins, to establish the best ideal conditions for void formation in the core of the nickel nanowire. Substrates were then imaged in

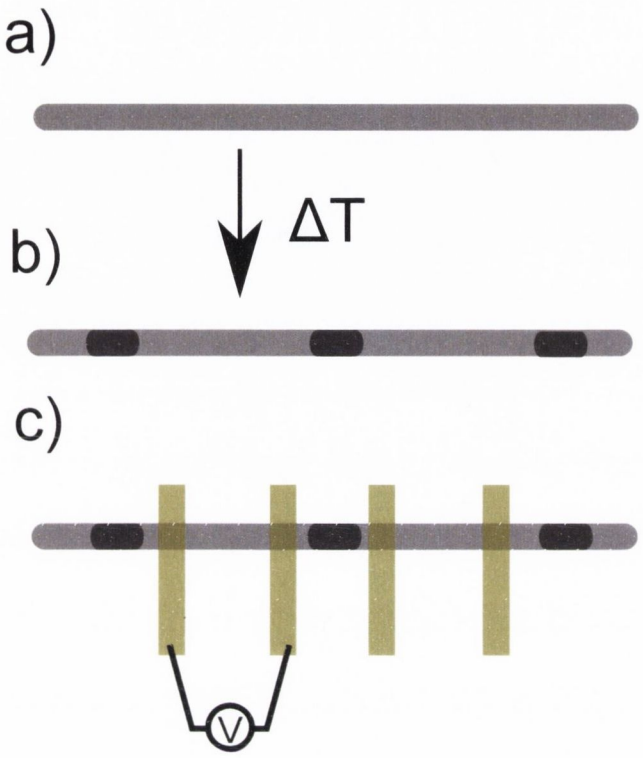

Figure 5.3: *Experimental scheme for characterisation of voids within nickel nanowires. (a) nanowires drop cast onto silicon substrate, (b) thermal anneal is performed to create voids within the nanowire core, (c) metallic contacts fabricated to enable electrical characterisation.*

an SEM to examine changes to the wire's morphology as a result of the thermal anneal process.

Figure 5.5 displays a results matrix of the anneal processes with various temperatures and times. No observable changes to the wires were observed for anneal times of 20 minutes or less at a temperature 350 °C. Slight roughening of the wires was observed for longer anneals at 350 °C and moderate length 10 and 20 minute anneals at 400 °C. The formation of a NiO bamboo-like structure was observed at an anneal temperature of 600 °C and above. The bamboo morphology is not useful for the purpose of a resistive switching conductive cell, due to the absence of any kind of conductive metallic core, which is necessary for switching. The desired anneal result involves void formation in the

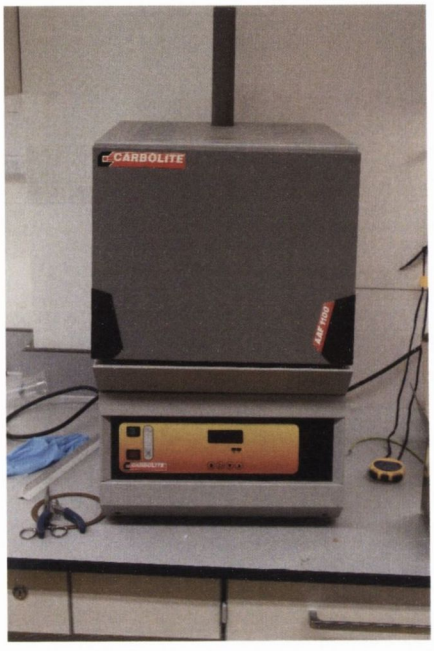

Figure 5.4: *Carbolite Furnace used for the nanowire anneal process.*

core of the nanowire, whilst leaving the shell in a uniform, non-bamboo like state. An anneal temperature of 450 °C and time of 120 minutes were identified as being optimum for controlled void formation in nickel nanowires. These conditions agree with previous reports[5;16] for void formation in nickel nanomaterials.

Figure 5.6 (a) displays an SEM of nickel nanowires annealed at 450 °C for 120 minutes. A TEM image of a nickel nanowire after a thermal anneal in the same conditions is presented in figure 5.6 (b). A clear brighter section of the wire is observable in the centre of the image; this area is the void where nickel has diffused to the NiO shell of the wire. The signature of the nanowire shell in the void region is amorphous, indicating nickel has diffused and an insulating void remains. There are also areas where minimal diffusion has occurred and the metallic core of the nanowire remains. This nickel will make up the resistive switching material once the wires are contacted via a combination of UV-lithography and EBL to enable electrical characterisation.

An inspection of 30 wires annealed at 450 °C for 120 minutes provided statistics for the average metallic core *cell length* and the vacant core *void length*, at 340 $\pm$ 117 and

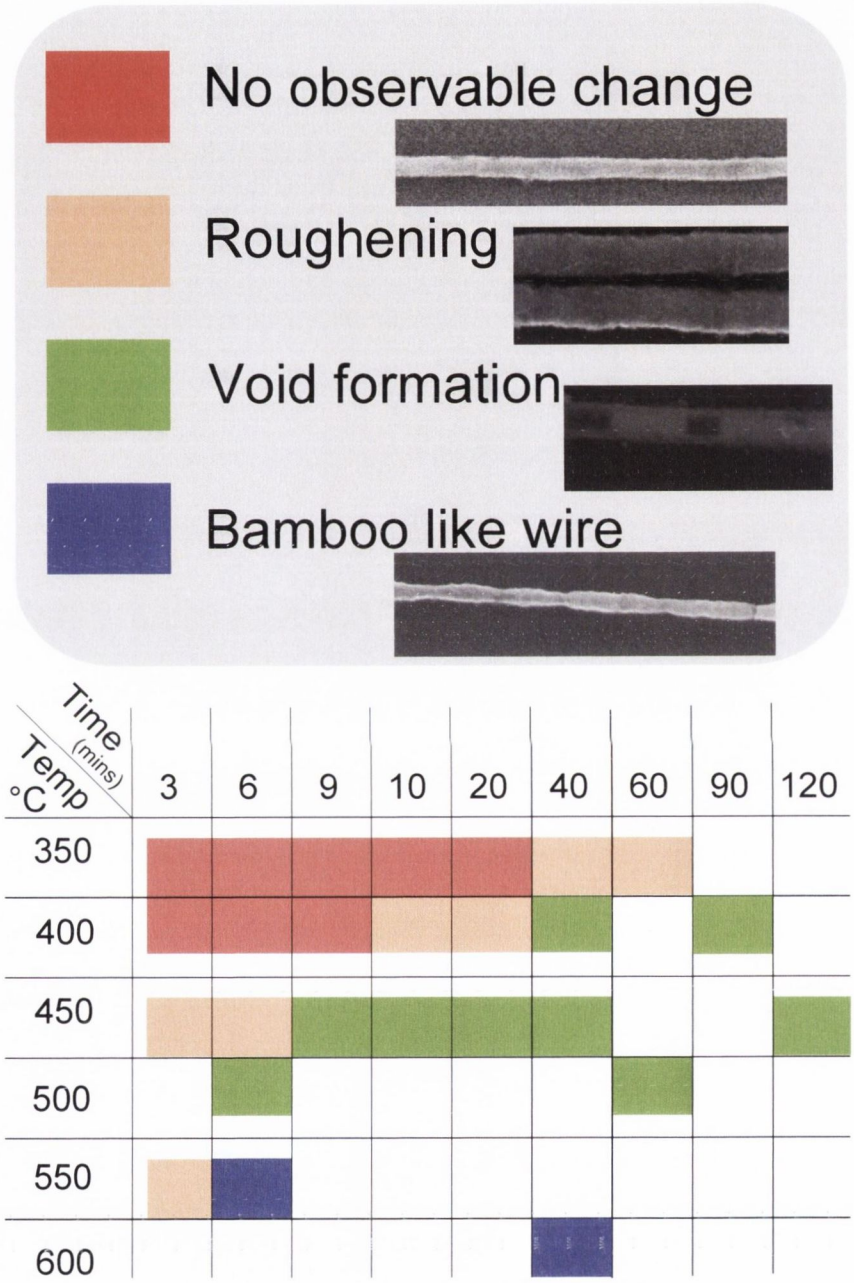

Figure 5.5: *SEM micrographs illustrating the various wire morphologies obtained and table displaying the anneal time and temperature required to obtain corresponding morphology.*

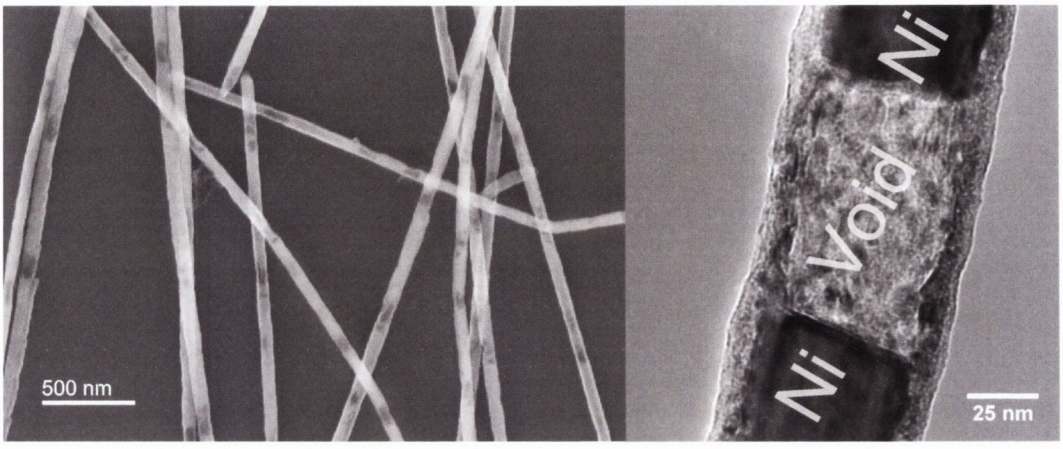

Figure 5.6: *(a) SEM image of nickel nanowires (b) TEM of individual nickel after thermal anneal of 450 °C for 120 minutes.*

180 ± 48 nm respectively, shown in figure 5.7 (a). Figure 5.7 (b) indicates the cell length and void length of the nanowires.

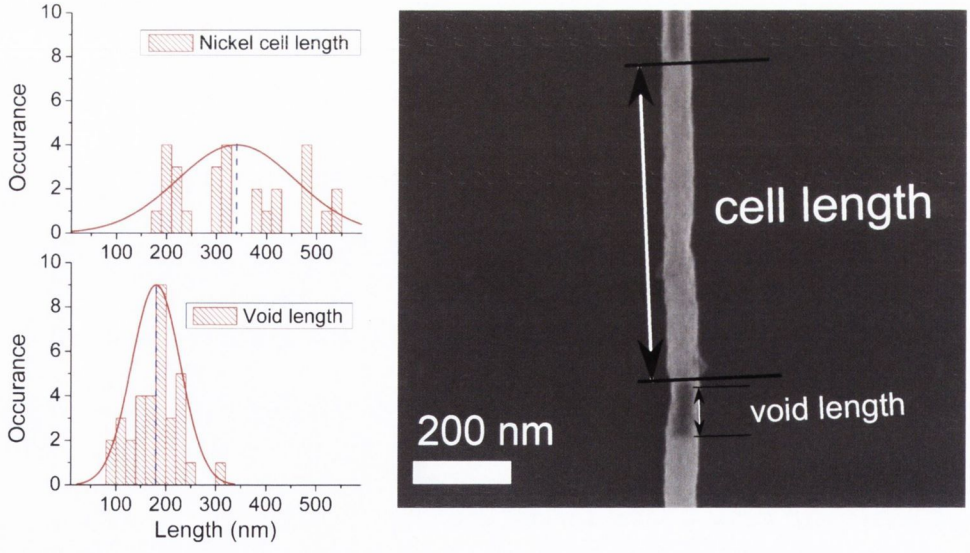

Figure 5.7: *Statistics of nickel cell length and void length for nickel nanowires annealed at 450 °C for 120 minutes. The accompanying SEM describes the cell length distance and void length distance.*

This study of anneal conditions identified the temperature and time required to anneal the nickel nanowires to fabricate a void structure in the core of the nanowire. The nickel nanowires will be now contacted to characterise their electrical properties.

5.3 Device Fabrication

Prior to deposition of nanowires onto insulating substrates, contact pads for electrical measurements and alignment marks were fabricated using UV lithography, as per section 3.2. Briefly, 4" silicon wafers were cleaved into 1 $\times$ 1 cm coupons and thoroughly cleaned with sonication energy in acetone and IPA for 3 minutes each. Substrates were dried for 3 minutes at 150 °C, 150 µl of S1813 UV sensitive resist was then spin coated at 5,000 rpm for 45 seconds. The resist was subsequently baked at 115 °C for 3 minutes. A positive UV lithography mask was placed in mask aligner. The pattern consists of a 6 $\times$ 6 array of 4 contact pads for electrical measurements, and the contact pad dimensions are 250 $\times$ 250 µm. Alignment marks, 10 µm large are spaced at 50 µm intervals to assist EBL contacting. The substrate was placed into a mask aligner. A 5.5 second UV irridation was used to transfer the pattern into the resist. The substrate is immersed in 2.38 % ($wt\%$) tetramethylammonium hydroxide (TMAH) for 25 seconds to develop the resist; during which those parts of the resist that were exposed to the UV energy are soluble and removed. Flowing DI water was employed to stop the development, and the substrate was blown dry in a stream of nitrogen. Metalisation was realised by e-beam metal deposition of 5 and 30 nm of titanium and gold, respectively. Lift off takes place in warm acetone and once complete, an oxygen plasma was employed to remove residual organic contaminants from the lithography process. The substrates were then ready to receive nanowires. An SEM image of the pattern is displayed in figure 5.8.

A 5 µl aliquot of low concentration nickel nanowires in IPA, with an approximate concentration of 10 µg/ml was deposited onto a 1 $\times$ 1 cm chip and allowed to dry. Inspection of the nanowires on the substrate is accomplished using optical microscopy. An example of an isolated contactable nanowire is shown in figure 5.9, a suitable wire for contacting is located within the white circle, a similar concentration of wires was

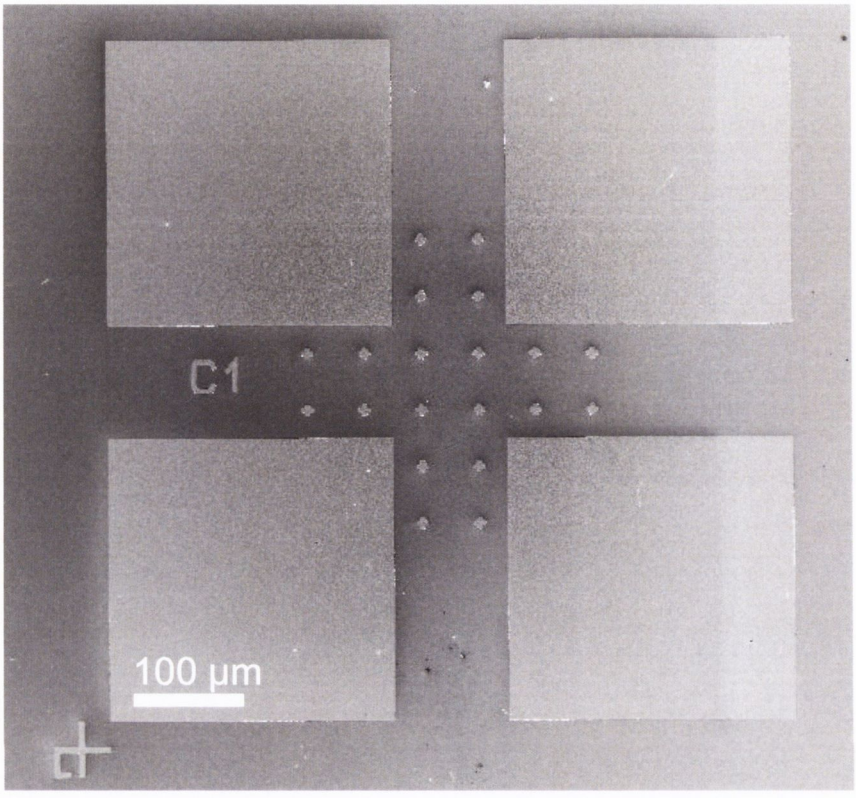

Figure 5.8: *An SEM image of UV lithographically patterned substrate. 4 contact pads are utilised for electrical characterisation. Each device is identifiable by the label on the right. 20 alignment marks assist in accurately locating nanomaterials for subsequent contacting.*

observed at various other sites on the chip. Thermal annealing of the wires could then be performed, figure 5.10 (a), substrates which had received nanowires were placed into a ceramic holder and loaded into the pre-heated furnace. A thermal anneal of 450 °C for 120 minutes was performed. An inspection in an optical microscope post anneal confirmed the nanowires had not become detached from the substrate during anneal. Optical micrographs of the sites were obtained using a Nikon D1300 14 megapixel camera mounted to a Leica microscope with a x50 lens.

These acquired images were analysed using image analysis software ImageJ to obtain an accurate *(x,y)* determination of location of the nanowire with respect to the alignment

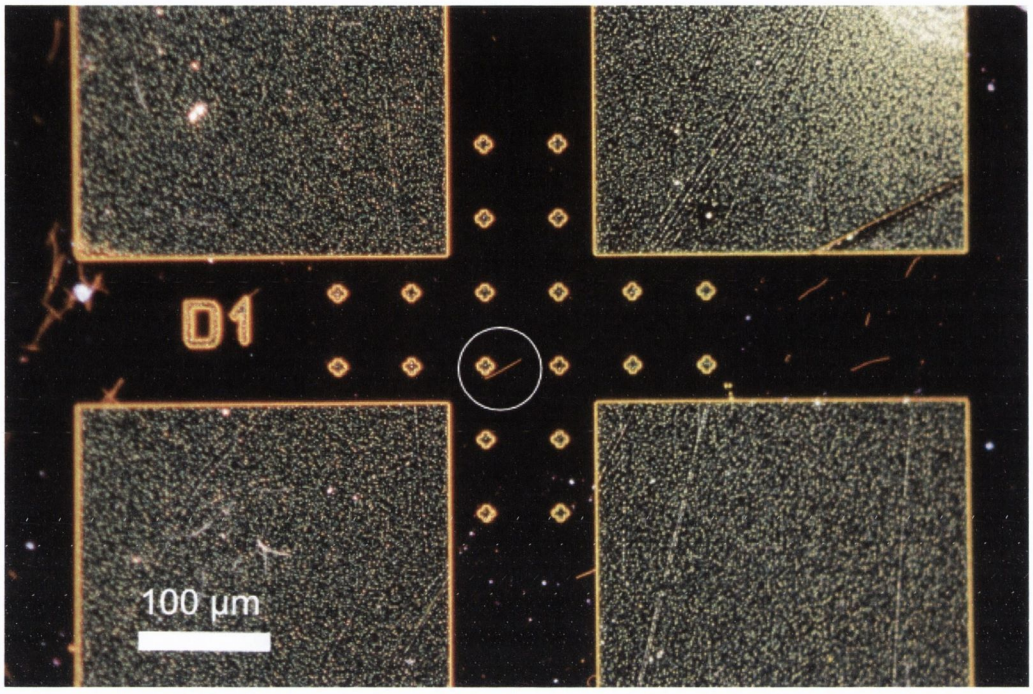

Figure 5.9: *An optical micrography of nickel nanowires dispersed and annealed on a substrate with pre-defined UV-lithography contact pads (large squares in four corners) and alignment marks (ordered array of marks in the centre of the contact pads).*

marks and contact pads. The precise location is important to ensure accurate placement of nanowire contacts. Prior to EBL contacting of the nanowires, ebeam resist was spin coated onto the substrates. PMMA A3 ebeam resist was spin coated at 3,000 rpm for 45 seconds and baked for 3 minutes at 180 °C, resulting in a resist thickness of 150 nm. Once cooled, the samples were loaded into the SEM chamber so that EBL could commence. A beam accelerating voltage of 15 kV was selected to perform EBL on the nanowires. This is a higher accelerating voltage than that employed to fabricate the electrodes in Chapter 3. A higher accelerating voltage will require a higher dose to clear the resist, but the higher energy of the electrons will have a smaller interaction area in the resist, enabling closer spacing of the electrodes, as discussed previously in section 2.6.

EBL contacting of the nanowires was achieved using a Raith Elphy Quantum Plus attached to a Zeiss Supra 40 FESEM. After alignment and careful focusing of the beam, the following parameters were used to accomplish successful lithographic procedure; beam step size 4 nm, dose 230 $\mu C/cm^2$, accelerating voltage 15 kV, aperture 10 µm and beam current 21 pA. Electrodes of width 250 nm with spacing of 400 nm were exposed in the resist. The resist was developed in a solution *v/v* of 1:3 MIBK:IPA for 45 seconds, the electron beam causes chain scission in the backbone of the PMMA resulting in the exposed polymer being soluble. Nickel metal deposition was used to contact the wires, figure 5.10 (c). 50 nm of nickel was e-beam deposited at 1 Å/sec and lift off takes

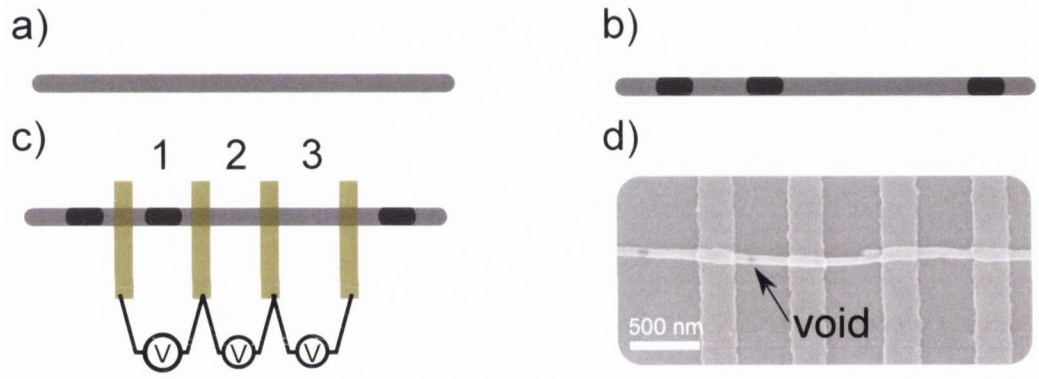

Figure 5.10: *Schematic for void formation in nickel nanowires and electrical contacting. (a) initial nanowire, (b) nanowire post anneal, (c) nanowire with electrodes contacting wire, (d) SEM of wire with void formation and subsequent EBL based contacting.*

place in warm acetone. An example of a contacted device is shown in figure 5.10 (d). If the thermal annealing is successful, channel 1 illustrated in figure 5.10 (c), should be insulating and no transport should be possible due to the non continuous nature of the nickel core, channels 2 & 3, figure 5.10 (c), should be metallic after a SET operation and demonstrate restive switching.

5.4 Electrical Characterisation of Thermally Annealed Nickel Nanowires

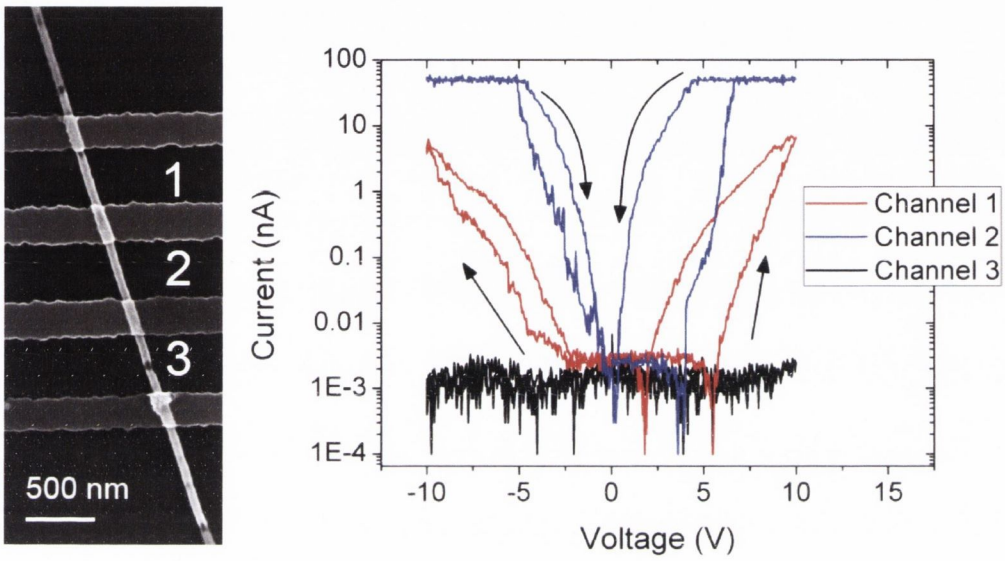

Figure 5.11: *(left) SEM of contacted wire with accompanying electrical (right) Associated current voltage characteristics for the contacted nanowire. Three different transport characteristics are observed.*

After successful EBL the wires were electrically characterised to assess the transport properties of annealed nanowires. A current compliance of 60 nA was applied to prevent catastrophic breakdown of the wires. An example of a contacted device is shown in figure 5.11 (a), 4 nickel electrodes have contacted the same nanowire; there is a channel width of 400 nm between adjacent electrodes. Electrical measurements for the contacted nanowire are shown in figure 5.11 (b).

The nanowire segment in channel 1 and 2 in figure 5.11 do not contain a void, and hence the devices could be switched on. In contrast for channel 3, the wire segment contains a void and is electrically insulating. No current greater than 1 pA was detected up to $\pm$ 10 V so that resistance for this segment of the wire is greater than 10 TΩ. Channel 2, figure 5.11 (left), exhibited an abrupt increase in current at V_{set} at 4.25 V. Channel 1, which contained a small void located just beside the metal electrode, turned

on at 6 V. In the annealed nanowires, transport is still possible where partial voids have formed, indicating metallic nickel remains. The resistance for these devices after a set operation is 80 MΩ for channel 2 and 20 GΩ for channel 1.

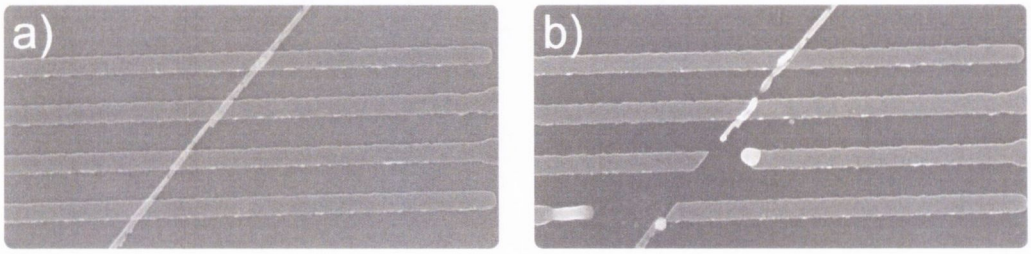

Figure 5.12: *Nickel nanowire with 4 EBL defined electrodes (a) before and (b) electrical measurements.*

Memory resistive switching in the nanowires was not observed, only threshold resistive switching* was observed. The absence of memory resistive switching was due to the inability of the wires to withstand high currents. The transition from threshold resistive switching to memory resistive switching occurs above a certain current, typically above 200 nA. This represents a current density of 70 $\mu A/\mu m^2$. This current dependant switching characteristic will be investigated in Chapter 6. These ambient annealed nickel nanowires cannot withstand such a high current. Figure 5.12 shows a before (a) and after (b) of a contacted annealed nanowire that has failed due to excessive current. A possible reason for this nanowire failure is a thicker oxide shell on the nanowires that have received a 120 minute thermal anneal at 450 °C. Virgin nanowires have an oxide thickness of $\sim$ 4 nm, *c.f.* figure 6.5. TEM data of the annealed nanowires indicates a thickness of $\sim$ 10 nm. This thicker oxide, figure 5.13, will require a higher current to be applied for a conductive filament to bridge the metallic core and the fabricated contact electrode.

A plot of resistance (measured at 4V) for contacted annealed nanowires is presented in figure 5.14. The resistance values are obtained at 4 V on the positive back sweep. In the absence of voids in the core of the nanowire, a resistance of 100 MΩ was obtained.

*Threshold resistive switching will be addressed in chapter 6, briefly, threshold resistive switching has only one stable resistance state, a HRS, with no external bias applied

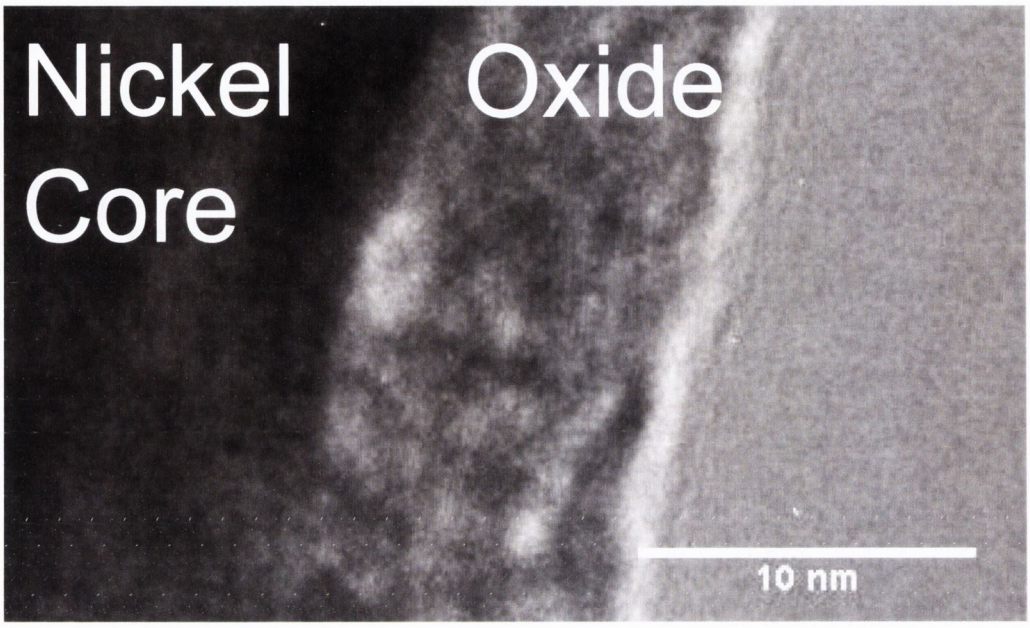

Figure 5.13: *TEM of an annealed nickel nanowire. The thermal anneal has increased the thickness of the oxide from 4 nm to 10 nm.*

This corresponds to a resistivity of the wire of 85 $\pm$ 15 Ω cm, however due to the nature of the wire and void geometry, 4 probe measurements are not possible to perform. This suggests the shell of the nanowire is contributing to the majority of the transport. The thicker oxide requires a higher forming voltage, which is not sustainable in these wire systems.

A small spread in the resistance values was measured for the 4 devices containing no voids. However, in the case of partial voids and full voids, spreads of resistances over 6 orders of magnitude were observed. We will now address this issue and the possible contributors to this spread in values.

Where a void in the nanowire only partially spans the diameter of the conductive core of the nanowire, the effective resistance of the metallic nickel segment increases due to the locally reduced nickel composition

Energy-dispersive X-ray spectroscopy (EDX) was used to investigate the material composition of the nickel nanowires and the voids within. Spectrum 25, figure 5.15, displays the spectra obtained for the region highlighted in green. This area shows no

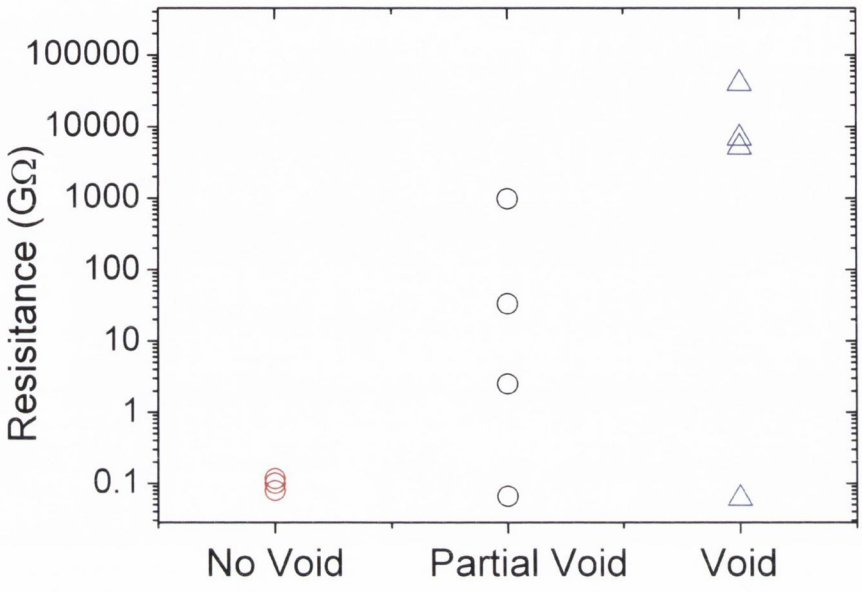

Figure 5.14: *Plot of resistance values obtained for three different types of wire states. Wires with no void showed a resistance of ~ 100 MΩ whereas wires containing voids of some description had a larger resistance and much greater spread of values.*

visible signs of defects and is nickel rich. Spectrum 26 is obtained from a void in the core of the nanowire. Both spectra show peaks at 0.5 keV and 1.75 keV which represent, respectively, an oxygen and silicon peak. These peaks are expected due to the contribution from the 300 nm of thermally grown oxide on the substrate and bulk silicon beneath. The presence of a carbon peak is likely due to surface contamination.

The intensity peak at 0.85 keV is a measure of the quantity of nickel contained in the area investigated. In the section of the wire containing no void, spectrum 25, the nickel composition is 2.05 %, however, the void shows a nickel composition 0.29 %. Table 5.4 displays the percentage elemental composition in the respective areas highlighted. This approximate 1:10 nickel content ratio for void:wire is a possible reason that non-insulating resistance values were obtained for 2 probe measurements where a void is

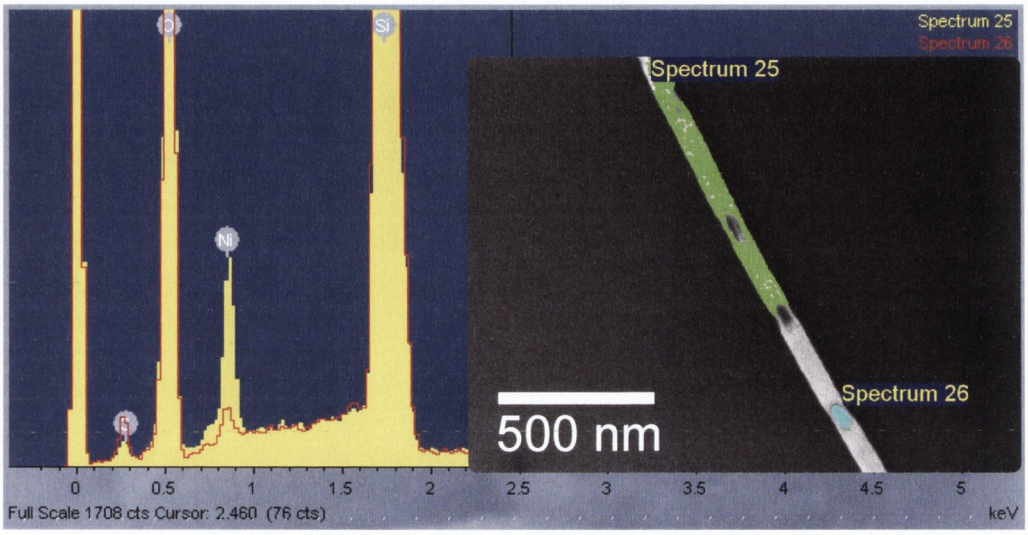

Figure 5.15: *EDX spectra of annealed nickel nanowire at two different sites on the wire. A clear nickel peak is located at 850 eV for the spectra obtained in the non-void area. The spectra recorded on a void lacks the nickel peak, there is however a smaller nickel peak indicating there is nickel remaining in the void.*

Element	Spectrum 25	Spectrum 26
C	5.29 %	11.62 %
O	47.71 %	44.39 %
Si	44.95 %	43.69 %
Ni	2.05 %	0.29 %

Table 5.1: *Elemental composition of nickel nanowire in figure 5.15.*

located in the channel. This residual nickel can also be observed in TEM images of voids located within the wire.

TEM images in figure 5.16 show the detailed structure of a void located within the wire. The dark areas either side of the void are the nickel core of the nanowire. The crystal planes of the wire are observed either side of the void and appear to remain intact even after a thermal anneal. The image on the right shows a zoomed in region of the void. In this region an ordered array of atoms is observed, with a spacing of $\sim$ 2.0 Å.

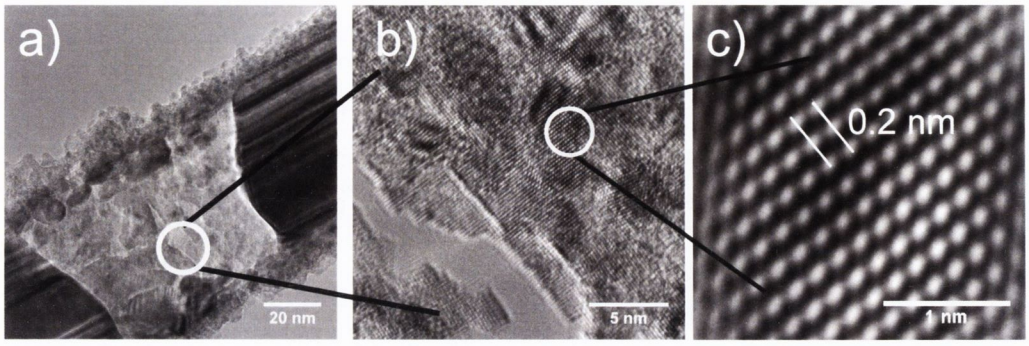

Figure 5.16: *(a) TEM image showing a nickel nanowire containing a void. The crystal planes of the metallic core can be observed on each side of the void. (b) and (c) zooming in on the void area indicates that the material remaining is partially polycrystalline. The atomic spacing in the polycrystalline area is 2 Å.*

The shell oxide in these wires is amorphous, an example of the amorphous nature is displayed in figure 5.17, and so this ordering is as a result of residual nickel remaining in the core remaining. This remaining nickel in the void could be a contributing factor to transport across a void and explain the non-insulating nature of nanowires with voids being located in the channel.

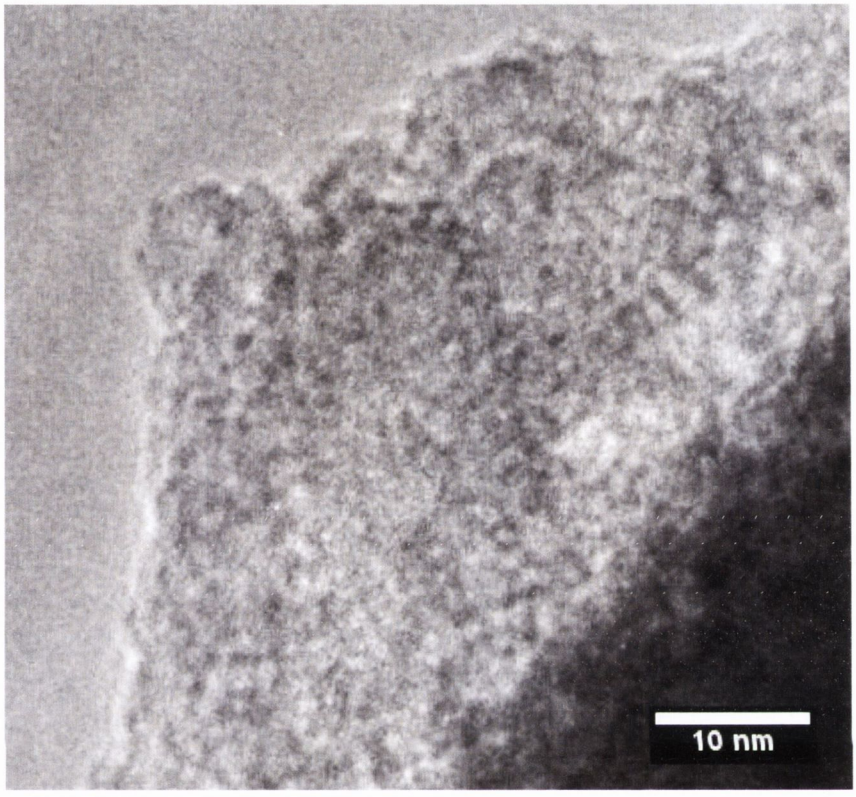

Figure 5.17: *TEM image of a nickel nanowire shell, showing the amorphous nature.*

5.5 Conclusions and future work

Nickel nanowires have been controllably annealed in an ambient atmosphere to produce various morphologies. The formation of voids in nickel nanowires is used to investigate how the electrical characteristics depend on where voids are located and where there is an absence of voids. In the case complete voids in the core of the wire, an electrically insulating behaviour is observed. However, even in the presence of voids, nanowires exhibited both insulating and conductive behaviour. EDX and TEM were employed to provide evidence of residual nickel grains or even atomic chains bridging the void and hence contributing to the non-insulating nature of the material.

For future studies, we propose a wire contacting regime displayed in figure 5.18. Controlled annealing of nickel nanowires results in void formation in the core of the

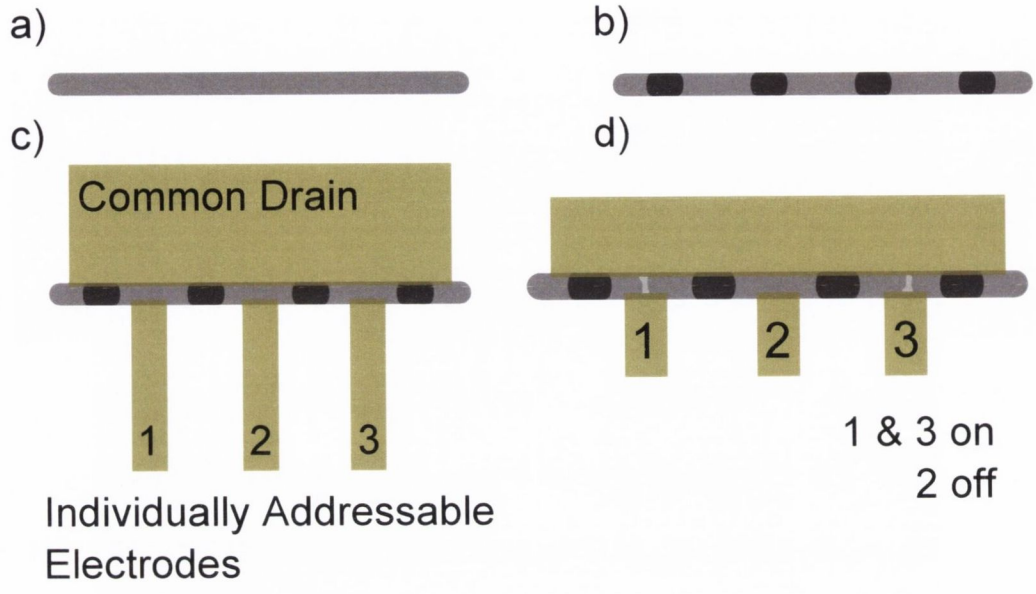

Figure 5.18: *Schematic for proposed nanowire based memory cells. (a) & (b) nanowire is annealed, (c) fabricate a common drain with individually addressable sources. Electrodes are located in between voids and the insulating nature of the voids prevents charge leakage across the wire (d) as an example channels 1 and 3 can be turned on and channel 2 remain off.*

nanowire, while the external structure of the nanowire remains intact. Nickel-nickel oxide ReRAM could be realised by thermal annealing and subsequent high precision EBL. Annealing of the wires would result in voids, figure 5.18 (b), and the wires would be subsequently contacted by EBL. However, this contacting strategy differs from that previously demonstrated in section 5.3. A common electrode acting as the drain would be fabricated on one side of the nanowire and individual electrodes fabricated on the opposite side of the wire, figure 5.18 (c). The individual sections of the wire act as memory cells. The presence of the voids will act as transport barriers across the wire. A set operation, figure 5.18 (d), as demonstrated in channels 1 and 3, transforms the section from a HRS to a LRS.

We propose that controlling the oxide thickness of the nanowire in combination with an anneal optimisation of void formation sub-200 nm ReRAM memory cells could be realised.

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6

Threshold and memory resistive switching in nickel oxide nanowires

An investigation of the electrical resistance switching behaviour of nickel nanowires in a sparse network, as well as the reproducibility and controllability of the memory operation observed in these networks is presented in this chapter. Two different types of resistance switching (RS) mechanisms are observed. Both memory resistive switching and threshold resistive switching are demonstrated and either can be selected depending on the compliance current applied in the SET operation.

This is the first time both bi-stable memory and mono-stable threshold resistive switching have been observed in nickel nanowire networks. To date, a co-existence of both threshold and memory resistive switching has been observed in only a small number of material systems, such as, NiO films,[1;2] NbO_X films,[3] as well as individual nickel nanowires.[4] While only nickel nanowire network data will be presented in this chapter, we predict this behaviour will also be observed in other core-shell based nanowire networks, such as, but not limited to copper, germanium or lead.

The ability to control the switching mechanisms is critical for the integration of memory elements and switches into large device arrays. The addition of a switch in an array prevents cross talk between memory elements and eliminate the issue of sneak currents around memory arrays.[5] Typically, multilayer lithography and metal deposition is required to integrate memory and switching cells into the same array. The methodology

presented in this chapter eliminates this requirement. We will demonstrate that nickel oxide nanowire networks can be utilised as both switching and memory elements.

6.1 Introduction

There exists two types of unipolar resistive switching effects; memory resistive switching and threshold resistive switching. The typical current-voltage characteristics observed are presented in figure 6.1. Memory resistive switching[6;7;8], presented in figure 6.1 (a),

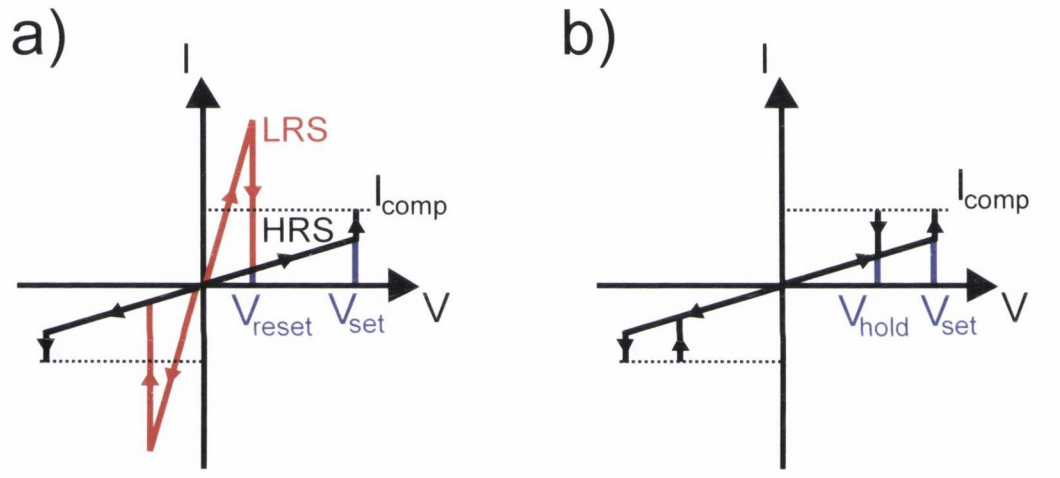

Figure 6.1: *(a) Unipolar memory resistive switching, two resistance states are possible at zero bias, (b) unipolar threshold resistive switching, one state is attainable at zero bias.*

has two reversible transitions, at a certain voltage a transition from a conducting state to an insulating state is observed, this voltage is referred to as V_{reset}, the other transition is one from a high resistance state to a low resistance state, this is typically observed at a higher voltage than V_{reset}, and is referred to as V_{set}. Both of these resistance states are real states in the material and can be read at zero bias. Conversely, threshold resistive switching,[1;9] presented in figure 6.1 (b), has only one stable resistance state at zero bias, the HRS, but switches between HRS and LRS states at finite bias.

Seo *et al.*[1] demonstrated both threshold and memory resistive switching in NiO films. To accomplish this two different oxygen concentrations were used during the NiO film

deposition. Depositing the film in an atmosphere of 5 % oxygen resulted in a NiO composition of $Ni_{1.05}O$, and at 20 % oxygen a composition of $Ni_{0.95}O$. These results show that an atmosphere of 5 % oxygen produces an excess of nickel and an atmosphere of 20 % excess oxygen in the NiO films. These different compositions are enough to alter the resistive switching characteristic from memory to threshold resistive switching. In this earlie study different resistive switching characteristics are demonstrated in the same material, although at different nickel compositions.

Figure 6.2 (a) & (b) display switching characteristics of NiO films deposited in different oxygen ambients; these differing oxygen contents produce NiO in differing stoichiometric ratios. At 5 % oxygen content, nickel defects and vacancies coexist in a NiO film,[10] at 3 %, resistive switching is observed. Figure 6.2 (a), at zero bias, two different resistance states are attainable. However, as the authors increased the oxygen content in the gas mixture during NiO deposition, metallic nickel defects decrease and nickel vacancies increase, and as a result threshold resistive switching is observed. Figure 6.2 (b) displays the current voltage characteristics, and at zero bias only one resistance state is observed. The non-retention of a metallic conductive filament (CF) at zero bias renders this material unsuitable as a non-volatile resistive random access memory (ReRAM) candidate. The lower content of nickel is most likely the contributing factor to the differing resistive switching characteristics observed in the two NiO systems.

Resistive threshold and memory switching in the same sample was first demonstrated by Chang *et al.*[2] Again NiO films are the switching material, however, rather than utilising nickel oxide stoichiometry as the switching dependent variable, the device operation temperature controlled the type of unipolar resistance switching observed. Threshold resistive switching was observed at temperatures greater than 156 K, figure 6.2 (d) & (e). Temperatures below 156 K resulted in a bi-stable memory state. Temperature dependent changes observed in the RS of the film are displayed in figure 6.2 (c) - (f). Memory RS is observed in figure 6.2 (c) & (f), both measurements are performed at a temperature below 156 K. The RS mechanism observed in the device is reversible. This temperature dependence indicates that the RS effects are dependent on the thermal

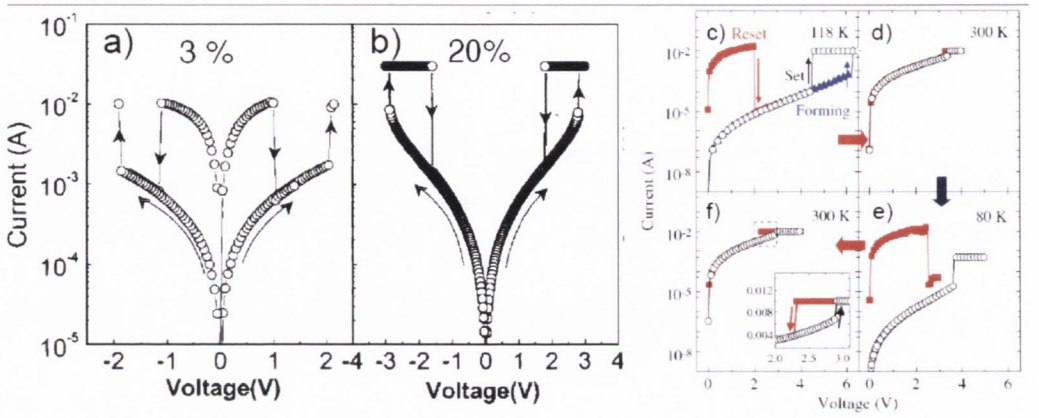

Figure 6.2: *(a) Bi-stable resistance switching of NiO film deposited at 3 % oxygen content. At zero bias two possible memory states are evident (b) mono-stable threshold switching of NiO films deposited at 20 % oxygen content.*[1] *At zero bias only one memory state is possible. Temperature dependant changes of resistance switching are presented (c) - (f) Measurements are taken at 118, 300, 80, 300 K respectively. Differing resistive switching characteristics are noted during the temperature cycle, the effects are reversible.*[2]

stability of the conductive filaments in the insulating oxide medium, both Joule heating and thermal dissipation.

Another approach to produce both threshold and memory RS is to vary the thickness of the bottom electrode in a ReRAM stack. Pt/NiO/Pt ReRAM cells can be switched from a memory RS to a threshold RS simply by altering the thickness of the bottom electrode,[8] a Pt thickness below 30 nm resulted in threshold RS, whereas in samples with Pt thicknesses above 50 nm memory RS was observed. This difference in switching characteristics is attributed to heat dissipation in the bottom electrode. The thinner bottom electrode makes dissipation less efficient, and, as a result heat cannot dissipate from the CF keeping it at a higher temperature and is less stable.

The remainder of this chapter will describe the threshold resistive switching nature of nickel nanowire networks through the application of low compliance currents during the FORM and SET operations. A ReRAM device with a memory and switch element in series is presented. Nickel nanowire networks will be switching material, two nickel

nanowire network resistive switching devices will be fabricated in series. One device will utilise threshold resistive switching, the second device will utilise memory switching.

6.2 Device Fabrication

Nickel nanowire devices were fabricated as previously described in Chapter 3. Briefly, UV lithography defined contact pads and alignment marks received e-beam deposited metal, 5 nm of Ti and 40 nm of Au, figure 6.3 (a). Lift-off was accomplished in gently

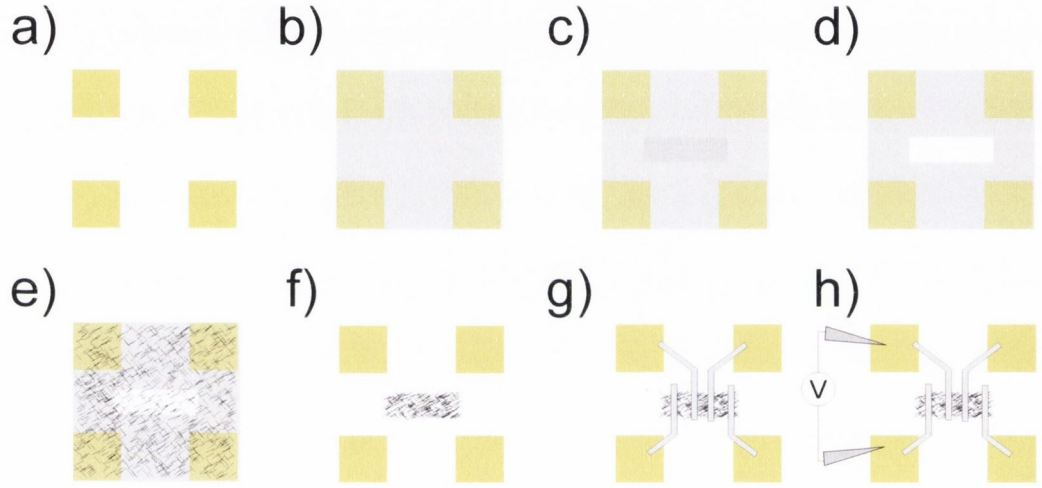

Figure 6.3: *(a) Fabrication of contact pads for electrical measurements, (b) PMMA spin coated onto substrate, (c) EBL exposure of 50 × 150 μm wide windows, (d) development of window using MIBK:IPA, (e) spray coating of nanowires onto substrate, (f) removal of resist in acetone to leave window of nanowires, (g) electrode fabrication using EBL, (h) electrical probing.*

heated acetone. PMMA A3 was spin coated onto silicon oxide substrates, figure 6.3 (b). Windows of 50 × 150 μm were opened in spin coated PMMA thin films using EBL; figure 6.3 (c) & (d). Nickel nanowires were spray coated onto the substrate, figure 6.3 (e). Where no resist remained, the wires adhered to the substrate, figure 6.3 (f). The wires remaining on the substrate were subsequently contacted for electrical characterisation. EBL defined electrodes with a separation of 40 μm were exposed in

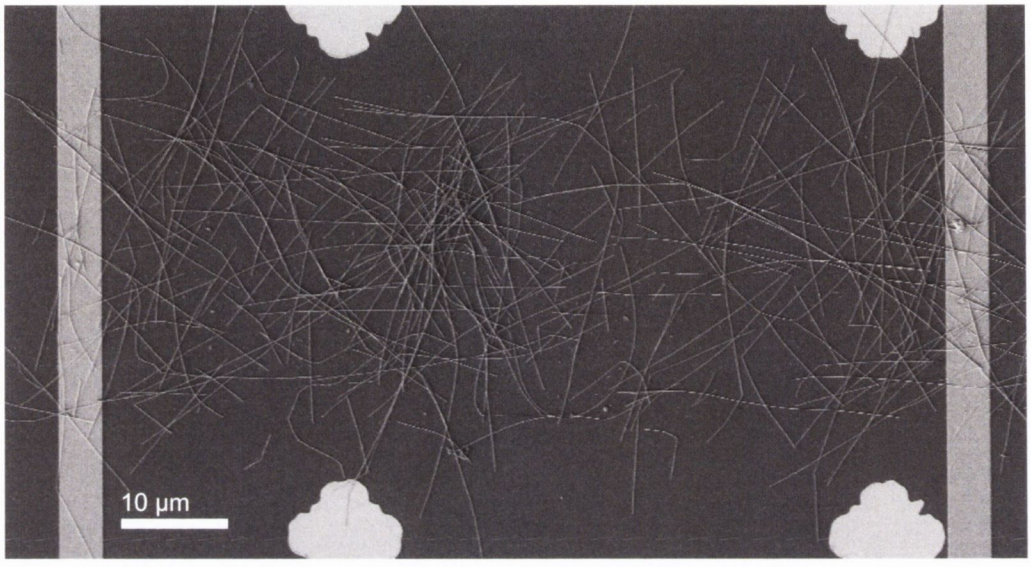

Figure 6.4: *Nickel nanowire nework with EBL defined nickel electrodes.*

PMMA of $\sim$ 400 nm thickness and developed in a 1:3 MIBK:IPA solution. Nickel was e-beam deposited and the resulting electrodes were 120 nm thick, figure 6.3 (g). An example of a contacted nickel nanowire network is displayed in figure 6.4. Individual nanowires are not long enough to span the width of the channel, and so, the creation of a low resistance state must involve the formation of connections between individual wires and span the channel. These multiple nanowire-nanowire junctions act as the switching material. Based on TEM analysis, figure 6.5, approximately 8 nm of NiO* acts as the barrier to transport for the high resistance state and the medium in which the conductive filament forms when the LRS is established.

The switching of nickel nanowire networks from an HRS to a LRS requires an initial *forming event* and subsequent SET operations. These current limited FORM/SET operations transform the device from a high resistance state (OFF state) to a low resistance state (ON state) and ensures a conductive filament is present at zero bias. These operations were described in detail in section 3.3. The retention of the conductive filament at zero bias is the essential contributing factor to the *non-volatile* nature of these devices.

*The native oxide on a nickel nanowire is 4 nm and a nanowire-nanowire junction results in combined oxide thickness of $\sim$ 8 nm

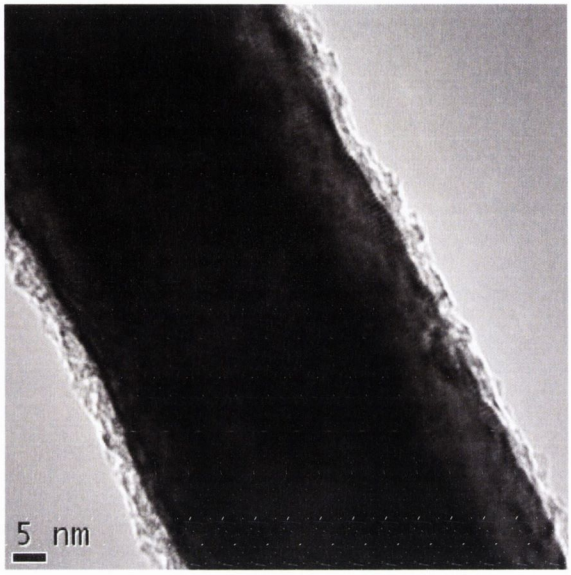

Figure 6.5: *TEM image of nickel nanowire showing approximate oxide thickness of 4 nm.*

There is however an interest in utilising resistive switching properties of these devices as a switching element[11] rather than a memory element.

6.3 Results

The operating principle of a threshold resistive switching device is presented in figure 6.6 (a). Initially, when the device is in an OFF state, no current is observed, however at $\sim$ 3.7 V an increase in current is observed. The voltage where this increase occurs is referred to as V_{set}. The compliance current applied to the device determines the resistive switching nature observed, in general, a high compliance current, $>$ 1 µA, results in memory resistive switching, and a low compliance current, $<$ 200 nA, results in threshold resistive switching. In light of these observations a compliance current of 50 nA is applied to the source meter.

Once the current is at 50 nA an ON state is established. This ON state is retained as long as the voltage applied is above V_{hold}. In figure 6.6 (a) V_{hold} is approximately 3.3 V. As long as a compliance current is applied, the device can be kept in an ON

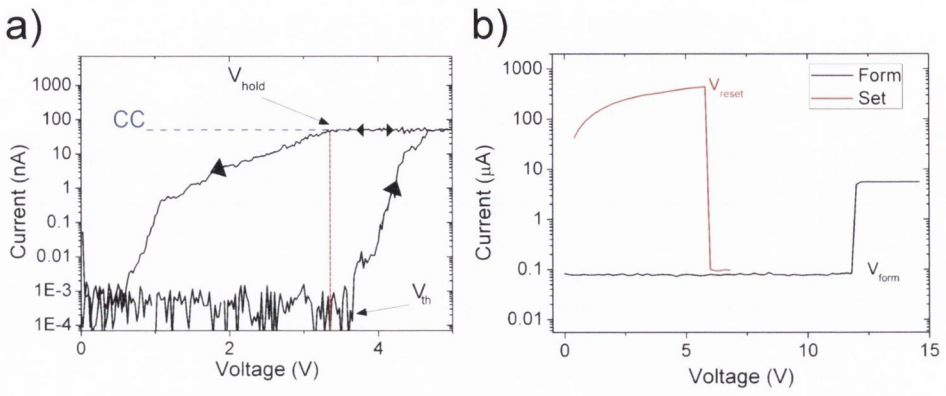

Figure 6.6: *(a) Operating principle for nickel nanowire threshold resistive switching based device. V_{set} indicates the transition from an OFF to ON state. V_{hold} is the minimum voltage possible to still attain an ON state. A compliance current of 50 nA is indicated by dashed blue line. (b) FORM and SET current-voltage characteristics for device.*

state once the applied voltage is greater than V_{hold}. The device is returned to an OFF state by sweeping the voltage back to zero and a high resistance state is reestablished. Because of the non-retention of a conductive filament at zero bias, the volatile nature of the resistance switching exhibited here is not suitable for memory recording.

To facilitate the study of threshold resistive switching in nickel nanowire networks, in a different but similar network, an initial FORM operation on the device had to be performed, this FORMING operation is the black curve in figure 6.6 (b). A current compliance of 5 μA is applied to prevent dielectric breakdown. An abrupt increase in current is noted at 11.8 V. The device is now in a low resistance state. A RESET operation is required to transform the device into a high resistance state and enable a study of threshold resistive switching on the SET compliance current, by applying different current compliances and monitoring the effect on RS mechanism. This RESET operation is the red curve in figure 6.6 (b). Voltage is swept until an abrupt decrease in current is noted at 5.8 V. The device is now in a high resistance state and can be used to investigate threshold resistive switching.

Figure 6.7 shows the current-voltage characteristics of a ReRAM cell of nickel nanowires with an electrode width of 40 μm, see figure 6.8. Prior to performing voltage sweeps, a

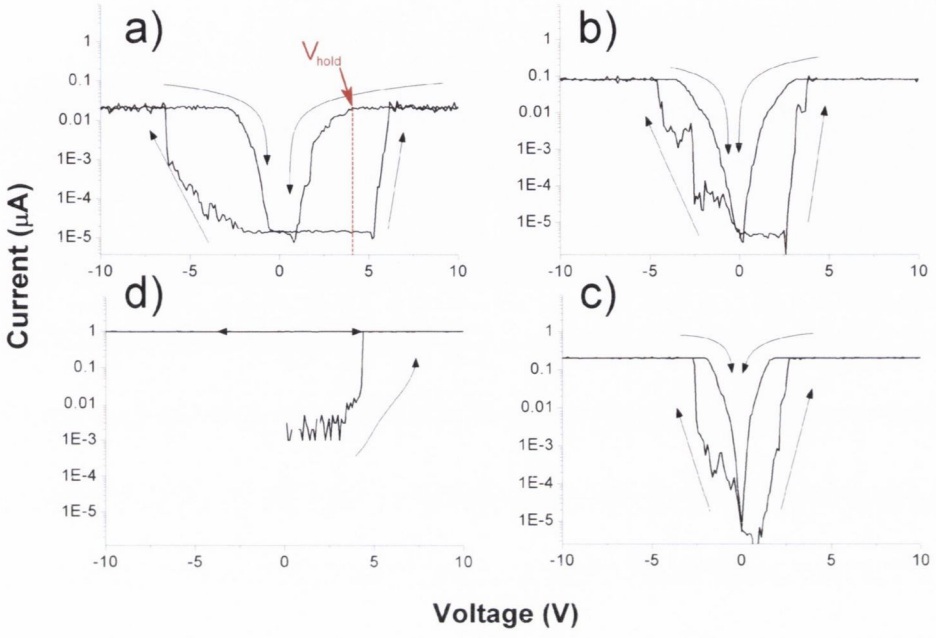

Figure 6.7: *Resistive switching characteristics for nickel nanowire networks. (a) current compliance of 20 nA results in threshold resistive switching, (b) & (c) have compliance currents of 100 and 200 nA respectively, both exhibit threshold resistive switching, (d) memory resistive switching is observed with the application of 1 μA compliance. A conductive filament remains at zero bias.*

current compliance was applied to the source meter. Figure 6.7 (a) has a compliance of 20 nA applied. During the voltage sweep, the current increases suddenly at a threshold voltage, V_{set}, of 5.3 V. This increase corresponds to a transition from a high resistance state of 280 GΩ to a low resistance state of 260 MΩ. The voltage sweep continues and the device can be kept in a low resistance state as long as the voltage is kept above V_{hold}, $\sim$ 3.75 V. Below this voltage, the conductive filament keeping the device in a low resistance state becomes unstable and can no longer bridge the insulating oxide. This non-retention of the conductive filament is due to the compliance current not being set at a high enough current value. A higher compliance current results in more current

flowing through the conductive filament during its evolution, and as a result, a stronger conductive filament is formed.

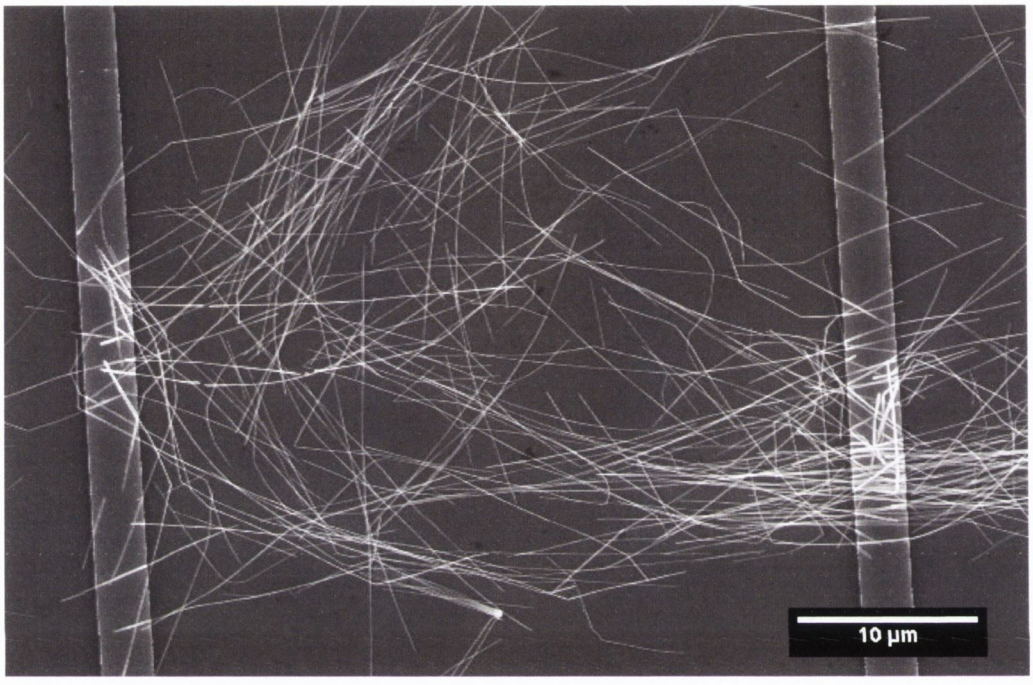

Figure 6.8: *SEM image of nanowire network of width 40 µm. Electrical data presented in figure 6.7.*

The compliance current was increased to 100 and 200 nA for figures 6.7 (b) and (c) respectively. Again, threshold resistive switching is observed. A return to a high resistive state is observed at zero bias. No RESET operation has been performed. To transform the device into a bi-stable memory element, a compliance current value of 1 µA was applied. Figure 6.7 (d) displays the current voltage data. A V_{set} of 4.5 V is observed. However, unlike the three previous sweeps, the device remains in the LRS state at zero bias. This demonstrates that the transition between threshold resistive switching and memory resistive switching can be controlled simply by tuning the compliance current above or below a critical value.

The hysteresis in the current voltage curves observed in figure 6.7 give interesting insights into filament formation and rupture. Figure 6.7 (a) is represented in figure 6.9 as

both linear and log plots of the data. All current voltage sweeps are performed identically,

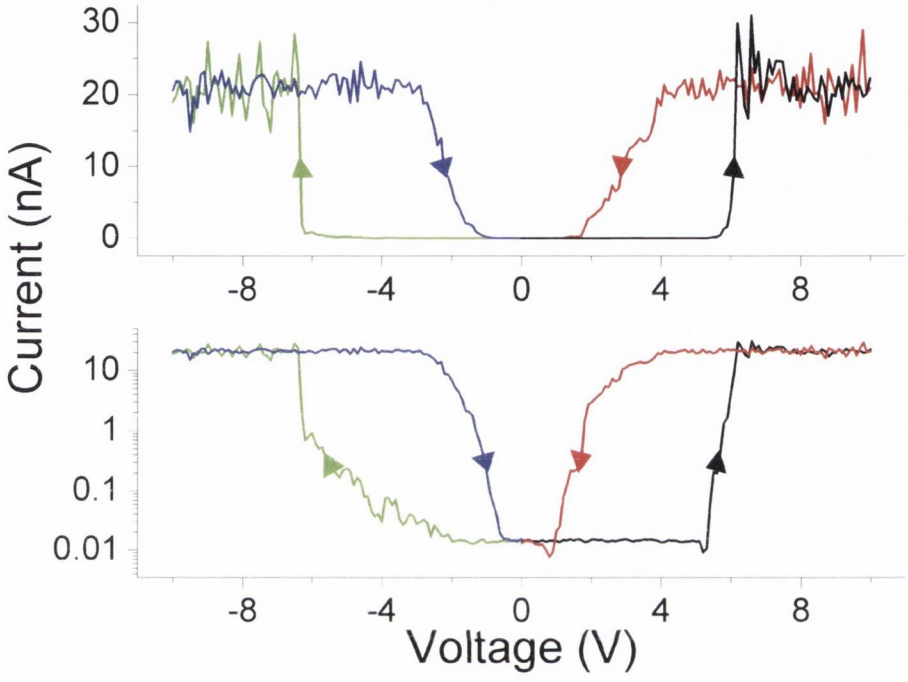

Figure 6.9: *Threshold resistive switching data replotted from figure 6.7 (a), linear y-axis in upper panel and log y-axis in lower panel.*

the bias is initially at zero and swept positively to V_{max}, 10 V, and is subsequently swept from V_{max} to V_{min} and finally to 0 V. Typical threshold resistive switching results in no current being observed until an abrupt increase, as shown in figure 6.9 black curve. On the return sweep the current decreases over a much larger voltage range, and the decrease is a lot more gradual, figure 6.9 red curve. The subsequent reverse sweep, figure 6.9 green curve, doesn't experience an abrupt increase in current, rather a residual filament appears to remain and a gradual increase in current is observed. The reverse sweep, figure 6.9 blue curve, again, as at positive bias, is a gradual reduction in current. Both return sweeps to zero bias exhibit current-voltage characteristics of linear nature, more evidence that the filament is metallic in nature.

The characteristics observed suggest there is residual filament remaining at zero bias during a voltage sweep. Filament formation is a distinctly different mechanism to filament rupture. Filament formation takes place over a smaller bias window.

Maintaining the compliance current at or below 200 nA ensures the device experiences only threshold resistance switching. Should a conductive filament remain intact at zero bias, removal can be achieved simply by a RESET operation to the device, a voltage ramp and no compliance current applied will return the device to an OFF state. At V_{reset} an abrupt decrease in current will represent the rupturing of the conductive filament and a return to a high resistance state.

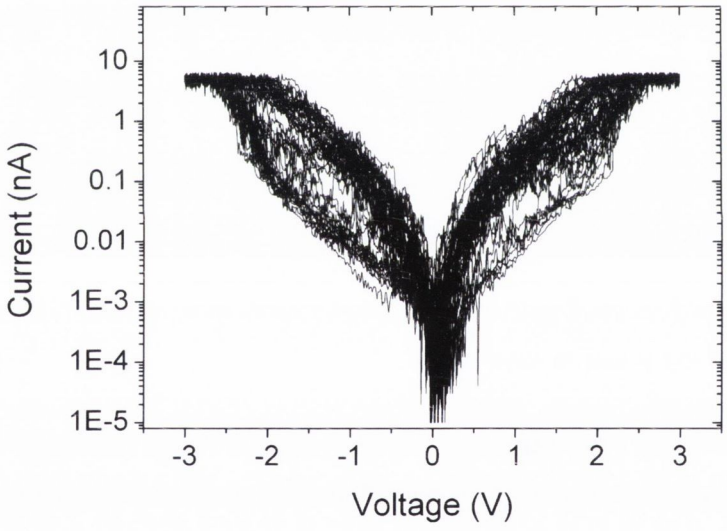

Figure 6.10: *Current-voltage characteristics of nickel nanowire device. A 5 nA compliance current is applied to ensure threshold resistive switching is observed.*

If these nickel nanowire networks are to be integrated into ReRAM devices, the long term stability of these threshold switches is of huge importance. Can they repeatedly switch on and off? Figure 6.10 displays 20 consecutive voltage sweeps on a log scale. The compliance current is 5 nA. The device continues to exhibit a hysteresis loop after 20 sweeps. This controllability of switching characteristics enables us to fabricate devices in series exhibiting two different switching mechanisms.

6.4 Nickel nanowire memory and switching device

Non volatile memory consists of a memory element with bi-stable states at zero bias and a switching element. The resistance of the switches is controlled by external bias. The memory element of the device stores the information and the switch element controls access to a specific memory element. Fabricating memory and switching elements in series presents both technical and fabrication challenges. As discussed in the introduction of this chapter, being able to tune the electrical properties of these nanowire networks opens up the possibility to integrate both memory and switching elements into a memory array made solely out of nanowire networks.

Figure 6.11 (a) shows a three dimensional stack structure of a memory device, comprised of a switch and memory element located in between conductive lines. A switch is required to ensure no reading interference is observed, i.e. there are no sneak currents across adjacent devices. Figure 6.11 (b) shows a typical error arising in the operation of a 2×2 cell. The HRS cell is being read, but current can flow between the three devices in a LRS to cause a mis-read. By adding a switch element, as in figure 6.11 (c), alternate paths are rectified and the reading current flows only through the selected cells. However this method requires advanced lithographic methods, as well as the expensive integration of three distinct materials, NiO, Pt and VO_2. We propose utilising the memory resistive and threshold resistive switching properties of nickel nanowire networks to fabricate a memory and switching device. Firstly, we will present the operating principle of the proposed bi-stable memory device.

Figure 6.12 (a) displays the switching characteristics of a bi-stable memory device. The device exhibits a transition from a high resistance state to a low resistance state at a SET voltage (V_{set}) of $\sim$ 8 V and from a low resistance state to high resistance state at a RESET voltage (V_{reset}) of 4.5 V. Figure 6.12 (b) shows typical behaviour of a threshold resistive switching device. During voltage sweeps the current increases at a threshold voltage (V_{th}) of 4 V and the device switches from a high resistance state to a low resistance state. This LRS can then be held at a low resistance state at voltages higher than a hold voltage (V_{hold}) of 2.5 V. Voltages below V_{hold} result in the device returning to a high resistance state.

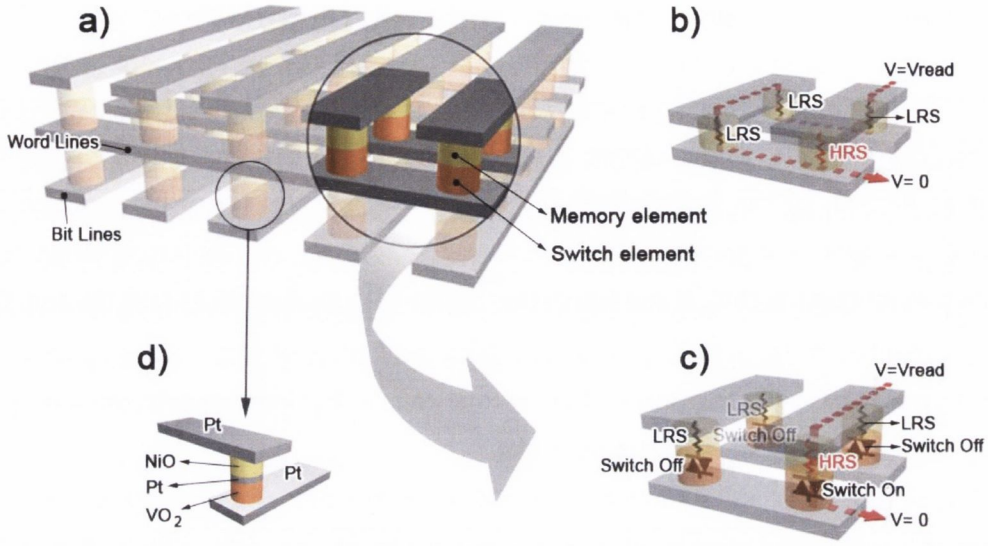

Figure 6.11: *(a) Cross bar memory structure, each bit consists of a memory and switch element confined between conductive lines, (b) reading interference obtained due to absence of switch (c) rectified reading operation with switch element (d) structure of a single cell containing NiO as memory element and VO_2 as switch element. Reproduced from Lee* et al.[12] *(2007).*

To assess if these switching characteristics can be integrated into a series device a nickel nanowire network was contacted using three electrodes, as shown in figure 6.13 (a). The top memory element was programmed to be the bi-stable memory device and the lower memory element the threshold switching memory element. Based on knowledge acquired in section 6.3 we can selectively program elements to exhibit certain switching characteristics.

The top element was SET with a current compliance of 1 μA, to enable memory resistive switching and the voltage was swept. A transition from a high resistance state to a low resistance state was observed. The lower element had a current compliance of 10 nA SET to enable threshold resistive. A voltage sweep confirmed the presence of threshold resistance switching.

Both devices were connected in series, a compliance current of 10 nA was applied to source meter V_2 in figure 6.13 (a) and the voltage swept in source meter V_1. Figure 6.13 (b) displays the resulting current voltage data across the two other electrodes. Initially, at a voltage lower than V_{th}, the device is in a high resistance state, the upper element being in low resistance state but the lower element being in a high resistance state. At a voltage above V_{th}, the lower element switches from an OFF to ON state and overall the device is in a LRS. The voltage is increased until the upper element is *reset* and the device is returned to a HRS. The devices exhibit an ON/OFF ratio $> 10^3$. This large ratio reduces the possibility of a mis-read. The same switching characteristics are expected for negative bias operations.

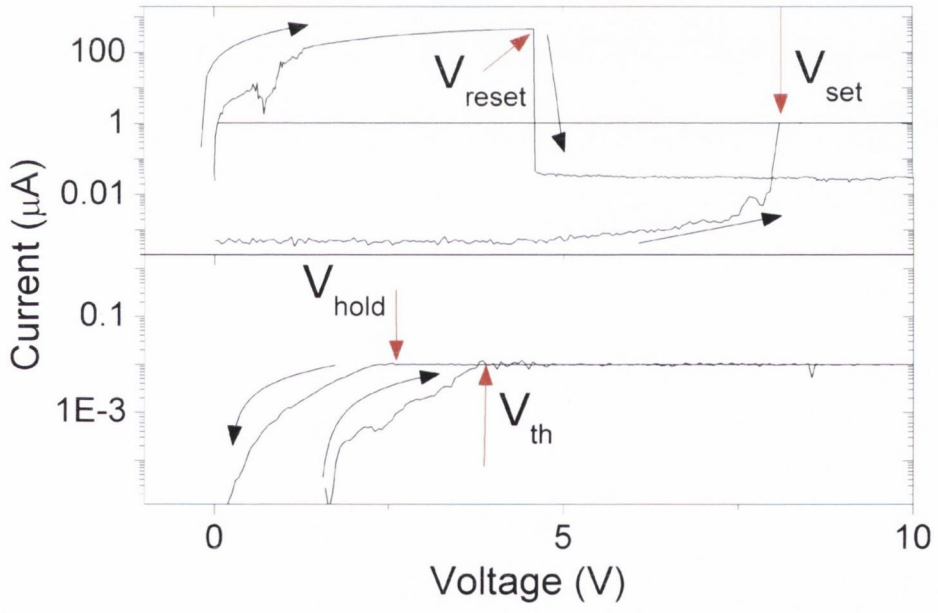

Figure 6.12: *(a) Bi-stable resistance switching of a nickel nanowire network, achieved using a 1 μA compliance current (b) threshold resistive switching observed with compliance current of 10 nA. Both networks contain identical nickel nanowires.*

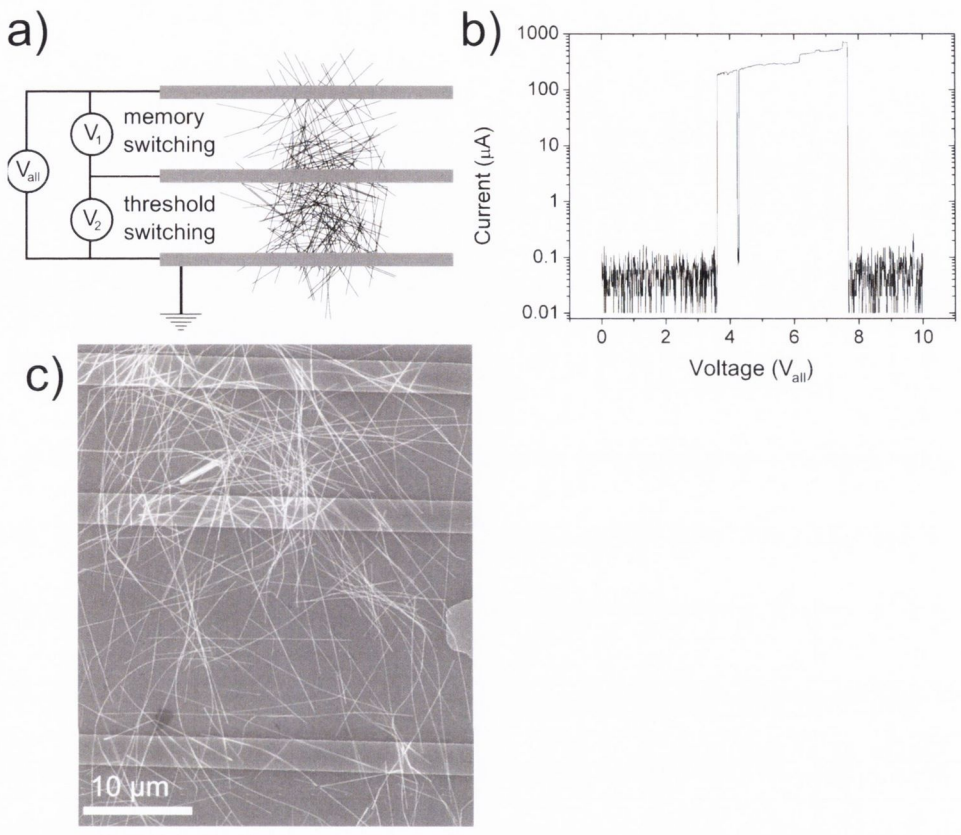

Figure 6.13: *(a) Schematic of switching device, upper network exhibiting memory switching, lower network threshold switching. (b) current voltage characteristics of switching device across both outer electrodes. Initially the cell is in an OFF state since the switch is in an OFF state. After V_{th}, $\sim$ 3.75 V, the device is in an ON state and the stored information can be read. By applying a voltage comparable to V_{reset}, $\sim$ 7.75 V,the device is transformed to an OFF state. The memory cell can be read once the voltage applied is greater than V_{th} and subsequent set and reset operations can be performed. (c) SEM image of the device.*

6.5 Conclusions

Using the same material we have shown that the type of switching observed is controllable based on the compliance current that is defined for the SET process. Nickel

nanowire networks have shown both bi-stable memory resistive switching and mono-stable threshold resistive switching. Further investigation is required to integrate this multiple resistive switching into individual nickel core-shell nanowires, thereby reducing the dimensions of ReRAM devices sub 100 nm.

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7

Ongoing work - Hysteretic behaviour of nanowire network systems

Parts of this chapter have been published in Nano Letters: Peter N. Nirmalraj, Allen T. Bellew, Alan P. Bell, Jessamyn A. Fairfield, Eoin K. McCarthy, Curtis O'Kelly, Luiz F. C. Pereira, Sophie Sorel, Diana Morosan, Jonathan N. Coleman, Mauro S. Ferreira, and John J. Boland, "Manipulating Connectivity and Electrical Conductivity in Metallic Nanowire Networks," Nano Lett. 2012, 12, 5966-5971

7.1 Introduction

NANOWIRE networks have found uses in many applications, such as, sensing materials, flexible displays and transparent conductors[1;2;3], and, as detailed in chapter 4, resistive random access memory. Of the types of nanomaterials available one dimensional materials are the most suited to enable directional transport in networks over distances many times their length. Zero-dimensional nanomaterials, or nanoparticles, offer the worst return for transport over large distances, with two dimensional nano-sheets, like graphene, faring slightly better. We will investigate the transport characteristics of networks of nickel nanowires over length scales much larger than those investigated in Chapter 4, as well as the memristor like characteristics of copper nanowire networks.

Dense nickel nanowire networks will be fabricated by spray coating nanowires onto substrates and subsequently contacted to study the evolving conductivity exhibited in the current-voltage curves. The well connected dense nature of the network is shown to enable the evolution of conductive pathways across nickel nanowires to bridge the electrodes. This evolutionary behaviour is unlike the transport characteristics of short channel nickel nanowire networks. For short sparse nickel nanowire networks, there is no evidence of hysteresis or memristance once a conductive pathway is established, *c.f.* figure 4.7. In contrast to the short channel characteristics, the behaviour of denser larger networks exhibits accumulating hysteresis and memristance. This evolving conductance will also be presented for the case of a copper nanowire network short channel device.

There is still a distinct lack of understanding of the types of connectivity and randomness exhibited in nanowire networks. This work will also introduce initial findings on memristance like characteristics displayed in nanowire networks as well as evolving hysteresis in short channel networks containing copper nanowires.

The chapter will be structured as follows; firstly, the concept of a memristor will be introduced. This brief introduction will be followed by two different nanowire material systems, namely short channel copper nanowires and long channel dense networks of nickel nanowires, both of which exhibit a memristance like behaviour.

7.2 Memristance

We will introduce the concept of memristance and the memristor device in this section. The memristor was proposed theoretically by Leon Chua in 1971,[4] but experimental verification of the memristor was not accomplished until 2008 when a team in HP labs published details of a switching memristor based on a thin film of TiO_2.[5] Oxygen vacancies are fundamental to the operation of the memristor presented in their work. The mathematical definition of a current controlled memristor is:

$$\mathcal{V}(t) = \left(\mathcal{R}_{ON}\frac{\omega(t)}{\mathcal{D}} + \mathcal{R}_{OFF}\left(1 - \frac{\omega(t)}{\mathcal{D}}\right)\right)\mathcal{I}(t) \tag{7.1}$$

$$\frac{d\omega(t)}{dt} = \mu_v\frac{\mathcal{R}_{ON}}{\mathcal{D}}\mathcal{I}(t) \tag{7.2}$$

The voltage and current across the device are given by the variables $\mathcal{V}(t)$ and $\mathcal{I}(t)$, respectively. A schematic of a memristor and the dimensions involved are displayed in figure 7.1. The thickness of the active switching region is given by $\mathcal{D}$, the thickness of the switching region that is doped with oxygen vacancies, that enhance conduction, is $\omega(t)$. $\mathcal{R}_{ON}$ and $\mathcal{R}_{OFF}$ are the minimum and maximum resistances, and the mobility of the oxygen vacancies is given by μ_v. Integrating equation 7.2 yields the following formula for $\omega(t) = \mu_v \frac{\mathcal{R}_{ON}}{\mathcal{D}} q(t)$, where q is charge. The implication that the charge q is a function of time means a memristor can be smoothly transformed to a lower state of resistance by increasing the dwell time on each current-voltage data point. This transformation is associated with the movement of the doping front $\omega(t)$ across the width of the device $\mathcal{D}$.

The application of a positive voltage to the doped side of a memristor will cause charges to drift into the undoped region. This doped region will extend across the width of the device, $\mathcal{D}$, and eventually span the full distance. The device will now be in a lower resistance state. Conversely, if the bias voltage is reversed the oxygen vacancies will recede and eventually ω, the width of the doped region, will approach zero and the device will be in the highest resistance state.

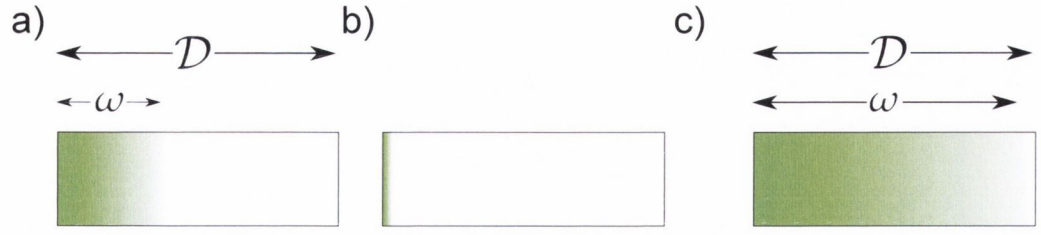

Figure 7.1: *(a) Memristor diagram, the green shading indicating the doped region, $\mathcal{D}$ is the width of the device and ω is the width of the doped region, (b) OFF state, (c) ON state.*

The devices that we will present here in this work are not strictly memristors, however, in 2011 Chua[6] declared:

> All 2-terminal non-volatile memory devices based on *resistance switching* are *memristors*, regardless of the device material and physical operating mechanisms

this declaration brought numerous systems into the memristor category that otherwise would have been excluded.[7;8;9]

This chapter introduces two materials that show evolving resistance characteristics. *Neither* of these systems are true memristors, the resistance of the system evolves only towards a lower resistance state, unlike a conventional memristor, which shows reversible behaviour, however, they both show memristance like characteristics. A true memristor's resistance state is reversible, and multiple cycles between high and low resistance states are possible. Although there is however, no evidence yet of a reversing of the memristance like behaviour in nanowire networks, it is reasonable to expect that such a reversible material can be designed.

The first system investigated will be dense large scale networks of nickel nanowires, the second system will be short channel copper nanowire networks.

7.3 Resistance evolution in dense nickel nanowire networks

Dense nickel nanowire networks were sprayed onto substrates as described in section 3.2. Device fabrication was accomplished on a quartz substrate, the transparent substrate enabled the acquisition of a transmittance value of the substrate in the presence of nanowires. Transmittance at 550 nm of the devices reported in this section are 80%. This value is important. If these nanowire networks are to be used as part of transparent displays, a high transmittance value is imperative.

Nanowire dispersions of concentration 0.1 mg/ml are used for spray coating. 25 ml of nickel nanowire solution is spray coated onto a quartz substrate. Nickel electrodes with separations of 600 μm were fabricated using electron beam lithography and nickel e-beam deposition; an optical microscope image of a set of electrodes is shown in figure 7.2 (a). This large, wide separation, as well as a dense network of nanowires ensures the presence multiple nanowire pathways in the channel to bridge the electrodes. The

existence of multiple pathways is essential if the nanowire networks are to exhibit evolving connectivity.

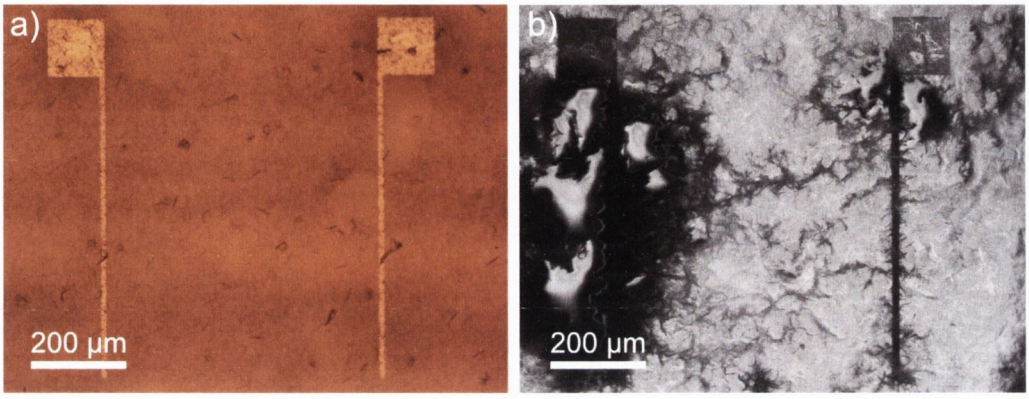

Figure 7.2: *(a) Optical micrograph of nickel nanowire network contacted by two nickel electrodes fabricated by EBL. The channel is 600 µm wide. The black lines on the image are clumps of wires that were not fully separated during AAO extraction, (b) An SEM of a similar device, the non-uniform nature of the nanowire network is evident. Connectivity with the electrodes is apparent with the darker areas of the channel representing wires connected to electrodes.*

The operating principles of this large scale device are similar to those exhibited in sparse short channels. The device initially is in a state of high resistance. A FORMING operation is required to transform the network from an initial high resistance state, to a lower resistance state, with some, but not all pathways activated. A representative FORMING curve, with a current compliance value of 5 µA, is displayed in figure 7.3 (a). When the device is initially in a high resistance state, no current is detected. At 35 V an abrupt decrease in resistance is observed. This value is approximately an order of magnitude larger than the values observed in short channel devices. This higher voltage is due to the far higher amount of nanowire-junctions that need to be converted to an ON state.

The high resistance state is $\sim$ 750 MΩ. After FORMING, the device has a low resistance state of 7 MΩ, this value is limited by the applied current compliance. This

abrupt increase in current corresponds to the formation of a single or multiple conductive pathway bridging the two electrodes.

A conductive pathway has bridged the electrodes, however, only a small number of pathways have been converted to a low resistance state. A reset operation is attempted on the device. The voltage is swept to 20 V, figure 7.3 (b), no characteristic abrupt drop in current typical of a RESET operation is observed. However, hysteresis is noted in the current-voltage measurement. This hysteresis in current-voltage measurements is not observed for sparse nickel nanowire networks at short inter-electrode separations, *c.f.* figure 4.7. The density of the nanowire network, in addition to the wider channel,

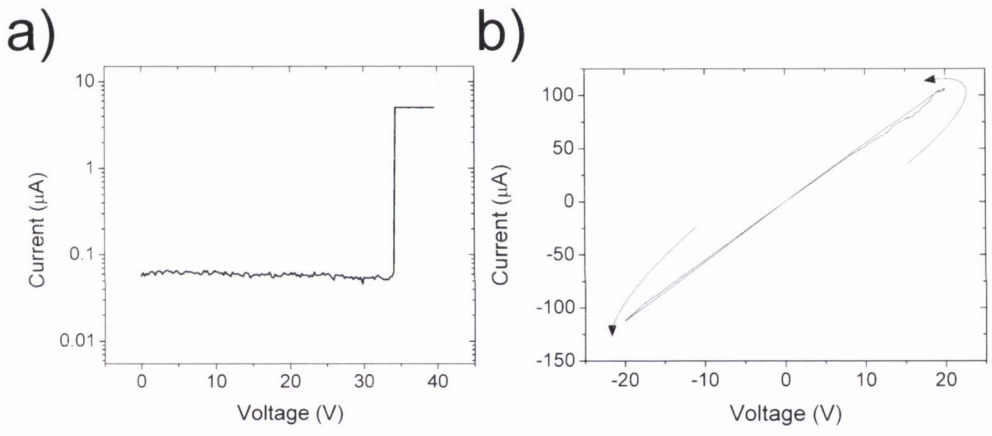

Figure 7.3: *(a) Set operation of nickel nanowire network displayed in figure 7.2, inititally the device is in a high resistance state, and, at 35 V an abrupt increase of current is observed, indicating a transition from a high resistance state, to a low resistance state. (b) Current-voltage sweep of the device having undergone a set operation in (a) minor hysteresis can be observed at higher voltages, the hysteresis is observed in the different currents observed for the same voltage.*

is responsible for in the observed hysteresis effect. Numerous conductive pathways are possible, not just small number available for short channel devices. To assess the possibility of evolving more pathways and activating more nanowire-nanowire junctions the voltage was incrementally ramped to 30, 40, 50 and 60 V, this is displayed in figure 7.4. The current voltage measurement curve evolves on each sweep. As the magnitude

of the maximum voltage, V_{max} is increased, a decrease in the resistance of the device is observed. This resistance decrease is observed as a result of the evolutionary hysteretic nature of the current-voltage curves, as shown in figure 7.3 (b). No RESET of the network was observed.

To compare the network to a memristor, one should consider the preforming condition necessary to shift the nanowires from the OFF state. Forming the device is akin to a small amount of charge diffusing across the width of the memristor along a single conducting path. The repeated sweeps as displayed in figure 7.4 (a) are equivalent to the charge diffusing across the full width of the channel until the device is in an ON state. The increase in current corresponds to the activation of additional nanowire-nanowire junctions. In principle the fully ON condition should correspond to current voltage curves that no longer exhibit hysteresis with all junctions connected. However device failure at the electrode occurs before this condition is ever reached.

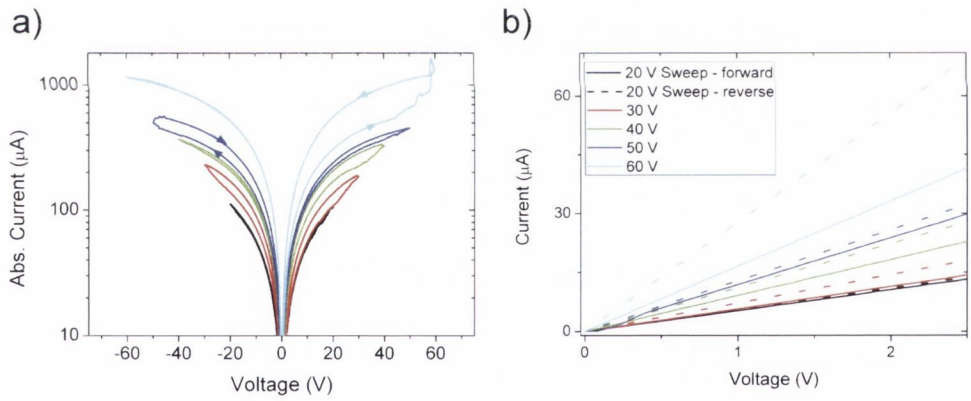

Figure 7.4: *(a) Current-voltage measurements for dense network of nickel nanowires, the measurement was performed on the device present in figure 7.2 (b), the device is exhibiting clear memristance-like behaviour. The hysteresis in the device is indicative of an evolving conduction pathway. (b) shows the low bias data displayed in (a), the curves are non-linear indicating little evolution of the network at low bias.*

The non-linear characteristic of current-voltage curves is evidence of evolving conductive pathways in the nanowire network. However, this evolving nature of the network only proceeds at higher voltages. Figure 7.4 (b) displays positive low-bias current-voltage

data from figure 7.4 (a). The curves exhibit a strong linear characteristic, if pathway evolution were evident at low bias, a strong non-linearity of current-voltage behaviour at low bias would be evident. The linear current-voltage curves indicate a constant resistance value. A non-linear increase in the curve is indicative of pathway evolution. The key message is that at low bias the network exhibits a stable sheet resistance.

The accurate characterisation of the resistance at $\pm$ 18 V was evaluated for all five of the voltage sweeps*. An example of a typical current voltage sweep is displayed in figure 7.5 (a), the four different coloured symbols, located along the current voltage sweep, indicate the condition of the resistance measurement. These resistance values are obtained from the five sweeps in figure 7.4 (a) and displayed in figure 7.5 (b). Acquisition of the resistance at $\pm$ 18 V gives an indication of the reduction in the resistance and hence the evolution of the network pathways.

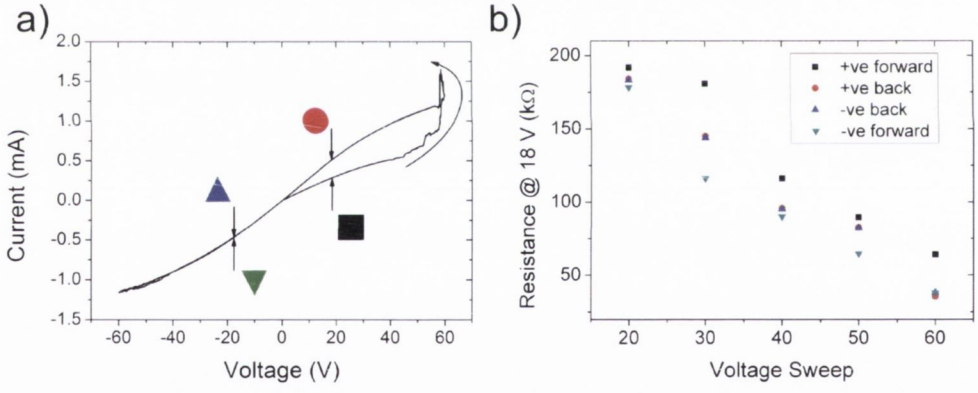

Figure 7.5: *(a) Current-voltage sweep exhibiting hysteresis at large voltages, the shapes on the plot indicate the position of the current-voltage sweep at which resistance values were obtained for the plot in (b). (b) Resistance values are plotted against the corresponding voltage sweep. A clear reduction in voltage is observed at the voltage sweep value is increased.*

The overlay of the positive sweep back and the negative sweep back, the red circle and blue triangle, resistance values means that there is little change in the overall resistance

*18 V was selected as all sweeps had a stable resistance value and there would be significant difference in forward and back sweep

of the device between these voltages, figure 7.5 (b). These resistance values correspond to values acquired at +18 V and subsequently -18 V. We can see that most of the resistance decrease, or network evolution, occurs at high bias.

If the majority of the resistance reduction, or network evolution, occurs at higher biases then the two areas of resistance decrease should be observed between the values of resistance at the black square and red circle and also at the blue triangle and green triangle. This reduction in resistance is observed in almost all the voltage sweeps. For example, as is shown in figure 7.5 (b), the voltage sweep for V_{max} 30 V resulted in a drop between the positive forward and positive reverse sweep in resistance of 35 kΩ. The value on the forward sweep, or black square, was 180 kΩ, with the reverse sweep, red circle, exhibiting a value of 145 kΩ. The subsequent measurement gave a resistance of 144 kΩ, again indicating that there is little evolution of the pathway at low bias. The final section of the voltage sweep, the green triangle, resulted in a resistance of 116 kΩ.

We have demonstrated conductivity evolution in large scale dense nickel nanowire networks. We will now look at short channel conductivity evolution in copper nanowire networks.

7.4 Resistance evolution in sparse copper nanowire networks

Copper nanowires were purchased from `nanomaterials.it` (Milan, Italy) and processed in exactly the same manner as the nickel ones described in section 3.1. The morphology of the wires differed greatly from that observed on nickel nanowires. Figure 7.6 (a) is an SEM image of copper nanowires used in this study. The exterior of the wires showed significant roughening. The diameter of the wires was $\sim$ 50 nm; however, the average length of the wires, at $\sim$ 6 µm, was significantly shorter than the average of the nickel nanowires ($\sim$ 10 µm).

Copper nanowire networks were fabricated and subsequently contacted by EBL as per protocol described in section 3.2. An example of a contacted device is displayed in figure 7.6 (b). The nanowires show significant evidence of clumping, possibly as a result of failed extraction from the AAO template. The copper nanowires exhibit a similar

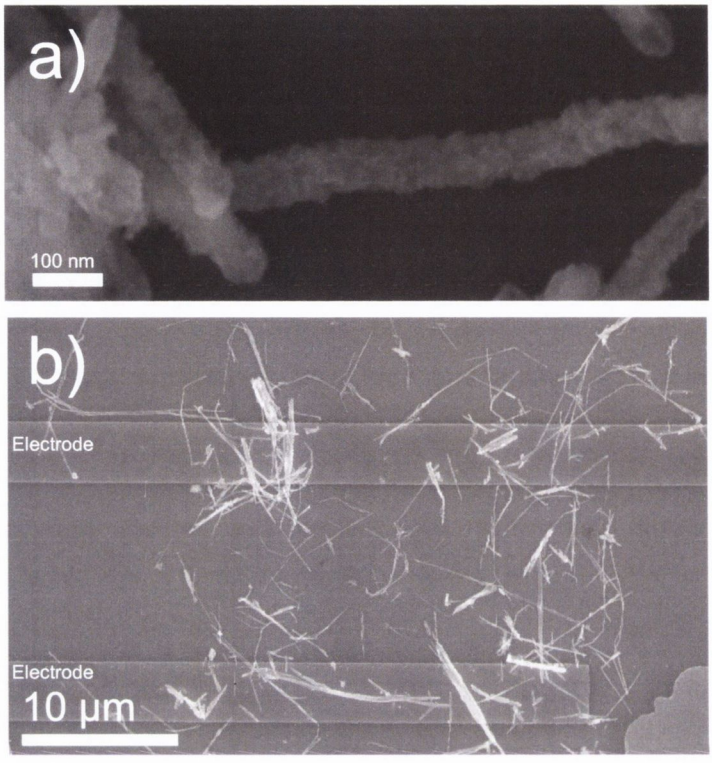

Figure 7.6: *(a) SEM of copper nanowires used in this study, (b) example of copper nanowire network. Two copper electrodes are contacting the network. The channel length is 12 µm.*

structure to nickel nanowires, a metallic core is surrounded by an insulating oxide as shown in figure 7.7. This should result in the electrical characteristics being similar to those exhibited in nickel nanowires, where upon a conductive metal pathway bridging the insulating oxide transforms the electrical properties, and the material resistance changes from a high resistance state abruptly to a low resistance state. However as will be described in the following section, no abrupt resistive switching is observed, rather, the nanowire networks show a gradual reduction in resistance as current voltage measurements are performed. This increasing conductive nature of the device is similar to that observed in a memristor, except that it cannot be reversed by applying a reverse bias.

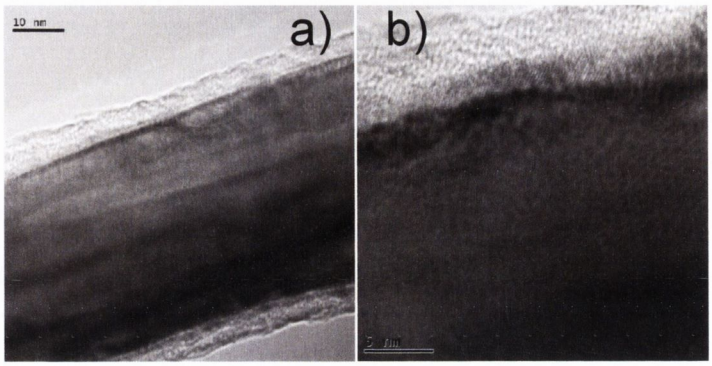

Figure 7.7: *(a) TEM of copper nanowires used in this study, a native oxide on the shell is observed to be ~ 6 nm thick. (b) A high mag TEM image showing the crystalline nature of the core.*

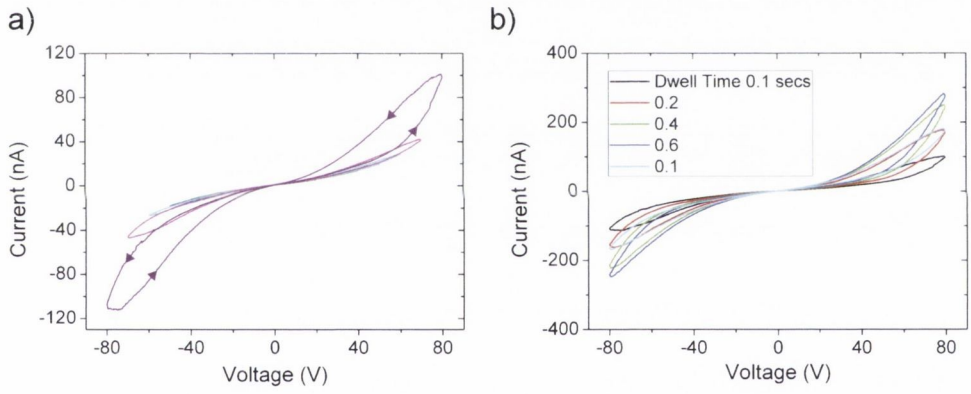

Figure 7.8: *(a) Current-voltage sweeps of copper nanowire network figure 7.6 (b). Final voltage values are incrementally ramped from 10 to 80 V in 10 V increments. Each loop results in an increase of current across the device. (b) The same device was subsequently probed to investigate a time dependence on the dwell time acquisition of each data point.*

Devices with electrode geometry length 12 μm and width 20 μm, similar to that in figure 7.6 (b) were probed to investigate the current-voltage characteristics of copper nanowire networks. An initial current limited FORM operation was attempted on the device from an initial high resistance state to a low resistance state, however, no abrupt increase in current took place, indicating no transition from a high resistance state to a low resistance state was observed. A non-linear hysteretic current-voltage curve was

observed. Current-voltage sweeps with an increasing V_{max} are presented in figure 7.8. The sweeps display clear loops that evolve at higher biases to a lower resistance. The lowering in resistance may be due to an electromigration of copper atoms across the oxide[10] creating a lower resistance path, albeit not a metallic bridge.

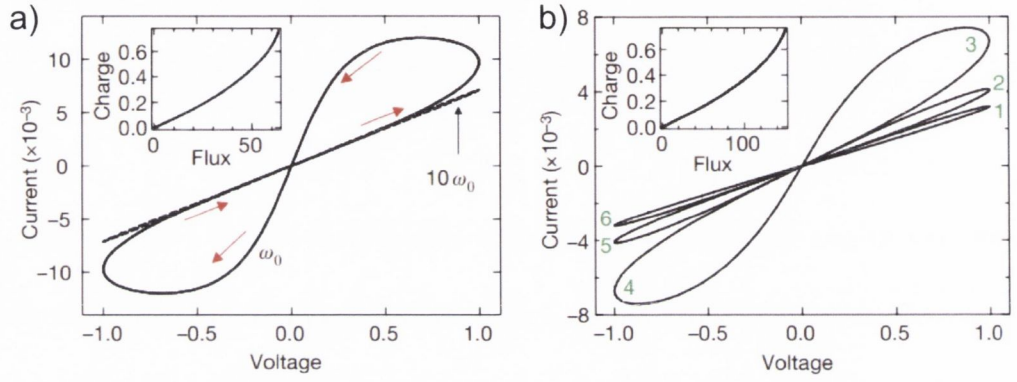

Figure 7.9: *(a) Simulated example of current-voltage curve of a memristor, the collapse of the hysteresis is observed after a tenfold increase in frequency (b) 6 sequential voltage sweeps showing evolution and subsequent retraction of the curve growth. Image reproduced from Strukov (2008)*[5].

A memristor exhibits current-voltage characteristics that are time dependant. Time dependent behaviour on current-voltage characteristics is observed in the short channel copper nanowire networks. Figure 7.8 (b) shows the dwell time dependent nature of the curves. All voltage sweeps have a V_{max} of 80 V. An initial sweep is performed with each current-voltage data point having a dwell time of 0.1 seconds. This initial sweep was followed by a sweep with a dwell time on each point of 0.2 seconds, the resulting curve showed increasing hysteresis. Sweeps with dwell times of 0.4 and 0.6 seconds were subsequently performed with evolving hysteresis evident. A final sweep with a shorter dwell time was performed to assess if the curve evolution was merely an evolution based on sweep order rather than a time dependence. The dwell time was reduced to 0.1 seconds for the final sweep. Reducing the dwell time, and hence increasing the data acquisition frequency, does indeed cause a reduction in the current going through the device. The reduction does not return the device to the state observed

in the initial sweep. An overlap in the two 0.1 second dwell time current-voltage curves would be observed in an ideal memristor. The time dependant nature of current-voltage measurements of a memristor are presented in figure 7.9.

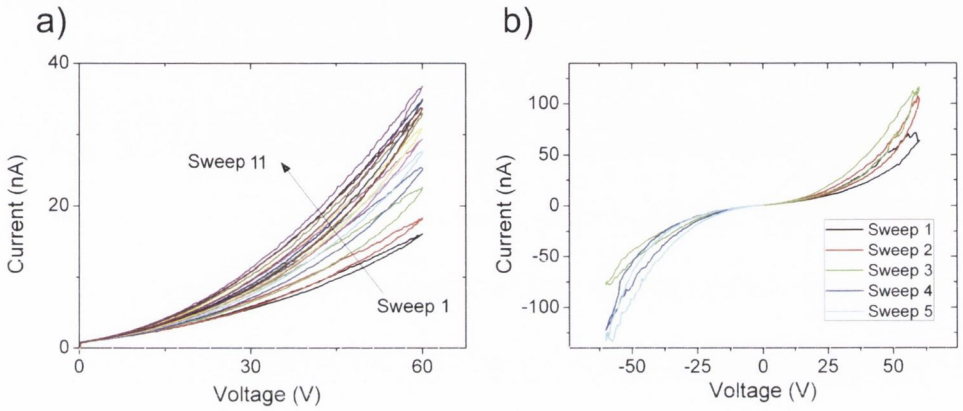

Figure 7.10: *(a) Repeated current-voltage measurements performed on a copper nanowire network. An reduction of high bias resistance is observed on each sweep. This incremental increase in current is a memristor like characteristic. (b) Current-voltage sweeps to assess memristor like behaviour. The positive sweeps resulted in an increase in current, as is expected in a memristor, however, the negative sweeps also resulted in an increase in current, behaviour not associated with a memristor.*

An examination of the continued evolution of the current-voltage curves of copper nanowire networks was performed on a different device. The device was fabricated identically to that described in this section and had electrode dimensions identical to those presented in figure 7.6 (b). Current-voltage data, obtained from 11 identical sweeps are presented in figure 7.10 (a). A continued evolution of the curve is evident through each curve swept. Remarkably, each sweep results in a lower resistance at 60 V than the previous sweep. This evolution like behaviour was not observed in short channel nickel oxide nanowire networks.

To assess memristor behaviour, the voltage was swept $0 \rightarrow V_{\mathrm{max}} \rightarrow 0 \rightarrow V_{\mathrm{max}} \rightarrow 0 \rightarrow V_{\mathrm{max}} \rightarrow 0 \rightarrow -V_{\mathrm{max}} \rightarrow 0 \rightarrow -V_{\mathrm{max}} \rightarrow 0 \rightarrow -V_{\mathrm{max}} \rightarrow 0$, and the resulting current voltages presented in figure 7.10. Current voltage curves similar to those presented in 7.9 (b) would indicate the memristance nature of the device. Curve

evolution was observed during the sweeps, figure 7.10 (b), however on the final two sweeps, sweeps 4 and 5, rather than collapsing back to a higher state of resistance, as a result of vacancies receding, the curves continued to evolve.

Copper nanowires presented in this section have shown a one way memristance like behaviour. There appears to be no work in the literature showing this memristance like behaviour and such interesting behaviour in not just short channel copper nanowire networks, but also large scale dense nickel nanowire networks, deserves to be further investigated.

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Conclusions

Memory devices are the subject of much research over the last 40 years, a summary of the emerging memory technologies was presented in Chapter 1.

Chapter 2 outlined the equipment used in the fabrication and analysis of the materials detailed in Chapters 3-7.

Chapter 3 described the extraction and subsequent selective deposition of nickel nanowire networks for resistive switching. The lithographic process to electrically contact these networks for characterisation was detailed. Selective deposition utilising PMMA and lift-off was detailed. We believe this is a novel method to selectively deposit nanowire networks, as well as individual nanowires.

Chapter 4 detailed the electrical properties of these nickel nanowire networks. The various switching operations were detailed as well as the memory window exhibited by these networks. ON/OFF ratios as high as 10^7 were demonstrated. The length dependence of the SET voltage and non dependence of RESET voltage demonstrates that the failure of the conductive filaments occurs at individual nanowire-nanowire junctions, rather than at each junction bridging the channel.

Controlled ambient annealing of nickel nanowires was presented in Chapter 5 along with electrical measurement performed on individual wires. Void formation due to thermal anneal results in an insulating state. This insulating void prevents current transport along the wire.

Chapter 6 details the two switching mechanisms available in nickel nanowire networks, the switching can be tuned simply by varying the compliance current applied during the FORM and SET operations. This control of the nanowire switching enabled the fabrication of a switch cell and a memory cell in series.

Chapter 7 detailed the properties of two distinctly different systems that exhibit remarkably similar properties. Short channel copper nanowire networks and large scale nickel nanowire networks were electrically characterised. Both systems acted in ways similar to that of a memristor, albeit, only evolving in one direction. The large nickel network acted in a totally different manor to the short channel. Dimensions roughly one order of magnitude wider and longer resulted in far more possible conductive pathways. Once the device had undergone a FORM operation it could not be RESET, rather the conductance of the device continued to increase. This we believe is due to the evolving nature of the network, more and more pathways becoming activated and contributing to the overall reduction in conductance.

Short channel copper nanowire networks exhibited a similar behaviour to the large scale nickel nanowire networks. The networks could not be SET, but rather the conductance gradually increased, much the same way a memristor would. However, a true memristor would undergo a lowering of the conductance during reverse voltage sweeps. This behaviour was not observed, however the initial results are enough to encourage further research in this area with nanowire systems like TiO_2 and Bi_2Te_3.

List of Publications

- A safe-by-design approach to the development of gold nanoboxes as carriers for internalization into cancer cells Movia, Dania Valerie Gerard, Ciaran Manus Maguire, Namrata Jain, Alan P. Bell, Valeria Nicolosi, Tiina O'Neill, Dimitri Scholz, Yurii Gun'ko, Yuri Volkov, Adriele Prina-Mello, Biomaterials 35, 9, 2543 (2014)

- Synthesis, structural, photophysical and electrochemical studies of various d-metal complexes of btp [2,6-bis(1,2,3-triazol-4-yl)pyridine] ligands that give rise to the formation of metallo-supramolecular gels Joseph P. Byrne, Jonathan A. Kitchen, Oxana Kotova, Vivienne Leigh, Alan P. Bell, John J. Boland, Martin Albrecht, Thorfinnur Gunnlaugsson, Dalton Trans. 43, 1 ,196 (2014)

- Polymer reinforcement using liquid-exfoliated boron nitride nanosheets Umar Khan, Peter May, Arlene O'Neill, Alan P. Bell, Elodie Boussac, Arnaud Martin, James Semple, Jonathan N. Coleman, Nanoscale 5, 2 581 (2013)

- Single crystal iron nanocube synthesis via the surface energy driven growth method Curtis O'Kelly, Soon Jung Jung, Alan P. Bell, John J. Boland, Nanotechnology 23, 43, 435604 (2012)

- Manipulating Connectivity and Electrical Conductivity in Metallic Nanowire Networks Peter N. Nirmalraj, Allen T. Bellew, Alan P. Bell, Jessamyn A. Fairfield, Eoin K. McCarthy, Curtis O'Kelly, Luiz F. C. Pereira, Sophie Sorel, Diana Mo-

rosan, Jonathan N. Coleman, Mauro S. Ferreira, John J. Boland, 12, 11, 5966 (2012)

- Free-Standing, Single-Crystal Cu_3Si Nanowires Soon Jung Jung, Tarek Lutz, Alan P. Bell, Eoin K. McCarthy, John J. Boland, Crystal Growth and Design 12, 6, (2012)