

Rapid Thermal Oxidation of Ge-rich Strained Layers

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Abstract – In this paper, we report for the first time the electrical properties of ultrathin oxides grown using rapid thermal oxidation (RTO) on strained Ge-rich layers on relaxed-SiGe buffers. Rapid thermal oxidation on strained Ge-rich layer is employed to prevent strain relaxation. Electrical properties of MOS capacitors fabricated using RTO grown oxides directly on strained Ge-rich has been studied in detail using capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) characteristics. Interface trap density, fixed oxide charge density, the frequency dispersion and hysteresis effects of the oxide have been determined. From the I-V characteristics, the current conduction mechanism has also been studied. RTO grown oxides show good electrical properties and may find applications in the future generation Ge-CMOS as a gate dielectric.

I. INTRODUCTION

As bulk-Si reaches its fundamental limits with the demand of high performance CMOS technologies and faster scaling of the devices, new device structures are implemented to suffice the need [1]. One of the promising candidates is Ge owing to its narrow band gap, high hole mobility (roughly four times that of bulk-Si) and high solubility limits of p-type dopants. With the advent of SiGe technology and its subsequent development with higher Ge concentration, there has been an urgent need to establish an effective passivation layer on Ge surfaces. In the last few decades, efforts have been made to realize stable oxide layers on Ge [2]-[4] by various oxidation processes. Unlike Si, however, the lack of a stable native oxide hinders the passivation of Ge surfaces. Again a number of dielectric like Ge oxynitride [5], Ge_3N_4 [6] and Al_2O_3 [7] have been

attempted on Ge surfaces. However, none of them has been able to offer an equivalent oxide thickness (EOT) of less than 10 Å to advance the current technology beyond sub-20 nm regime. In this study, we have successfully employed rapid thermal oxidation process for the growth of good quality oxide on strained Ge-rich layers grown on virtual substrates. In case of strained-Ge layers, it is important that the oxidation should not cause strain relaxation. Studies have revealed RTO as a means to prevent strain relaxation due to its low thermal budget [8]. Another advantages of this process are its high temperature ramp up rate (and hence a reduced thermal exposure) and a good control of oxide thickness. Strain relaxation has also been minimized with the use of virtual substrate [9] as growth of SiGe buffer layer on the bulk-Si reduces the dislocation and defects.

II. EXPERIMENTAL

The starting substrate was n-type Si (100) with resistivity 10-20 $\Omega\cdot\text{cm}$. The wafer was cleaned in four separate baths before loading in the process chamber. First the wafer was dipped in 10:1 HF solution for 1 min to remove the native oxide. Then they were cleaned in 1:1 H_2SO_4 and H_2O_2 solution, followed by a dip in 10:1 HF solution for 1 min to remove the thin oxide formed during cleaning. In the next step, the wafer were cleaned in megasonically agitated solution of NH_4OH , H_2O_2 , and H_2O to remove particles residing on the surface of the wafer and dipped in 10:1 HF solution for 1 min to remove the oxide. Finally, the wafers were exposed to 48% HF for 1 min for hydrogen surface passivation immediately before loading into load lock. From loadlock the wafer are transferred to the process chamber by robotic arm.

Relaxed graded- $\text{Si}_{1-x}\text{Ge}_x$ buffers with $x = 0-0.6$ of 0.8-1.0 μm thickness were grown by UHV compatible LPCVD at 800°C. In order to avoid high surface roughness generally relaxed graded buffers are chemically mechanically polished (CMP) to remove the surface roughness associated with mismatched heteroepitaxial layers [10]. This process minimizes subsequent dislocations and reduces defect densities. On this substrate, strained Ge-rich layers of 0.15-0.2 μm thicknesses were grown in the process chamber and on top of it sacrificial Si cap layer was deposited. The process gases used were SiH_4 and GeH_4 and working pressure was kept between 0.092-

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0.150 Torr. The total film thickness was kept between 1-1.2 μm . The structure of the layers is shown in the Fig. 1.

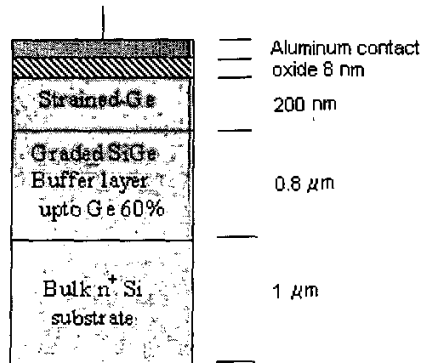


Fig. 1. Schematic diagram of MOS structure.

The oxide was grown on the strained Ge-rich layers by the process of rapid thermal oxidation (RTO) at a temperature of 620°C for 105 s. The ramp up rate of the rapid thermal processor is 30°Cs⁻¹ while the ramp down rate is low. A cross sectional image of strained-Ge structure were obtained from TEM micrograph using PHILLIPS TECHNAI F20. The field emission gun produces a potential of 200 kV. Prior to TEM, the sample is subjected to mechanical grinding followed by Ga⁺ ion milling. Raman spectral analysis was registered in backscattering geometry using a RENISHAW 1000 micro-Raman system equipped with LEICA microscope. The power density was kept below 105 mWcm⁻² to reduce the sample preheating. The measurements were performed at room temperature with Ar⁺ laser. An 1800 lines/mm grating was used in all measurements with spectral resolution of ~ 2.5 cm⁻¹ per pixels. The 100 times magnifying objectives of the Leica microscope focuses the beam into the spot of about 1 μm in diameter. MOS capacitors were then fabricated by depositing aluminum circular dots on the sample of area 1.96×10^{-3} cm². The electrical measurement including C-V dispersion, I-V and hysteresis in the C-V characteristics were carried out using HP-4061A semiconductor test system.

III. RESULTS AND DISCUSSIONS

The cross-sectional TEM image in Fig. 2 shows the complete picture of heterostructure layers. It also reveals an undulation in the film surface as the growth is carried out at an elevated temperature. It is found that the compressively strained-layers starts to undulate at wavelengths approximately 100 nm. It is noticed that the entire Si cap layer have been used up for the growth oxide layers. Fig. 3 shows that the Raman peaks are present at wave numbers

of 400 cm⁻¹ and 465 cm⁻¹ due to, Si-Ge and Si-Si bonds respectively.

The spectral lines are fitted with Lorentzian or Gaussian functions. The strain level determines the phonon energy obtained in the Raman peaks and thus can be used to extract strain of the heterolayers. The strain in the layer was found to be 0.01688. Similar peaks for the Si_{0.3}Ge_{0.7} are shown in [11] and [12].

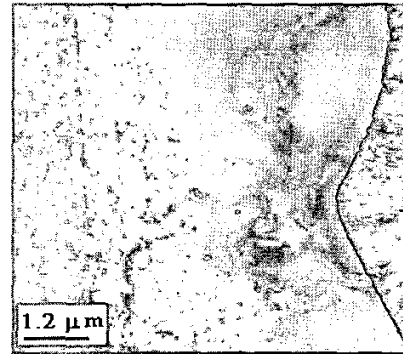


Fig. 2. TEM micrograph of strained-Ge layers.

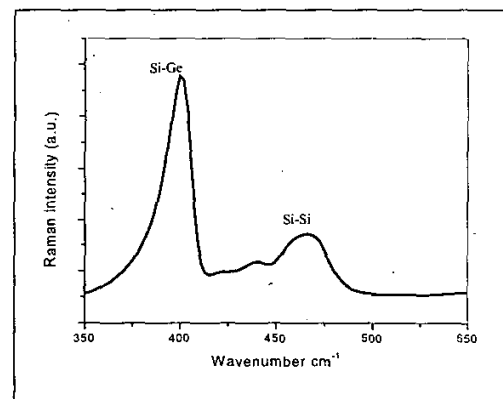


Fig. 3. Raman spectra of strained-Ge.

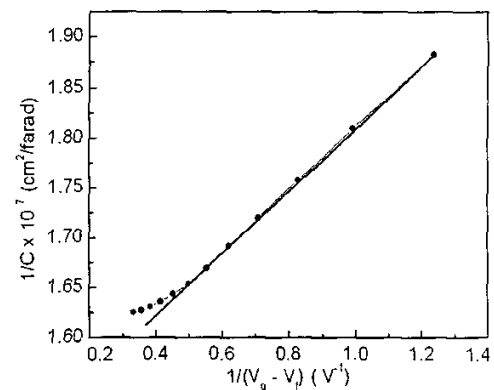


Fig. 4. $1/C$ vs. $1/(V_g - V_T)$ plot.

The thickness is measured from $1/C$ vs. $1/(V_g - V_{fb})$ [13] plot at high frequency found to be $80 \pm 3 \text{ \AA}$ as shown in Fig. 4. The C-V dispersion (Fig. 5) shows a shift in the flat-band voltage in the positive bias and stretch of C-V characteristics with the increase of frequency. This may be attributed to the presence of interface traps and mobile oxide charges. The interface trap density is evaluated by Hill's method at the midgap energy value from C-V and G-V characteristics is found to be $7.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and the fixed oxide charge density obtained from C-V characteristics is found to be $1.35 \times 10^{12} \text{ cm}^{-2}$. Similar results were reported by Benamuna et al. [14]. It may be noticed that at a comparatively low frequency the capacitance in the accumulation decreases with the increase of applied field which may be due to conduction of charges across the oxide layers. The dispersion in the inversion is mainly attributed to the effect of resistance of at the semiconductor oxide interface and the substrate back contact. The hysteresis in the high frequency C-V characteristics is obtained from double voltage sweep from inversion to accumulation and back to inversion. The hysteresis voltage is found to be 56 mV (Fig. 6). Similar results were also reported by Chui et al. [15].

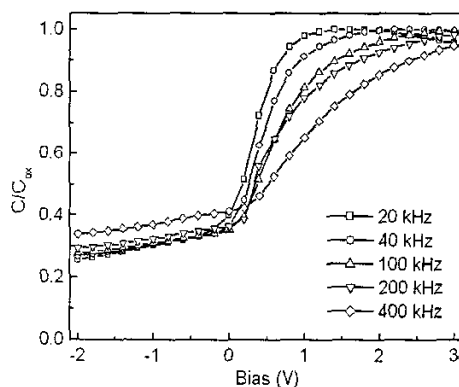


Fig. 5. C-V dispersion of RTO grown MOS on strained-Ge.

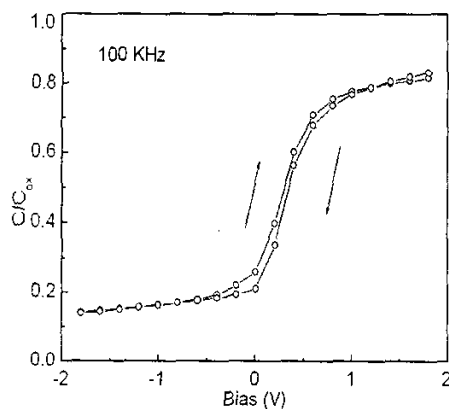


Fig. 6. C-V characteristics of RTO grown MOS.

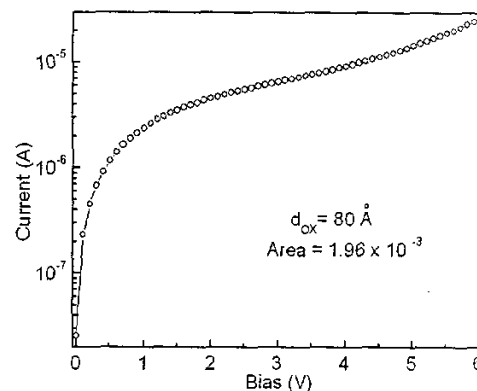


Fig. 7. Typical I-V characteristics of RTO grown MOS.

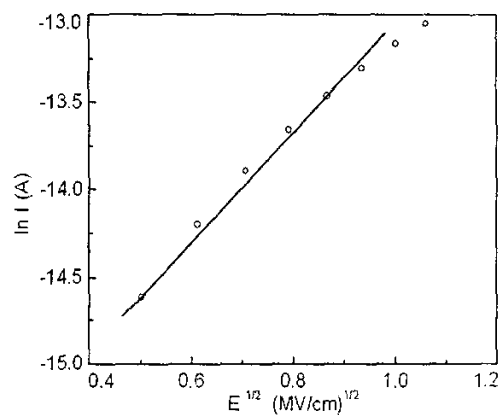


Fig. 8. $\ln(I)$ vs $E^{1/2}$ plot: Schottky emission characteristics.

The I-V characteristics in Fig. 7 show the current in the accumulation region for n-type substrate. To determine the dominant leakage current mechanism in the oxide layer a plot of $\ln(I)$ versus $E^{1/2}$ (Schottky emission mechanism) is commonly used (Fig. 8). RTO grown oxide on strained-Ge shows clearly a linear relationship and the conduction mechanism is dominated by the Schottky emission at room temperature [16]. It is noted that the Schottky emission occurs as a result of lowering of the columbic potential barrier due to free carrier generation out of the defect centers and traps under the applied electric field. The phenomena may be considered as electrode limited, occurring at low voltage where carriers at the metal surface or semiconductors transit above potential barrier and are prominent in thin films.

IV. CONCLUSION

The results of our studies on the electrical characteristics of MOS capacitors fabricated using RTO

grown oxides directly on strained Ge-rich layers reveal a reasonably good reliability. The leakage current through the oxide is comparable to that of conventional SiO₂ grown on Si-substrates. The low hysteresis voltage also indicates a good reliability of the oxides grown directly on strained Ge-rich layers. It is expected that the strained Ge-rich heterolayers can possibly immerge as a suitable candidate for the next generation high performance Ge-CMOS technology.

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