

A Study of Electronic Structure and Thermal Stability of Engineered SOI Material



A thesis presented to the University of Dublin, Trinity College
for the degree of
Doctor of Philosophy in Chemistry

2017

Barimar Prabhava Sai Narayana

Under the supervision of Prof. John Boland
School of Chemistry & CRANN
Trinity College Dublin

DECLARATION

I, the undersigned, declare that this work has not previously been submitted as an exercise for a degree at this, or any other University, and that unless otherwise stated is my own work. Elements of this work that have been carried out jointly with others or by collaborators have been duly acknowledged in the text.

I agree to deposit this thesis in the University's open access institutional repository or allow the library to do so on my behalf, subject to Irish Copyright Legislation and Trinity College Library conditions of use and acknowledgement.

Barimar Prabhava Sai Narayana

Date

SUMMARY

The objective of this thesis is to provide new insights into the properties of silicon-on-oxide (SOI) and the stability and electronic structure of patterned SOI. Any freshly formed silicon surface is highly reactive and in the presence of oxygen the surface immediately forms a thin layer of oxide known as a native oxide. Surface analysis of silicon samples by scanning tunneling microscopy – a key focus of this work - requires removal of the native oxide before measurement. Removing the thin native oxide layer from silicon in an UHV environment involves annealing and processing SOI at elevated temperature in a manner that avoids damage to the device layer. The potential for modifying the chemical composition on the surface, the potential for contamination and loss of dopants, and potential loss of the structural integrity of the device layer are all major issues. In order to address this challenge, a low thermal budget process was developed and the thermal decomposition of the native oxide in UHV has been investigated using various surface analysis techniques. The evolving morphology and chemical composition of the native oxide and the SOI device layer were investigated as a function of anneal temperature and duration. An elaborate ex-situ cleaning process has been developed to both reduce the contamination and cap the surface with a chemically grown ultra-thin oxide. The annealing parameters to desorb oxide without disturbing the integrity of the device layer were optimised that enabled surface analysis of ultra-thin SOI films and nanostructures fabricated from SOI.

Following the refinement of the surface cleaning and preparation process, the capability of scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) to study nanoscale Si(100) device layers in silicon-on-insulator (SOI) was demonstrated. The device layer is a macroscopic 2D silicon sheet and understanding the effective coupling of charge in and out of this sheet determines whether it is possible to accurately measure the electronic properties of the sheet by STM techniques. Specifically, how spreading resistance manifests in STM following the processing of SOI device layers with various doping levels have been analysed. Depending on the doping level, ultra-thin SOI exhibited significant blue

shifts of the peaks in the tunneling and field emission spectra. By comparing these peak shifts with the film resistivity it is shown that the contribution of spreading resistance in STM and STS can be estimated. It is also shown that STM can be used to study the effective n-type dopant concentrations in the 10^{13} - 10^{16} cm⁻³ range. It was also demonstrated that ultra-thin SOI with sufficiently high doping levels ($\sim 10^{20}$ cm⁻³) and device layer thicknesses down to 5 nm can be studied with STM and that these materials exhibit bulk like electronic characteristics.

The evolution of the morphology of silicon-on-insulator (SOI) due to annealing in an UHV environment was also investigated. Thin SOI films deform at high temperatures into 3D crystals in a process known as dewetting. The process is driven by surface energy minimization and occurs via surface diffusion. The dewetting process in SOI is known to start with the nucleation of voids in the film and grows via capillary edge and Rayleigh instabilities. In this work, preliminary measurements have suggested that SOI with thicknesses below 4 nm dewet spontaneously through a process that involves thermally driven fluctuations of the film thickness. STM measurements have shown that annealing 3 nm SOI film produces low energy facets along with a wave-like modulation of the surface roughness. Supporting evidence was also provided in the form of SEM and AFM measurements, which show the presence of thickness fluctuations in the film which is known to be a characteristic of films dewetting via the growth of thermal fluctuations. KPM measurements showed clear evidence of the presence of an ultra-thin wetting layer between the dewetting crystals of a 3 nm SOI film, consistent with the emergence of a new dewetting mechanism at these thicknesses.

Finally, surface analysis of silicon nanowires of different widths, fabricated from SOI wafers using electron beam lithography was investigated. Due to the capillary edge and Rayleigh instabilities, the edges of patterned SOI and nanowires fabricated from SOI dewet at a reduced temperature when compared to non-patterned SOI, making the surface analysis of these nanowires challenging. Nonetheless, we have shown in this work that nanowires can be processed in UHV using low thermal budget flashing and then analysed with STM. The reduction in thermal budget is believed to be due to the edge effect along the length of the

nanowires. An increase in surface diffusion of silicon atoms away from the edges due to capillary forces expedites the oxide desorption process in the nanowires. By carefully controlling the thermal process, nanowires can be prepared without affecting their structural integrity. However, if annealed further, capillary forces deform the edges of the nanowires and finally lead to the formation of a row of crystals due to Rayleigh instability. The findings in this work shows that surface analysis of ultra-small silicon nanowires on insulator structures is possible. In order to carry out the surface analysis on smaller nanostructures beyond the limits of EBL, a simple nanowire and nanodisc fabrication technique has been developed. Commercially available TiO_2 nanowires and nanoparticles spray deposited over SOI were used as an etch mask to fabricate silicon nanowires and nanodiscs from SOI. Studies of the newly patterned wires and dots are currently underway.

Acknowledgements

As I get a step closer towards realizing my dream of completing my higher studies, I would like to thank some of the most important people who supported and helped me at various stages.

First and foremost I would like to express my profound sense of gratitude to my PhD supervisor, Prof. John Boland for giving me the opportunity to pursue a PhD. I would also like to thank him for his constant support, guidance, encouragement and patience throughout the course of my PhD, without which this thesis would not have been possible. I am also grateful to Science Foundation Ireland (SFI) for the gracious funding.

I would like to thank all the members of the Boland group, past and present, but in particular Catherine, Jing, Borislav, Xiaopu, Shaun, Sam, Peter, Hugh, Felim, David, Mallik, Emmet, Fabio, Sahar and Rishab. Special thanks to Catherine, Shaun and Sam for proof-reading this thesis. Thanks to all members of CRANN and the AML who helped over the years, especially, Mike, Dermot, Clive, Eoin, Niall, Chris and Venky. I am also grateful to Mary for all the admin support.

I would also like to thank the people who supported and guided me during different stages of my education, especially Prof. K. P Ramesh, Dr. Vijay Mishra, Dr. Gajanana Honnavar, Prof. Sriprakash, Dr. G. M. Jagadish, Vinay Bhushan and Suma.

On a personal note I am grateful to Appa, Amma and Swathi, who have always been there for me. I am thankful for their immense love and endless support throughout my life. I would also like to express my sincere gratitude to my uncles Ashok Barimar, Shyam Sunder and Sadhashiva Rao for their enormous support. I am thankful to my dear friends Akshara and Ramya for their support when it was most needed.

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION.....	1
1.1 Chemical etching of oxide.....	5
1.2 Thermal processing of SOI.....	5
1.3 Formation of SiC surface structures.....	6
1.4 Diffusion of dopants.....	6
1.5 Spreading resistance.....	7
1.6 Dewetting.....	9
1.7 Capillary-induced surface diffusion.....	11
1.8 Rayleigh Instability.....	12
1.9 References.....	14
CHAPTER 2 EQUIPMENT AND METHODS.....	22
2. 1 Ultra-high vacuum.....	22
2.2 Scanning tunneling microscopy (STM).....	23
2.2.1 Elastic tunneling through a one-dimensional rectangular potential barrier.....	23
2.2.2 Elastic tunneling through a one-dimensional potential barrier of arbitrary shape.....	25
2.2.3 Elastic tunneling in planar metal-insulator-metal (MIM) tunnel junctions.....	25
2.2.4 Quantum mechanical tunneling as applied to STM.....	27
2.2.5 STM – Experimental details.....	29
2.2.6 Tunneling spectroscopy.....	30
2.2.7 Field emission spectroscopy.....	32
2.2.8 Experimental details.....	33
2.2.9 Tip preparation.....	35
2.3 Low energy electron diffraction (LEED)	36

2.4 X-ray photoelectron spectroscopy (XPS).....	38
2.5.1 Atomic Force Microscopy (AFM).....	39
2.5.2 Phase contrast imaging.....	42
2.5.3 Kelvin probe microscopy (KPM).....	44
2.6 Electron microscopy.....	46
2.6.1 Scanning electron microscopy (SEM).....	46
2.6.2 Electron beam lithography (EBL).....	47
2.6.3 Transmission electron microscopy (TEM).....	48
2.7 Inductively coupled plasma – Reactive ion etching (ICP-RIE).....	48
2.8 Spectroscopic Ellipsometry.....	49
2.9 Secondary Ion Mass Spectroscopy (SIMS).....	50
2.10 References.....	52
CHAPTER 3 THERMAL TREATMENT OF SILICON-ON-INSULATOR.....	58
3.1 Introduction.....	59
3.2 Experimental details.....	60
3.3 Test chamber.....	61
3.4 Chemical etching of oxide.....	62
3.5 Thermal desorption of oxide layer.....	64
3.6 Surface compositional analysis after annealing.....	69
3.6.1 X-ray photoelectron spectroscopy.....	69
3.6.2 AFM phase analysis.....	73
3.7 Elimination of surface carbide and STM analysis.....	76
3.8 Conclusion.....	79
3.9 References.....	80
CHAPTER 4 SPREADING RESISTANCE AT THE NANOSCALE STUDIED BY SCANNING TUNNELING AND FIELD EMISSION SPECTROSCOPY.....	86
4.1 Introduction.....	87
4.2 Experimental details.....	88
4.3 Tip quality determination.....	91

4.4 Topographic phase transition in Si (100) (2×1) STM.....	92
4.5 Voltage shift in STM and STS.....	94
4.6 STS blue shift vs band gap widening in Si thin film.....	96
4.7 Sample resistance in STM.....	98
4.8 Work function determination through KPM.....	101
4.9 Tip induced band bending in Si(100).....	102
4.10 Spreading resistance.....	104
4.11 Annealing and dopant re-distribution.....	107
4.12 STM and STS of < 12 nm SOI.....	110
4.13 Conclusion.....	111
4.14 References.....	114
CHAPTER 5 THERMAL STABILITY OF ULTRA-THIN SOI.....	118
5.1 Introduction.....	119
5.2 Experimental details.....	120
5.3 Surface studies of annealed ultra-thin SOI.....	121
5.4 Kelvin probe microscopy of annealed 3 nm SOI.....	128
5.5 Different dewetting mechanisms in SOI device layer.....	131
5.6 Conclusions.....	137
5.7 References.....	139
CHAPTER 6 THERMAL PROCESSING OF PATTERNED SOI NANOWIRES.....	142
6.1 Introduction.....	143
6.2 Experimental detail.....	144
6.2.1 Nanowire design considerations.....	144
6.2.2 Electron beam lithography (EBL) and nanowire edge smoothening.....	145
6.3 Edge effect: oxide desorption and dewetting.....	146
6.4 STM analysis of SOI nanowires.....	148
6.5 TiO ₂ nanowire masked Si nanowires.....	151

6.6 Conclusion.....	155
6.7 References.....	156
CHAPTER 7 CONCLUSIONS AND FUTURE WORK.....	159

LIST OF FIGURES

1.1	Diagram illustrating the electronic density of states depending on the dimensionality.....	2
1.2	Cross-sectional profile of the SOI.....	3
1.3	Schematic showing equipotential surface and current density for a circular metal contact on a semiconductor.....	7
1.4	Schematic illustration of the equilibrium shape of a thin film, assuming isotropic surface energies and a rigid substrate, as determined by Young.....	9
1.5	Schematic illustration of the capillary instability.....	12
1.6	Graphical illustration of the Rayleigh instability.....	13
2.1	Wave function $\psi(x)$ for an electron with energy E interacting with a one dimensional potential barrier with height V_0 and width s	24
2.2	Arbitrary shaped potential barrier between two metal electrodes..	26
2.3	Illustration of the Bardeen approach to tunneling theory.....	28
2.4	Schematic diagram of a typical scanning tunneling microscope....	29
2.5	Energy level diagrams for sample and tip.....	31
2.6	Example of scanning tunneling spectroscopy data.....	31
2.7	Energy diagram for field emission and a typical $z(U)$ and dz/dU spectra for Si(100) taken with a Pt tip.....	32
2.8	Schematics of the LT-STM.....	34
2.9	Shows a direct heating and indirect heating STM sample holder...	34
2.10	Schematic representation of an electrochemical cell showing the etching of a tungsten wire to form a STM tip.....	36
2.11	Bragg diffraction.....	37
2.12	Schematic of a LEED experimental set-up and an example of LEED pattern.....	37
2.13	Force – Distance plot showing the interaction of an AFM tip with the surface.....	40
2.14	Illustration of the basic components of an AFM.....	41
2.15	Schematic of a Q-plus AFM/STM sensor.....	41
2.16	The phase lag changes depending on the mechanical properties of the sample surface.....	42
2.17	Ideal tip and sample electronic energies at the vacuum level E_{vac} and Fermi level E_F , for the case of dissimilar work function.....	44
2.18	LiftMode principles used in CPD measurements.....	45
2.19	Schematic of the various interactions between the electron beam and the sample.....	47

2.20	Interaction of the linearly polarized light with the sample.....	49
3.1	Schematic and an image of the standalone UHV chamber demonstrating different parts.....	61
3.2	H-passivated 12 nm SOI surface after flash annealing at 700 °C...	63
3.3	Schematic of the stages of thermal desorption.....	64
3.4	SEM images showing six different regions along the centre of a 50 nm SOI samples after annealing at 750 °C, ten cycles of 60 s duration each.....	65
3.5	SEM images of a 50 nm SOI sample after ten anneal cycles at 750 °C, each lasting 30 s.....	67
3.6	SEM images of a 50 nm SOI after ten cycles of annealing at 750 °C, each for a duration of 90 s.....	68
3.7	SEM data for a 50 nm SOI sample annealed at 690 °C for 60 min.....	69
3.8	XPS measurements showing the Si 2p core level for a pristine and a flashed SOI.....	71
3.9	XPS measurements showing the C 1s core level for a pristine and a flashed SOI.....	72
3.10	Topography and phase contrast AFM images measured across a 50 nm SOI sample after 10 anneal cycles at 750 °C, each lasting 60 s.....	74
3.11	Topography and current error STM images of a pristine 50 nm SOI sample after 10 anneal cycles at 750 °C, each lasting 90 s.....	77
3.12	Si thinning rate and oxide growth rate plotted against the ICP time.....	78
4.1	Shows the schematic of sample preparation for KPM measurements, with device layer thickness varying between 45 nm and 3 nm.....	89
4.2	Typical 2x1 LEED pattern observed at room temperature, for the Si(100) SOI samples of different device layer thickness after flashing.....	90
4.3	Shows an I-V and a dI/dV spectra of a metallic and non-metallic tip.....	91
4.4	Typical tunneling spectra for a bulk Si(100) (2x1) surface, indicating the occupied (π) and empty state (π^* and σ^*) spectral features.....	92
4.5	Constant-current filled state topographic images recorded at +1 V and +0.5 V, depicting the image contributions due to σ^* and π^* states, respectively.....	93

4.6	Tunneling (IV) and field emission (z(V)) spectra of thinned SOI showing blue shift; Multi bias STM image showing ‘topographic phase transition’ (PT).....	95
4.7	Voltage shift observed in STM and STS measurements as a function of SOI film thickness.....	96
4.8	Peak shift observed in STM, STS and field emission spectroscopy plotted as a function of SOI thickness, showing a sharp increase in the shifted value below 16 nm.....	97
4.9	Four point resistivity of SOI as a function of device layer thickness.....	98
4.10	Doping concentration for SOI of varying thickness calculated from the resistivity data measured at 300 K and 77 K plotted along with the SIMS data; Comparison between sample resistance and tunneling resistance at 2V, 20 pA set-point.....	100
4.11	KPM image showing the contact potential difference (CPD) for two regions of SOI with respective thickness of 9 nm and 3 nm and an Au reference film; Workfunction of SOI plotted as function of thickness.....	102
4.12	Schematic illustration of tip-induced band bending for n-type Si(100)-(2×1) for $V_{\text{sample}} \ll 0$ and $V_{\text{sample}} \gg 0$	103
4.13	z(V) spectra for 12 nm SOI showing the tip sample separation with the tip sample separation off-set values between 1 – 4 Å and normalized electric field between the tip and the sample surface calculated using the z(V) spectra.....	103
4.14	Schematic representation of tunneling in STM demonstrating the tip position over the sample, the effective tunneling area and the resistive components such as tunneling resistance (RT), spreading resistance (RSP) and sample resistance (RS); Graph comparing Rsp with STS and FES blue shift.....	105
4.15	Phosphorus concentration of 45 nm SOI film recorded with SIMS depth analysis following ten anneal cycles at 750 °C.....	107
4.16	Four point resistivity of SOI thinned after 10 anneal cycles at 750°C, plotted as a function of device layer thickness.....	108
4.17	Phosphorus concentration for doped un-annealed and annealed 12 nm SOI recorded with SIMS depth analysis.....	109
4.18	Scanning tunneling microscopy and spectroscopy of 5 nm SOI....	111
5.1	STM height image and spectroscopy of a 5 nm SOI.....	122
5.2	STM image of a flash annealed 3 nm SOI.....	123
5.3	STM 3D height images of the 3 nm SOI surface showing different surface features.....	124

5.4	Height line profile and spectra recorded on an annealed 3 nm SOI.....	125
5.5	SEM images of thickness fluctuations and dewetting captured in the same 3 nm SOI due to thermal gradient across the sample.....	126
5.6	Schematic illustration of the equilibrium contact angle considered in Young's equation.....	127
5.7	AFM and KPM data suggesting the possibility of freezing a transient morphology in annealed ultra-thin SOI: dewetting crystals inter-connected with an ultra-thin "wetting" film.....	130
5.8	SEM images showing different stages of dewetting of the SOI device layer.....	132
5.9	Schematic illustration of an interfacial wave in SOI oscillating at a wavelength λ showing the change in film thickness Δt resulting from the perturbation, where t_0 is the initial film thickness.....	134
5.10	Contrast corrected SEM image of a 6 nm annealed SOI.	135
5.11	Two dewetting modes: through hole nucleation and growth in thick SOI; through growth of thermal fluctuation in ultra-thin SOI.....	136
6.1	Schematic showing the design of the EBL Si nanowires and the EBL process.....	145
6.2	SEM images of 50 nm Si nanowires on a 10 nm SOI before and after oxygen plasma treatment.....	145
6.3	Edge effect in SOI.....	147
6.4	STM height image of a 50 nm wide SOI nanowires fabricated on an 8 nm SOI.....	149
6.5	A close-up of a 50 nm wide nanowire on SOI showing a clean Si(100) (2×1) surface and a typical STS spectra recorded on the nanowire.....	150
6.6	Different stages of thermal instability in Si nanowires on SOI.....	151
6.7	Schematic of the TiO ₂ masked Si nanowires fabrication process...	153
6.8	SEM images showing low edge roughness nanostructures fabricated on SOI.....	154

LIST OF ABBREVIATIONS

AFM – Atomic Force Microscopy
BOX – Buried oxide
DOS – Density of states
EBL – Electron beam lithography
HF – Hydrofluoric acid
ICP – Inductively coupled plasma
KPM – Kelvin Probe Microscope
LDOS – Local density of states
LEED – Low-energy electron diffraction
MIM – Metal-Insulator-Metal
PT – Topographic phase transition
RF – Radio frequency
FES – Field emission spectroscopy
RIE – Reactive-ion etching
SEM – Scanning electron microscope
SOI – Silicon on Insulator
STM – Scanning tunneling microscopy
STS – Scanning tunneling spectroscopy
UHV – Ultra high vacuum
XPS – X-ray photoelectron spectroscopy

LIST OF PUBLICATIONS

Prabhava S. N. Barimar, Catherine M. Doyle, Borislav Naydenov, and John J. Boland, “*Study of the effect of thermal treatment on morphology and chemical composition of silicon-on-insulator*”, Journal of Vacuum Science & Technology B, 34, 2016, 041806

Prabhava S N Barimar, Borislav Naydenov, Jing Li and John J. Boland “*Spreading resistance at the nano-scale studied by scanning tunneling and field emission spectroscopy*”, Applied Physics Letters, 110, 2017, 263111

K. D. M. Rao, Prabhava S N Barimar, Emmet Sheerin and John J. Boland “Transparent Si nanowire network for high performance photo detectors” (In preparation)

1

INTRODUCTION

The electronics industry has been growing at an unprecedented rate, since the invention of the first integrated chip. This tremendous growth can be attributed to the exponential increase in the component density that can be integrated onto a single chip [2]. Moore's law [6, 7], which is an empirical observation and extrapolation made by Gordon Moore in 1965, states that the component density on an integrated circuit doubles every year. The forecast was later revised to the component density doubling every two years [6, 7]. Although Moore's law has been consistent for the last four decades, the growth rate has decreased, with the component density currently doubling every two to three years [2].

In 22 nm technology, a commercially available central processing unit (CPU) has over 2.9 billion transistors and a graphics processing unit (GPU) contains over 7 billion transistors [8]. As the component density in an integrated circuit increases, the device dimensions shrink. Currently, a typical transistor gate length in microprocessor circuits is about 18 nm – 13 nm [9]. The miniaturization of devices cause the performance and reliability of electronic micro-components to depend increasingly on the nanoscale quality of surfaces and interfaces [10]. Furthermore, with the dimensions of the devices reducing further, the properties of the material will eventually be dominated by quantum effects.

The properties of nanoscale materials, can be influenced greatly by variations in size [11-14], shape [15] and properties of their surfaces [11, 16]. For example, silicon nanocrystals have been shown to exhibit photoluminescence [12, 14], with tuneable wavelength [11]. These characteristics of nanomaterials create opportunities for making interesting devices including flexible, stretchable and

transparent devices [17]. Additionally, silicon nanostructures have an added advantage due to their compatibility with established semiconductor techniques. This provides a straightforward path for the integration of silicon nanomaterials into existing Si-based electronic platforms [17-20].

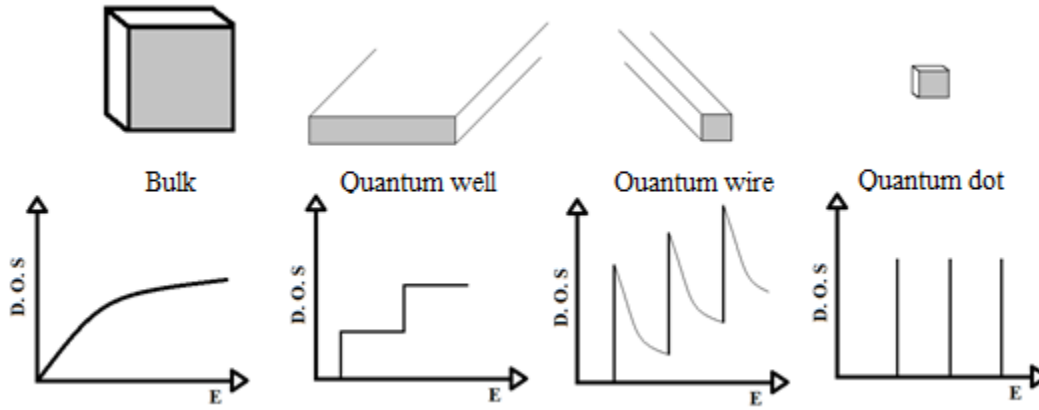


Fig. 1.1: Diagram illustrating the electronic density of states depending on the dimensionality [1].

Most of the physical properties of bulk materials are explained by assuming a collective contribution of an infinite number of atoms in the material. This assumption starts to break down when the material dimension is reduced to the nanoscale [21-24]. Nanoscale materials tend to exhibit new electronic [21], mechanical [17], optical [11, 22] and thermodynamic properties [25-27]. Fig. 1.1, for example, shows how the density of state (DOS) of different nanostructures vary in comparison to their bulk counterparts [1]. Furthermore, the variations in thickness of the nanostructures, even due to surface roughness, can significantly alter the DOS and affect the electron transport properties in the nanostructures [17]. At these dimensions, even the atomic scale environment of dopants, such as their proximity to surfaces can severely influence the dopant characteristics such as the shape of their wave function [28] and their ionization energy [29]. As a result, a detailed understanding of the atomic and electronic structure of nanomaterials and their surfaces remains a challenge.

Silicon nanostructures are expected to play a key role in future nanotechnology such as development of low power light emitting diodes and 1-D quantum-wire high speed field effect transistors [30, 31]. However, in order to

develop such devices, it is necessary to understand and control the atomic scale properties of nanomaterials. For conventional semiconductor devices, the local variations in the devices have minimal effect because the device functionality is based on statistically averaged properties of a large number of atoms. However, for nanoscale devices the local variations in the nanoscale properties become very important.

The objective of this thesis is to develop a systematic approach to study the properties of silicon based nanomaterials due to their particular importance in the electronics industry. Silicon-on-insulator (SOI) is an exceptional choice towards attaining this goal. SOI (Fig. 2) is a thin silicon film called the device layer that sits on top of an insulating layer of buried oxide (BOX), which itself sits on top of a bulk Si wafer. SOI is of a tremendous technological interest as it offers a possible means to achieve improved device performance [21, 32-34]. SOI devices provide reduced parasitic capacitances and leakage currents due to the dielectric isolation and deliver more than 20% improved performance with up to 40% reduction in

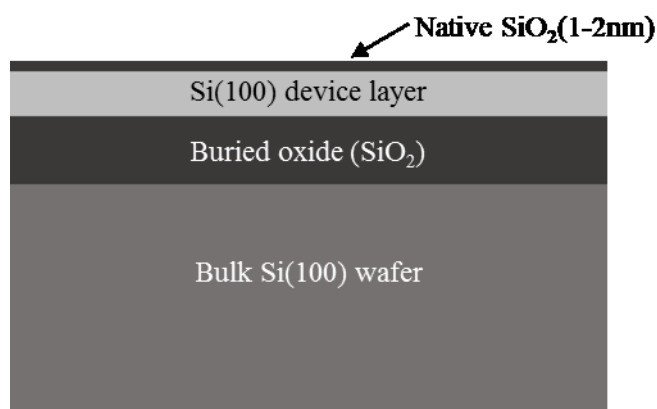


Fig. 1.2: Cross-sectional profile of the SOI

power consumption compared to bulk Si devices [35]. Furthermore, the SOI structure immensely simplifies the device fabrication process allowing easy formation and isolation of the Si device channels that are the heart of CMOS technology. SOI is also of fundamental scientific interest as the confinement of the electrons in the thin Si device layer may lead to different mechanical, electronic and optical properties compared to those of bulk Si [21, 32].

Although SOI structure provides a simple route to controllably fabricate silicon nanostructures and has immense industrial applications, it has not been explored as a platform to enable atomic level investigations of nanoscale silicon. Most of the SOI studies to date have involved in fabricating thin film and nanowire devices for device characterization [29-31] and area averaged spectroscopy [17,29]. There have been very few STM studies [28], probably due to the complex nature of the work, none of which have involved patterned substrates. The most notable STM studies on SOI are due to Lagally *et al* [21] who showed that room temperature STM is possible even in the absence of controlled doping and demonstrated anomalous conductivity of intrinsic SOI film. However, no STS experiments have been reported on SOI at room or cryogenic temperature.

This thesis attempts to study the electronic and thermo-mechanical properties of engineered SOI materials. The main goals of the thesis are: (i) develop a reliable SOI ultra-thin film and nanowire fabrication process, (ii) develop a low thermal budget ex-situ and UHV surface cleaning process, and subsequently use this process to (iii) study the electronic structure and thermomechanical properties of SOI nanostructures using scanning tunneling microscope. Specifically, this work aims to develop a test platform for the nanoscale engineering of arbitrary shaped silicon nanostructures on SOI material and investigate them at the atomic level.

An introduction to each relevant topic is given at the beginning of chapters 3-6 in order to provide context to the results and the conclusions drawn. In this chapter, a brief outline of the research material in this thesis is presented.

Due to the high reactivity of silicon, a freshly formed silicon surface immediately oxidises, forming a thin (1 - 2 nm) layer of oxide on the surface called a native oxide. The native oxide, being an insulator, hinders surface characterization, especially when using electron transport based measurements such as scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS). Surface analysis of silicon requires the native oxide to be removed before the measurements.

1.1 Chemical etching of oxide

There are several ways to remove native oxide from a silicon surface. One of the simplest techniques is to etch away the oxide layer in dil. hydrofluoric acid (HF). Since the etch rate of oxide in dil. HF is higher than that of the underlying silicon, the oxide layer can be etched without affecting the silicon. This etching process leaves the silicon surface passivated with hydrogen. However, the silicon surface passivated with hydrogen does not last long. The hydrogen bonds on the passivated silicon surface quickly react with oxygen and the oxide layer is regrown. Studies have shown that the hydrogen passivation is replaced with oxygen in less than 30 mins [36]. Furthermore, the hydrogen passivated surface and the residual dangling bonds of a Si dimer, react with hydrocarbons in the air to form two Si-C bonds [37-42]. On annealing, this hydrocarbon contamination forms SiC nanostructures on the silicon surface which severely hinders surface analysis. Therefore, chemical etching of native oxide prior to UHV processing is not a reliable surface cleaning technique for surface analysis.

1.2 Thermal processing of SOI

In ultra-high vacuum (UHV), the native oxide can be removed via a thermal desorption process [43-54]. At high temperatures, silicon dioxide (SiO_2) can react with silicon to form silicon monoxide (SiO) which eventually sublimates as shown by the equation



Typically, this process is carried out by heating samples to temperatures over 800 °C [32, 50, 55]. Sublimation of silicon monoxide from the surface forms voids in the oxide layer which eventually grows in size exposing the silicon beneath [32, 44, 52, 56]. This process removes the native oxide from the sample, resulting in an atomically clean surface [44, 52, 56]. Chapter 3 presents the challenges involved in the processing of SOI film without changing its chemical composition on the surface or loss of integrity of the SOI film. The processing parameters and the results of surface analysis are discussed in chapter 3.

Due to the small dimensions of the SOI structures, and high processing temperatures involved, thermal processing of SOI involves unique challenges that

are not issues in bulk silicon. The following sections briefly discuss some of the important challenges associated with thermal processing of SOI and SOI nanostructures and the chapters in which they are discussed in the thesis.

1.3 Formation of SiC surface structures

A clean silicon surface is crucial for surface studies. Thermal processing of silicon results in the removal of native oxide, nevertheless, at high temperatures, silicon also reacts with carbon contaminants and forms SiC structures on the surface according to the equation given by



The carbon contamination usually occurs due to *ex situ* processing, but the contamination can also occur due to outgassing of the sample holder and other UHV components at high temperatures.

1.4 Diffusion of dopants

The SOI device layer is actually sandwiched between two SiO₂ layers – buried oxide and native oxide. The presence of fixed charge in the oxide and the traps in the Si-SiO₂ interface, can cause the ultra-thin SOI device layer to become fully depleted of charge carriers [21, 32]. Even for the highest quality Si(100)-BOX interface, the interface trap density is on the order of 10¹⁰ - 10¹¹ cm⁻² [21, 32, 57]. In contrast, a 45 nm device layer doped at a typical 10¹⁵ cm⁻³ has only 10¹⁵ × 45 × 10⁻⁷ = 4.5 × 10⁹ majority carriers per cm⁻². Hence, SOI with device layer thickness lower than 45 nm (typical thicknesses considered in this study), with nominal doping (10¹⁵ cm⁻³), would be fully depleted of charge carriers. The lack of charge carriers in the film makes it difficult to carry out electrical transport measurements in fully depleted SOI [32, 57], especially at low temperatures. Therefore, in order to conduct surface analysis of SOI structures using STM, the device layer of SOI is doped over 10¹⁹ cm⁻³.

High temperature processing of doped silicon leads to diffusion of dopants [58], and a variation in the dopant density profile in the sample [59, 60]. Due to the high surface to volume ratio in nanostructures, segregation effects are more prominent than in bulk silicon [60]. High temperature annealing of doped SOI is also known to cause segregation of dopants at the interfaces and to form clusters

within the device layer [61-63]. Dopant segregation and clustering can significantly affect the electrical properties of the SOI film and nanostructures [61-63]. Details about diffusion of dopants and varying electrical properties are discussed in chapter 4.

1.5 Spreading resistance

A small area electrical contact (such as that associated with STM) results in an additional series resistance called the spreading resistance which arises due to the spreading of the current from the contact region. Spreading resistance was first explained by Maxwell in 1904 [64]. In this case, most of the voltage drops near the contact where the current density is

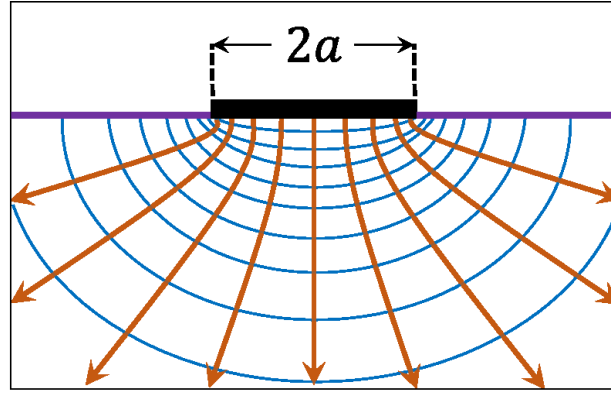


Fig. 1.3: Schematic showing equipotential surface and current density for a circular metal contact on a semiconductor [4].

the highest and the current density and hence the resistance approaches zero far from the contact. A schematic of current density in a semiconductor from a circular metal contact with radius a is shown in Fig. 3. The brown lines in Fig. 3 shows the current lines and the blue lines show the equipotential surface for the current flowing through the circular contact. The equipotential surfaces in the contact consists of an ellipsoid defined by the equation

$$\frac{r^2}{a^2 + \mu^2} + \frac{z^2}{\mu^2} = 1 \quad (1.3)$$

Where μ is the length of the vertical semi-axis of the ellipsoid and (r, z) are the cylindrical coordinates. The resistance between the equipotential surface with semi-axis μ and the contact is given as [65]

$$R_{\mu} = \frac{\rho}{2\pi} \int_0^{\mu} \frac{d\mu}{(a^2 + \mu^2)} = \frac{\rho}{2\pi a} \tan^{-1} \left(\frac{\mu}{a} \right) \quad (1.4)$$

where ρ is the resistivity of the semiconductor. Sufficiently far away from the contact where μ is large, the spreading resistance is given by

$$R_s = \frac{\rho}{4a} \quad (1.5)$$

As the relation above suggests, spreading resistance increases with decreasing contact radius. Hence, the contribution of the spreading resistance can become significant in the small contacts formed by scanning probe microscopy based electrical measurements like conductive-atomic force microscopy (C-AFM). Spreading resistance profiling (SRP), a modified C-AFM technique, has become a widely used resistivity and carrier concentration profiling technique [66, 67].

In an STM, an atomically sharp metallic tip is used to analyse a conducting sample. The tunneling contact radius in a typical STM measurement is on the order of 0.5 – 1.5 nm. In normal operation, the tunneling resistance, which is about 10 – 100 G Ω , dominates as the sample resistance and spreading resistance are negligible in comparison. The dominance of tunneling resistance ensures the voltage drop to occur at the tunneling point, hence enabling an accurate determination of the energy states of the sample surface. However, for samples with high resistivity, spreading resistance can become significant in STM measurements [68] and shifts in spectral features can be observed. However, if these shifts can be modelled, STM and STS may be used to determine the carrier concentration of the sample, similar to SRP [56].

In chapter 4, the capability of STM and STS to study nanoscale Si(100) device layers in SOI is explored. Especially, how spreading resistance manifests in STM following the processing of SOI device layers with various doping levels, are discussed. It's shown that ultra-thin SOI with sufficiently high doping levels can be studied with STM. This chapter also discusses the effects of annealing on dopant concentration profiles and electrical properties of the film.

1.6 Dewetting

At high temperatures, the thin device layer of SOI can become mechanically unstable and the thin film can break up into 3D crystals [3, 23, 69-71]. This process is driven by surface energy minimization and occurs well below the melting temperature of the film [3]. The Si film in SOI has a higher surface energy than the oxide underneath. Therefore, at elevated temperatures, once the native oxide has been removed, the system tries to minimize the surface energy by exposing the lower surface energy BOX and forming silicon 3D crystals with a reduced surface area. The driving force for dewetting and the rate of dewetting, both increase with decreasing film thickness. As a consequence, thinner films tend to dewet at lower temperature.

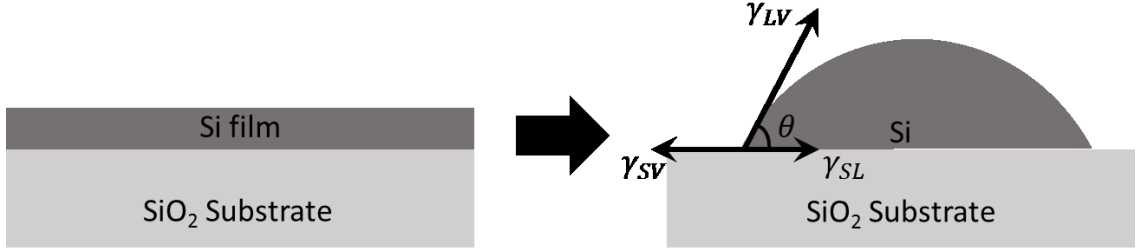


Fig. 1.4: Schematic illustration of the equilibrium shape of a thin film, assuming isotropic surface energies and a rigid substrate, as determined by Young [3].

Since thin films are usually metastable, they often tend to become unstable and evolve into equilibrium morphologies when they are heated to sufficiently high temperatures. The equilibrium morphology is either a flat film or a hemispherical island, depending on the relative magnitude of the surface energy of the film (γ_{LV}), surface energy of the substrate (γ_{SV}), and the interfacial energy of the film and the substrate (γ_{SL}). The expression [72] for the thermodynamic equilibrium between the three phases is given by,

$$\gamma_{SV} = \gamma_{SL} + \gamma_{LV} \cos \theta \quad (1.6)$$

where θ is the equilibrium contact angle at the three-phase boundary. When $\gamma_{SV} \geq \gamma_{SL} + \gamma_{LV}$, θ is 0° , meaning that the film wets the substrate and remains flat and continuous. However, when θ is nonzero, the equilibrium morphology of the film tends to shift from a flat continuous film to a hemispherical island, as shown in Fig. 1.4.

There are two different mechanisms through which a 2D film can agglomerate into crystals. Dewetting can occur through the propagation of nucleated voids or through spontaneously growing thermal fluctuations. In the first mechanism, the dewetting process is initiated by the presence of voids on the crystalline SOI film. However, analysis of the energetics of SOI films have shown that the film is stable against small morphology perturbations [73, 74], and the activation energy required to form even a small void in a very thin SOI film is prohibitively large [3]. Therefore homogeneous spontaneous nucleation of voids does not occur. The nucleation of the void in SOI is believed to occur only at defect sites on the surface or the interfaces of the film [75-77]. Hence, it is heterogeneous in nature and enabled by intrinsic defects in the film. The defects may include dislocations, stacking faults, oxide precipitates, surface particles, protrusions on the BOX or scratches in the film induced during SOI processing [76, 77]. Also, in order for the voids to grow, the size of the void must exceed a critical size ($r_{\text{void}} > r_{\text{crit}}$). Once supercritical voids are formed in the film, they grow in size via different morphological instabilities such as surface diffusion induced edge instability and Rayleigh instability.

For extremely thin films, dewetting occurs through the amplification of surface waves [78]. A competition between the stabilizing effect of interfacial tension and attractive intermolecular forces between the film-substrate and film-vacuum interfaces drives the thickness fluctuations in the film. The amplitude of the perturbations grows with time and eventually leads to dewetting if the growth in the amplitude lowers the total energy of the system. Otherwise, the perturbation decays and the film remains intact. Van der Waals forces become significant in the ultra-thin films which can overcome the interfacial tension, leading to spontaneous amplification of the thickness fluctuations which can eventually dewet the film [78-81] and contact angles that are not well described by the macroscopic Young's equation (1.6).

In chapter 5, the evolution of the morphology of SOI due to annealing in an UHV environment is analysed. Using surface analysis techniques, a major difference in the thermo-mechanical evolution of ultra-thin SOI has been

identified. It is shown in this chapter that the mechanism of thermal instability and dewetting of SOI below 4 nm deviates from thicker SOI.

1.7 Capillary-induced surface diffusion

Sharp edges of structures fabricated on silicon are fundamentally unstable at high temperatures due to their high local surface curvature [3]. The change in curvature creates a free-energy gradient that drives diffusion of atoms away from the curvature towards the flat region [3, 82-84]. This process further leads to capillary edge instability. At high temperatures, the increased diffusion at the edges of SOI thin films and nanostructures fabricated with SOI, can cause the device layer to peel back and uncover the BOX. This effect at the edges enables both oxide desorption and dewetting to occur at lower temperature.

The propagation of mass flow and subsequent dewetting at the void edge is due to surface-energy-driven surface-diffusion-induced morphological instability [3, 85, 86]. This instability is primarily dependent on the temperature and thickness of SOI. Assuming surface energies to be isotropic, the equation for the volumetric surface flux (i.e. volume flux along a surface per unit length perpendicular to the flux) due to surface-energy-driven surface diffusion is given by

$$J_s = - \frac{D_s \gamma \Omega^2 v}{kT} \nabla \kappa(s) \quad (1.7)$$

Where D_s is the surface diffusivity, γ is the surface energy, Ω is the atomic volume, v is the atomic surface density, $\kappa(s)$ is the mean surface curvature along the surface coordinate s , k is the Boltzmann constant, and T is the absolute temperature [3]. The atomic surface diffusion along the surface of the film is determined by the mean surface curvature profile of the film, driving mass flow from regions of higher mean curvature to lower mean curvature [3]. Since, D_s has a strong positive Arrhenius temperature dependence, ($D_s = D_0 \exp(-Q_s/kT)$, where D_0 is the surface diffusion pre-exponential factor and Q_s is the activation energy for surface diffusion) the surface-energy-driven surface diffusion is strongly temperature dependent.

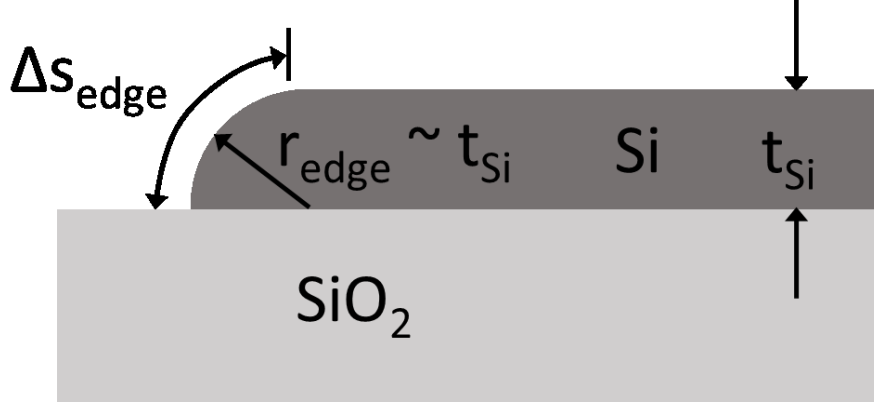


Fig. 1.5: Schematic illustration of the capillary instability. The high edge curvature of a SOI edge drives mass flow away from the edges, making the edges morphologically unstable.

The film thickness dependency of the film edge instability can be understood from the geometrical argument outlined below. Fig. 1.5, shows that for an edge in the SOI device layer, the surface curvature ($\kappa_{edge} \sim r_{edge}^{-1}$) is approximately t_{Si}^{-1} and the surface distance of the curvature Δs_{edge} is approximately equals a quarter arc of a circle given by $\pi t_{Si}/2$. Therefore, the average local curvature gradient can be approximated by

$$\nabla \kappa(edge) \sim \frac{\Delta \kappa(edge)}{\Delta s_{edge}} \sim \frac{1/t_{Si}}{\pi t_{Si}/2} \sim \frac{2}{\pi} \frac{1}{t_{Si}^2} \quad (1.8)$$

From (1.7) and (1.8), local surface diffusion flux at the film edge, J_s , has a inverse square dependence on Si film thickness, consistent with the existence of a capillary edge instability that drives the retraction of SOI edges. It also shows that edge instability increase rapidly with decreasing film thickness and increasing temperature [3].

1.8 Rayleigh Instability

A high-aspect-ratio cylindrical object becomes unstable under the influence of surface tension and lowers its total surface energy by breaking up into a row of spherical particles having uniform size and separation (see Fig. 1.6) [87]. Properties of cylindrical fluids were first analysed by Plateau and then by Rayleigh who demonstrated a relation between the wavelength of a perturbation and the size distribution of the droplets with the radius of the cylinder [88, 89]. This work on fluids was later adopted by Nichols and Mullins to explain the instability of solid

rods [90]. The characteristic wavelength of the Rayleigh instability is proportional to the original radius R_{cyl} of the cylinder and independent of the temperature.

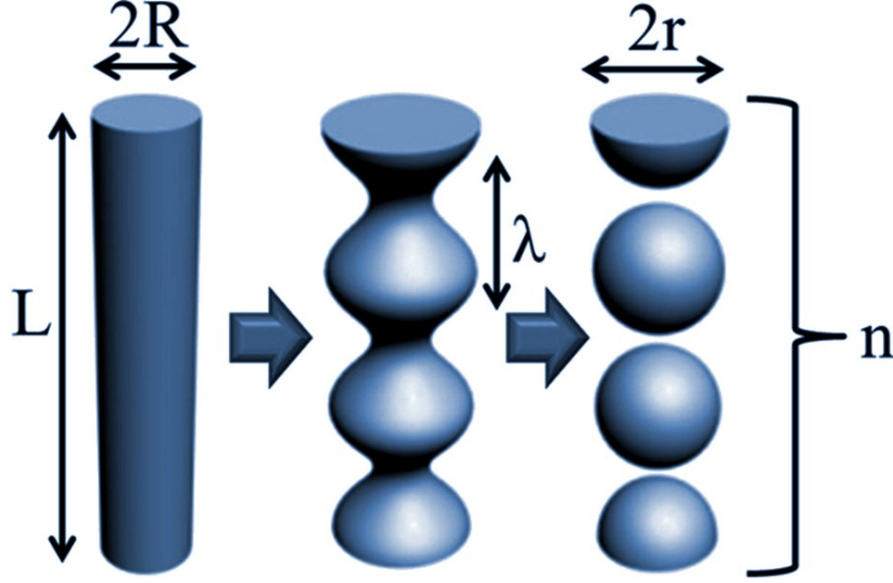


Fig. 1.6: Graphical illustration of the Rayleigh instability. A cylindrical object undulates and transforms into a chain of spheres (image taken from [5]).

A high aspect ratio nanowire fabricated with SOI breaks into crystals whose size increases proportionally to the initial radius of the nanowire. The evolution timescale of the Rayleigh instability decreases with the radius of the wire and also decreases strongly with increasing temperature. Therefore thinner nanowires break at lower temperature.

Due to the capillary edge and Rayleigh instabilities, nanowires fabricated from SOI dewets at a reduced temperature compared to un-patterned SOI, and therefore makes the surface analysis of nanowires challenging. However, it is shown in chapter 6 that the very forces that destabilises and deforms the nanowires could be used to clean the nanowires by controlling the thermal processing conditions. In this chapter, we have shown that surface analysis through STM can be conducted on ultra-small silicon nanowires on insulator structures. Furthermore, as a basis for future work, a simple nanowire and nanodisc fabrication technique has been demonstrated.

1.9 References

1. Teich, M.C. and B. Saleh, *Fundamentals of photonics*. Canada, Wiley Interscience, 1991. **3**.
2. Bhat, N., *Nanoelectronics Era: Novel Device Technologies Enabling Systems on Chips*. Journal of the Indian Institute of Science, 2012. **87**(1): p. 61.
3. Danielson, D.T., et al., *Surface-energy-driven dewetting theory of silicon-on-insulator agglomeration*. Journal of Applied Physics, 2006. **100**(8): p. 083507.
4. Berg, J.A.V.d., et al., *Characterization by medium energy ion scattering of damage and dopant profiles produced by ultrashallow B and As implants into Si at different temperatures*. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2002. **20**(3): p. 974-983.
5. Riss, A., et al., *Local Electronic and Chemical Structure of Oligo-acetylene Derivatives Formed Through Radical Cyclizations at a Surface*. Nano Letters, 2014. **14**(5): p. 2251-2255.
6. Schaller, R.R., *Moore's law: past, present and future*. IEEE spectrum, 1997. **34**(6): p. 52-59.
7. Moore, G.E. *Progress in digital integrated electronics*. in *Electron Devices Meeting*. 1975.
8. Bohr, M. and K. Mistry, *Intel's revolutionary 22 nm transistor technology*. Intel website, 2011.
9. Doyle, B., et al., *Transistor Elements for 30nm Physical Gate Lengths and Beyond*. Intel Technology Journal, 2002. **6**(2).
10. Ko, H., et al., *Ultrathin compound semiconductor on insulator layers for high performance nanoscale transistors*. arXiv preprint arXiv:1108.1127, 2011.
11. Lyons, D.M., et al., *Tailoring the Optical Properties of Silicon Nanowire Arrays through Strain*. Nano Letters, 2002. **2**(8): p. 811-816.
12. Canham, L.T., *Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers*. Applied Physics Letters, 1990. **57**(10): p. 1046-1048.

- 13.Hodes, G., *When Small Is Different: Some Recent Advances in Concepts and Applications of Nanoscale Phenomena*. Advanced Materials, 2007. **19**(5):p.639-655.
- 14.Wilson, W.L., P. Szajowski, and L. Brus, *Quantum confinement in size-selected, surface-oxidized silicon nanocrystals*. SCIENCE-NEW YORK THEN WASHINGTON-, 1993. **262**: p. 1242-1242.
- 15.Wu, Z., J.B. Neaton, and J.C. Grossman, *Quantum Confinement and Electronic Properties of Tapered Silicon Nanowires*. Physical Review Letters, 2008. **100**(24): p. 246804.
- 16.Leão, C.R., A. Fazzio, and A.J.R. da Silva, *Si Nanowires as Sensors: Choosing the Right Surface*. Nano Letters, 2007. **7**(5): p. 1172-1177.
- 17.Jang, H., et al., *Quantum Confinement Effects in Transferrable Silicon Nanomembranes and Their Applications on Unusual Substrates*. Nano Letters, 2013. **13**(11): p. 5600-5607.
- 18.Nolan, M., et al., *Silicon nanowire band gap modification*. Nano letters, 2007. **7**(1): p. 34-38.
- 19.Hirschman, K., et al., *Silicon-based visible light-emitting devices integrated into microelectronic circuits*. Nature, 1996. **384**(6607): p. 338.
- 20.Pavesi, L., et al., *Optical gain in silicon nanocrystals*. Nature, 2000. **408**(6811): p. 440.
- 21.Zhang, P., et al., *Electronic transport in nanometre-scale silicon-on-insulator membranes*. Nature, 2006. **439**(7077): p. 703.
- 22.Lu, Z., et al., *Quantum confinement and light emission in SiO₂/Si superlattices*. Nature, 1995. **378**(6554): p. 258.
- 23.Legrand, B., et al., *Formation of silicon islands on a silicon on insulator substrate upon thermal annealing*. Applied Physics Letters, 2000. **76**(22): p. 3271.
- 24.Liu, F., *Self-Assembly of Three-Dimensional Metal Islands: Nonstrained versus Strained Islands*. Physical Review Letters, 2002. **89**(24): p. 246105.
- 25.Lopeandía, A.F. and J. Rodríguez-Viejo, *Size-dependent melting and supercooling of Ge nanoparticles embedded in a SiO₂ thin film*. Thermochemica Acta, 2007. **461**(1): p. 82-87.

26. Sun, J. and S.L. Simon, *The melting behavior of aluminum nanoparticles*. Thermochemica Acta, 2007. **463**(1): p. 32-40.
27. Guisbiers, G., et al., *Mechanical and thermal properties of metallic and semiconductive nanostructures*. The Journal of Physical Chemistry C, 2008. **112**(11): p. 4097-4103.
28. Yakunin, A.M., et al., *Warping a single Mn acceptor wavefunction by straining the GaAs host*. Nature Materials, 2007. **6**: p. 512.
29. Wijnheijmer, A.P., et al., *Enhanced Donor Binding Energy Close to a Semiconductor Surface*. Physical Review Letters, 2009. **102**(16): p. 166101.
30. Georgiev, V.P., et al., *Experimental and Simulation Study of Silicon Nanowire Transistors Using Heavily Doped Channels*. IEEE Transactions on Nanotechnology, 2017. **16**(5): p. 727-735.
31. Teo, B.K. and X.H. Sun, *Silicon-Based Low-Dimensional Nanomaterials and Nanodevices*. Chemical Reviews, 2007. **107**(5): p. 1454-1532.
32. Sutter, P., W. Ernst, and E. Sutter, *Scanning tunneling microscopy on ultrathin silicon on insulator (100)*. Applied Physics Letters, 2004. **85**(15): p. 3148.
33. Celler, G. and S. Cristoloveanu, *Frontiers of silicon-on-insulator*. Journal of Applied Physics, 2003. **93**(9): p. 4955-4978.
34. Yan, R.-H., A. Ourmazd, and K.F. Lee, *Scaling the Si MOSFET: From bulk to SOI to bulk*. IEEE Transactions on Electron Devices, 1992. **39**(7): p. 1704-1710.
35. Flandre, D., et al., *Fully-depleted SOI CMOS technology for low-voltage low-power mixed digital/analog/microwave circuits*. Analog Integrated Circuits and Signal Processing, 1999. **21**(3): p. 213-228.
36. Zhao, L., et al., *Characterization on the passivation stability of HF aqueous solution treated silicon surfaces for HIT solar cell application by the effective minority carrier lifetime measurement*. Chinese Journal of Physics, 2010. **48**(3): p. 392-399.
37. Bender, H., S. Verhaverbeke, and M. Heyns, *Hydrogen Passivation of HF-Last Cleaned (100) Silicon Surfaces Investigated by Multiple Internal Reflection Infrared Spectroscopy*. Journal of the Electrochemical Society, 1994. **141**(11): p. 3128-3136.

38. Mayne, A.J., et al., *An STM study of the chemisorption of C₂H₄ on Si(001)(2 × 1)*. Surface Science, 1993. **284**(3): p. 247-256.
39. Bozack, M.J., et al., *Chemical activity of the C C double bond on silicon surfaces*. Surface Science, 1986. **177**(1): p. L933-L937.
40. Pan, W., T. Zhu, and W. Yang, *First-principles study of the structural and electronic properties of ethylene adsorption on Si(100)-(2×1) surface*. The Journal of Chemical Physics, 1997. **107**(10): p. 3981-3985.
41. Fisher, A.J., P.E. Blöchl, and G.A.D. Briggs, *Hydrocarbon adsorption on Si(001): when does the Si dimer bond break?* Surface Science, 1997. **374**(1): p. 298-305.
42. Yoshinobu, J., et al., *The adsorbed states of ethylene on Si(100)c(4×2), Si(100)(2×1), and vicinal Si(100) 9°: Electron energy loss spectroscopy and low-energy electron diffraction studies*. The Journal of Chemical Physics, 1987. **87**(12): p. 7332-7340.
43. Barimar, P.S.N., et al., *Study of the effect of thermal treatment on morphology and chemical composition of silicon-on-insulator*. Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena, 2016. **34**(4): p. 041806.
44. Xue, K., J.B. Xu, and H.P. Ho, *Nanoscale in situ investigation of ultrathin silicon oxide thermal decomposition by high temperature scanning tunneling microscopy*. Nanotechnology, 2007. **18**(48): p. 485709.
45. Hibino, H., M. Uematsu, and Y. Watanabe, *Void growth during thermal decomposition of silicon oxide layers studied by low-energy electron microscopy*. Journal of Applied Physics, 2006. **100**(11): p. 113519.
46. Johansson, U., H. Zhang, and R. Nyholm, *Thermal desorption of oxides on Si(100): a case study for the scanning photoelectron microscope at MAX-LAB*. Journal of Electron Spectroscopy and Related Phenomena, 1997. **84**(1): p. 45-52.
47. Sun, Y.K., D.J. Bonser, and T. Engel, *Spatial inhomogeneity and void-growth kinetics in the decomposition of ultrathin oxide overlayers on Si(100)*. Physical Review B, 1991. **43**(17): p. 14309-14312.

48. Sun, Y.K., D.J. Bonser, and T. Engel, *Thermal decomposition of ultrathin oxide layers on Si(100)*. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 1992. **10**(4): p. 2314-2321.
49. Ogawa, S., et al., *Consumption kinetics of Si atoms during growth and decomposition of very thin oxide on Si(001) surfaces*. Thin Solid Films, 2006. **508**(1): p. 169-174.
50. Tromp, R., et al., *High-Temperature SiO₂ Decomposition at the SiO₂/Si Interface*. Physical Review Letters, 1985. **55**(21): p. 2332-2335.
51. Johnson, K.E. and T. Engel, *Direct measurement of reaction kinetics for the decomposition of ultrathin oxide on Si(001) using scanning tunneling microscopy*. Physical Review Letters, 1992. **69**(2): p. 339-342.
52. Jones, D. and V. Palermo, *Production of nanostructures of silicon on silicon by atomic self-organization observed by scanning tunneling microscopy*. Applied Physics Letters, 2002. **80**(4): p. 673-675.
53. Kinefuchi, I., et al., *Inhomogeneous decomposition of ultrathin oxide films on Si(100): Application of Avrami kinetics to thermal desorption spectra*. The Journal of Chemical Physics, 2008. **128**(16): p. 164712.
54. Liehr, M., J.E. Lewis, and G.W. Rubloff, *Kinetics of high-temperature thermal decomposition of SiO₂ on Si(100)*. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 1987. **5**(4): p. 1559-1562.
55. Ota, Y., *n-Type Doping Techniques in Silicon Molecular Beam Epitaxy by Simultaneous Arsenic Ion Implantation and by Antimony Evaporation*. J. Electrochem. Soc, 1979. **126**(10).
56. Barimar, P.S.N., et al., *Spreading resistance at the nano-scale studied by scanning tunneling and field emission spectroscopy*. Applied Physics Letters, 2017. **110**(26): p. 263111.
57. Lin, K.C., et al., *Surface characterization of silicon on insulator material*. Applied Physics Letters, 1998. **72**(18): p. 2313-2315.
58. Christensen, J., et al., *Phosphorus and boron diffusion in silicon under equilibrium conditions*. Applied physics letters, 2003. **82**(14): p. 2254-2256.

- 59.Zhang, K., et al., *Fast flexible electronics using transferrable silicon nanomembranes*. Journal of Physics D: Applied Physics, 2012. **45**(14): p. 143001.
- 60.Ndoye, C., T. Liu, and M. Orlowski, *Comparison of Diffusion Mechanisms in Si Bulk, Nanomembranes, and Nanowires*. ECS Transactions, 2011. **33**(31): p. 3-18.
- 61.Shibahara, K., et al., *Dopant loss origins of low energy implanted arsenic and antimony for ultra shallow junction formation*. MRS Online Proceedings Library Archive, 1998. **532**.
- 62.Meishoku, K., et al., *Quantitative Evaluation of Dopant Loss in 5–10 keV As Ion Implantation for Low-Resistive, Ultrashallow Source/Drain Formation*. Japanese Journal of Applied Physics, 1999. **38**(4S): p. 2324.
- 63.Pei, L., *Dopant Segregation at Silicon-Oxide Interfaces*. 2007.
- 64.LEVIN, M. and M. MILLER, *Maxwell a treatise on electricity and magnetism*. Uspekhi Fizicheskikh Nauk, 1981. **135**(3): p. 425-440.
- 65.Slade, P.G., *Electrical contacts - principles and applications*. second ed.
- 66.Mazur, R. and D. Dickey, *A spreading resistance technique for resistivity measurements on silicon*. Journal of the electrochemical society, 1966. **113**(3): p. 255-259.
- 67.Ehrstein, J.R., *Spreading resistance measurements—An overview*, in *Emerging Semiconductor Technology*. 1987, ASTM International.
- 68.Johnson, M.B. and J.M. Halbout, *Scanning tunneling microscopy and spectroscopy for studying cross-sectioned Si(100)*. Journal of Vacuum Science & Technology B, 1992. **10**(1): p. 508-514.
- 69.Tabe, M., et al., *Formation of high-density silicon dots on a silicon-on-insulator substrate*. Applied Surface Science, 1999. **142**(1–4): p. 553-557.
- 70.Bussmann, E., et al., *Thermal instability of silicon-on-insulator thin films measured by low-energy electron microscopy*. IOP Conference Series: Materials Science and Engineering, 2010. **12**: p. 012016.
- 71.Bussmann, E., et al., *Dynamics of solid thin-film dewetting in the silicon-on-insulator system*. New Journal of Physics, 2011. **13**(4): p. 043017.

- 72.Young, T., *An essay on the cohesion of fluids*. Philosophical Transactions of the Royal Society of London, 1805. **95**: p. 65-87.
- 73.Aouassa, M., et al., *The kinetics of dewetting ultra-thin Si layers from silicon dioxide*. New Journal of Physics, 2012. **14**(6): p. 063038.
- 74.Srolovitz, D.J. and S.A. Safran, *Capillary instabilities in thin films. I. Energetics*. Journal of Applied Physics, 1986. **60**(1): p. 247-254.
- 75.Yukinori, O., et al., *Thermal Agglomeration of Thin Single Crystal Si on SiO₂ in Vacuum*. Japanese Journal of Applied Physics, 1995. **34**(4R): p. 1728.
- 76.D. K. Sadana, J.L., H. J. Hovel, K. Petrillo, and P. Roitman, Proceedings of the 1994 IEEE International SOI Conference (IEEE, Piscataway, NJ, 1994): p. 111.
- 77.Giles, L.F., A. Nejim, and P.L.F. Hemment, *New etchant for crystallographic defect studies in thin SOI materials (<1000 AA)*. Electronics Letters, 1993. **29**(9): p. 788-789.
- 78.Singh, S.P., *Spinodal theory: A common rupturing mechanism in spinodal dewetting and surface directed phase separation (some technological aspects: Spatial correlations and the significance of dipole-quadrupole interaction in spinodal dewetting)*. Advances in Condensed Matter Physics, 2011. **2011**.
- 79.Bischof, J., et al., *Dewetting Modes of Thin Metallic Films: Nucleation of Holes and Spinodal Dewetting*. Physical Review Letters, 1996. **77**(8): p. 1536-1539.
- 80.Trice, J., et al., *Novel self-organization mechanism in ultrathin liquid films: theory and experiment*. Physical review letters, 2008. **101**(1): p. 017802.
- 81.Brada, M. and D. Clarke, *A thermodynamic approach to the wetting and dewetting of grain boundaries*. Acta materialia, 1997. **45**(6): p. 2501-2508.
- 82.Mullins, W.W., *Flattening of a Nearly Plane Solid Surface due to Capillarity*. Journal of Applied Physics, 1959. **30**(1): p. 77-83.
- 83.Celano, T.A., et al., *Capillarity-Driven Welding of Semiconductor Nanowires for Crystalline and Electrically Ohmic Junctions*. Nano letters, 2016.**16**(8):p.5241-5246.
- 84.Nichols, F. and W. Mullins, *Morphological changes of a surface of revolution due to capillarity-induced surface diffusion*. Journal of Applied Physics, 1965. **36**(6): p. 1826-1835.

- 85.Jiran, E. and C.V. Thompson, *Capillary instabilities in thin films*. Journal of Electronic Materials, 1990. **19**(11): p. 1153-1160.
- 86.Jiran, E. and C.V. Thompson, *Capillary instabilities in thin, continuous films*. Thin Solid Films, 1992. **208**(1): p. 23-28.
- 87.Peng, H.Y., et al., *Bulk-quantity Si nanosphere chains prepared from semi-infinite length Si nanowires*. Journal of Applied Physics, 2001. **89**(1): p. 727-731.
- 88.Rauber, M., et al., *Thermal stability of electrodeposited platinum nanowires and morphological transformations at elevated temperatures*. Nanotechnology, 2012. **23**(47): p. 475710.
- 89.Rayleigh, L., *On The Instability Of Jets*. Proceedings of the London Mathematical Society, 1878. **s1-10**(1): p. 4-13.
- 90.Molares, M.E.T., et al., *Fragmentation of nanowires driven by Rayleigh instability*. Applied Physics Letters, 2004. **85**(22): p. 5337-5339.

2

EQUIPMENT & METHODS

The principles behind many of the experimental techniques used throughout this thesis are introduced in this chapter including scanning tunneling microscopy, X-ray photoelectron spectroscopy, atomic force microscopy, electron microscopy and lithography techniques.

2.1 Ultra-high vacuum

Vacuum is generally categorized as low, high and ultra-high vacuum based on the pressure range. Ultra-high vacuum (UHV) is a regime of vacuum which is characterized by a pressure that is lower than 10^{-9} mbar. Most surface science studies are carried out in an UHV environment. UHV conditions allow atomically clean surfaces to be obtained and maintained in a contamination free environment during the course of the experiment. Also, some techniques like low energy electron diffraction and X-ray photoelectron spectroscopy need UHV so that electrons can reach the screen or analyser without colliding with particles and being deflected. At atmospheric pressure a gas molecule has a mean free path of ~ 60 nm, which means that the gas molecule travels only around 60 nm between two collisions, while at UHV, the molecules have a mean free path of several kilometres [13]. This means that in low pressure only a few molecules will contaminate the sample surface. Therefore for surface science experiments that require atomically clean surfaces, UHV conditions are essential.

UHV chambers are typically made with certain variants of stainless steel, which apart from having superior mechanical and chemical characteristics, also exhibit properties such as low gas permeability and magnetic permeability close to 1 [14]. Materials used within UHV systems must have low vapour pressure even at

elevated temperature up to 200 °C, hence refractive metals such as Molybdenum and Tantalum are used in cases of high temperature applications. In order to attain UHV, the whole system is “baked”, i.e. heated up to temperatures above 100 °C to facilitate desorption of water and contaminants from the inner walls of the chamber. While baking, all parts within the chamber are also heated to temperatures slightly higher than their working temperature to allow desorption of adsorbed gasses which would otherwise outgas during experimental work.

Several different UHV systems have been used for the experiments described in this thesis. While the scanning tunneling microscopy (STM) and X-ray photoelectron spectroscopy (XPS) measurements were carried out with a CreaTec LT-STM/AFM system and a VG Scienta ESCALab MKII system respectively, the thermal process optimization was carried out in a home-made UHV system. Details about the CreaTech LT-STM/AFM and the home-made UHV system will be described in the following section and the VG Scienta ESCALab MKII XPS system will be presented in the XPS section.

2.2 Scanning tunneling microscopy (STM)

STM is a type of scanning probe microscopy that uses electron tunneling to measure the properties of conducting surfaces with atomic resolution. STM was developed at IBM Zurich in the 1980s by Binnig and Rohrer [3, 15, 16] and since then has developed into an important tool in surface science. STM operates on the principle of quantum mechanical tunneling: when a metallic tip is brought to within several angstroms from a surface and a bias is applied, there is a finite probability that electrons will tunnel between the tip and the surface. The direction of the tunneling depends on the applied bias. STM probes the local electronic density of states of the surface, allowing investigation of surface reconstruction and surface defects at the atomic scale. To a first approximation, STM provides information on the topography of the surface [17].

2.2.1 Elastic tunneling through a one-dimensional rectangular potential barrier

In classical mechanics, an electron with energy E can overcome a one-dimensional rectangular potential barrier V_0 only if $E > V_0$. However, in quantum

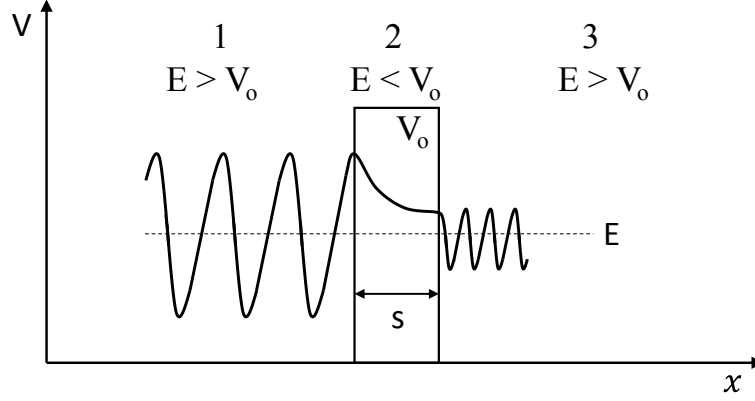


Fig. 2.1: Wave function $\psi(x)$ for an electron with energy E interacting with a one dimensional potential barrier with height V_0 and width s . Within the classically forbidden Region 2 ($E < V_0$), the wave function decays exponentially and is present in Region 3 ($E > V_0$).

mechanics, an electron is described with a wave function $\psi(x)$ which satisfies the Schrödinger equation:

$$-\frac{\hbar^2}{2m} \frac{d^2}{dx^2} \psi(x) + [V(x) - E] \psi = 0 \quad (2.1)$$

Fig. 2.1 shows the wave function of an electron with energy E interacting with a one-dimensional potential barrier of height V_0 and width s . In Region 1 where $E > V_0$ Equation (1) has the solution

$$\psi(x) = \psi(0)e^{\pm ikx} \quad (2.2)$$

where

$$k = \frac{\sqrt{(2m(E - V_0))}}{\hbar} \quad (2.3)$$

Where m is the mass of the electron, $\hbar$ is Planck's constant divided by 2π and k represents a travelling wave [5]. In Region 2 where $E < V_0$, the solution is of the form

$$\psi(x) = \psi(0)e^{\pm \alpha x} \quad (2.4)$$

where

$$\alpha = \frac{\sqrt{(2m(V_0 - E))}}{\hbar} \quad (2.5)$$

α is known as the decay constant [5]. In Region 3 ($E > V_0$) the solution is

$$\psi(x) = \psi(0)e^{-\alpha x} \quad (2.6)$$

Hence the electron wave function decays exponentially within the barrier and for a sufficiently narrow barrier, there is a finite probability that the particle will tunnel through the barrier. The probability density P of the wavefunction tunneling through the barrier is proportional to the square of the wave function [18] (2.6),

$$P \propto |\psi(0)|^2 e^{-2\alpha x} \quad (2.6 \text{ (a)})$$

2.2.2 Elastic tunneling through a one-dimensional potential barrier of arbitrary shape

An extension to the potential barrier of arbitrary shape can be obtained from the description outlined in the section above using the Wentzel-Kramers-Brillouin (WKB) approximation [17]. The WKB approximation is based on treating Planck's constant ($6.626 \times 10^{-34} \text{ m}^2 \text{ Kg s}^{-1}$) as a small number. The expression of the probability $D(E)$ of an electron tunneling through a barrier of arbitrary shape is given by

Where $V(x)$ is the barrier height at any position x , s_1 and s_2 (refer to Fig. 2.2) are the classical turning points of the barrier and $\Delta s = (s_2 - s_1)$ is the width of the barrier. The WKB approximation is appropriate only if $E \ll V$ and the slope of either side (s_2 and s_1) of the barrier is gentle.

2.2.3 Elastic tunneling in planar metal-insulator-metal (MIM) tunnel junctions

$$\begin{aligned} D(E) &= \exp\left(\frac{-2}{\hbar} \int_{s_1}^{s_2} \sqrt{2m [V(x) - E]} dx\right) \\ &= \exp\left(-2 \int_{s_1}^{s_2} \alpha(x, E) dx\right) \end{aligned} \quad (2.7)$$

The illustration of elastic tunneling in a one-dimensional potential barrier can be applied to MIM tunnel junctions as shown in Fig. 2.2. Here we consider similar metal electrodes at thermal equilibrium, exhibiting free electron behavior. The insulator is treated as though it were a vacuum. From Eq. (2.7), for an electron with energy component E_x with

$$E_x = \frac{(mv_x^2)}{2} \quad (2.8)$$

where v_x is the electron velocity component in x and m is the electron mass, the probability $D(E_x)$ of the electron tunneling from one electrode to another through an arbitrary shaped barrier is given by

$$D(E_x) = \exp\left(\frac{-2\sqrt{2m}}{\hbar} \int_{s_1}^{s_2} \sqrt{[\eta + \phi(x) - E_x]} dx\right) \quad (2.9)$$

where S_1 and S_2 are the distances from the surface of Electrode 1 to the point where the potential energy equals the Fermi energy near electrode surfaces 1 and 2 as shown in Fig. 2.2, η is the Fermi level of the electrode 1 and $\phi(x)$ is the potential energy of an electron at any position x between the two surfaces. By introducing a term $\overline{\phi}$ [9], defined as mean potential barrier height ϕ above the Fermi level η where

$$\overline{\phi} = \frac{1}{\Delta s} \int_{s_1}^{s_2} \phi(x) dx$$

the tunneling current density J at 0 K can be expressed as:

$$J = J_0 \overline{\phi} \exp(-A\Delta s \sqrt{\overline{\phi}}) - J_0 (\overline{\phi} + eV) \exp(-A\Delta s \sqrt{\overline{\phi} + eV}) \quad (2.10)$$

where

J_1

J_2

$$J_0 = \frac{e}{4\pi^2 \hbar (\beta \Delta s)^2}, \quad A = \frac{2\beta \sqrt{2m}}{\hbar}, \quad \beta \approx 1$$

Here, eV is the potential between the two electrodes. Eq. (2.10) can be interpreted as a current density J_1 flowing from Electrode 1 to Electrode 2 and a current density

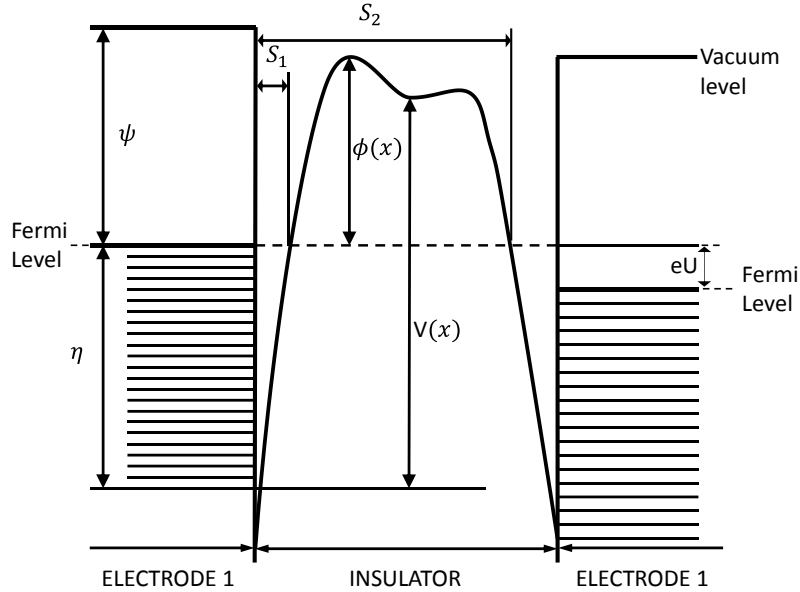


Fig. 2.2: Arbitrary shaped potential barrier between two metal electrodes. (Figure taken from [9]).

J_2 flowing from Electrode 2 to Electrode 1, with the difference between them equal to the net density J . The current density is zero with no voltage applied. With an applied voltage, the barrier is perturbed and this leads to a current flow which is proportional to the applied bias. The applied bias opens up an energy window of allowed states with width equal to eV for tunneling [9].

2.2.4 Quantum mechanical tunneling as applied to STM

An STM basically constitutes a metal-insulator-metal or a metal-insulator-conductor system where a metallic tip is separated a small distance s from the conducting sample. The quantum tunneling model for a one dimensional tunnel barrier demonstrated above can be applied to STM and used to calculate the exponential dependence of the tunnel current on tip-sample separation. The tunneling current I typically increases by an order of magnitude for a $1 \text{ \AA}$ decrease in the tip-sample separation [17-20]. This sensitivity of the tunneling current to tip-sample separation allows the STM to attain atomic resolution.

While the analysis of a one-dimensional tunnel barrier describes the exponential dependency of the tunnel current on the tip-sample separation, the scanning tunneling microscope is not one-dimensional. In addition to moving the scanner in the x - y plane with respect to the surface, it is also possible to generate images and spectra through varying the scanner position with respect to the surface in z . A more detailed theoretical treatment of the tunneling current in STM was developed by Bardeen in 1961 [21]. The theory is based on the tunneling process in a metal/insulator system. It is assumed that the metal electrodes are a weakly interacting system in which the tunneling process is facilitated by the overlapping of the wave functions within the insulator, as shown in Fig. 2.3. An expression of the tunneling current was obtained using the time dependent perturbation theory and Fermi's golden rule [22]. Tersoff and Hamann [11, 23] later extended the approach to provide a quantitative theory for vacuum tunneling between a real solid and a model probe with a spherical tip, as present in the STM. For the case of low temperature ($T \approx 0 \text{ K}$) and small voltage, they obtained an expression for tunneling current as:

$$I = \frac{2\pi}{\hbar} e^2 V \sum_{\mu, \nu} |M_{\mu, \nu}|^2 \delta(E_{\mu} - E_F) \delta(E_{\nu} - E_F) \quad (2.11)$$

where E_{μ} and E_F are the energies for the states ψ_{μ} of the sample and χ_{ν} of the tip, relative to the Fermi level of the respective electrodes. $M_{\mu, \nu}$ is the tunneling matrix element between the two states. The expression (2.11) can be interpreted in a simple fashion by considering the ideal case where the tip is assumed to be a single point charge at $\vec{r}_{tip}$ with a radius R . In this case the angle dependence of the charge distribution can be neglected. The tunneling matrix element $M_{\mu, \nu}$ is then simply proportional to the amplitude of the sample wave function ψ_{μ} at $\vec{r}_{tip}$. In this limit, Eq. (2.11) can be expressed as

$$I(\vec{r}_{tip}, V) \propto \sum_{\mu} |\psi_{\mu}(\vec{r}_{tip})|^2 \delta(E_{\mu} - E_F) \equiv \rho(\vec{r}_{tip}, E_F) \quad (2.12)$$

The quantity, $\rho(\vec{r}_{tip}, E_F)$, is the surface local density of states (LDOS) of the sample surface at E_F at the position of the tip $\vec{r}_{tip}$. Thus Eq. (2.12) demonstrates that the STM image is a contour map of constant surface LDOS.

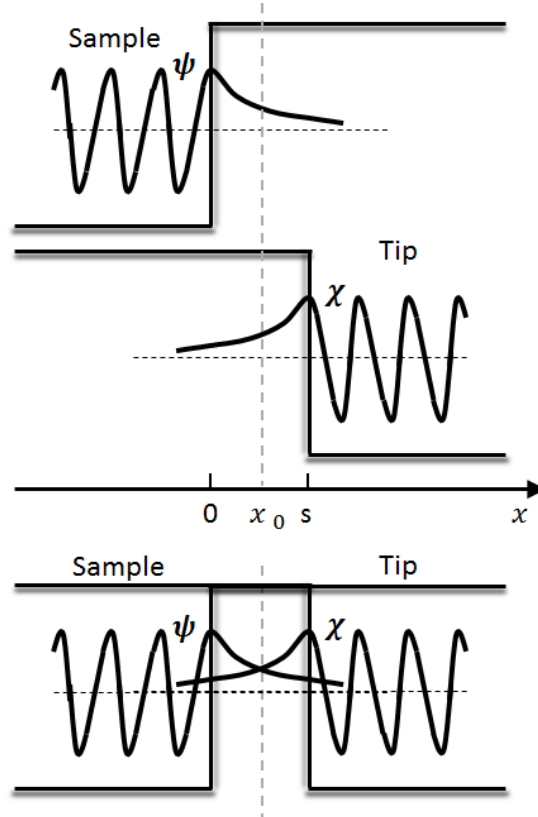


Fig. 2.3: Illustration of the Bardeen approach to tunneling theory [5].

2.2.5 STM – Experimental details

Fig. 2.4 shows a schematic diagram of the basic operation of an STM. An atomically sharp metallic tip is scanned over a conducting sample surface with a separation distance of a few ångströms while a potential difference is applied between the tip and the sample. The tip is positioned and scanned over the sample using a piezoelectric actuator which has a typical lateral (x-y) resolution of 0.1 Å and a vertical (z) resolution better than 0.01 Å . In order to achieve sub-ångström precision in an STM, several methods are used to eliminate or reduce mechanical vibration. A number of vibration isolation techniques are used in order to damp

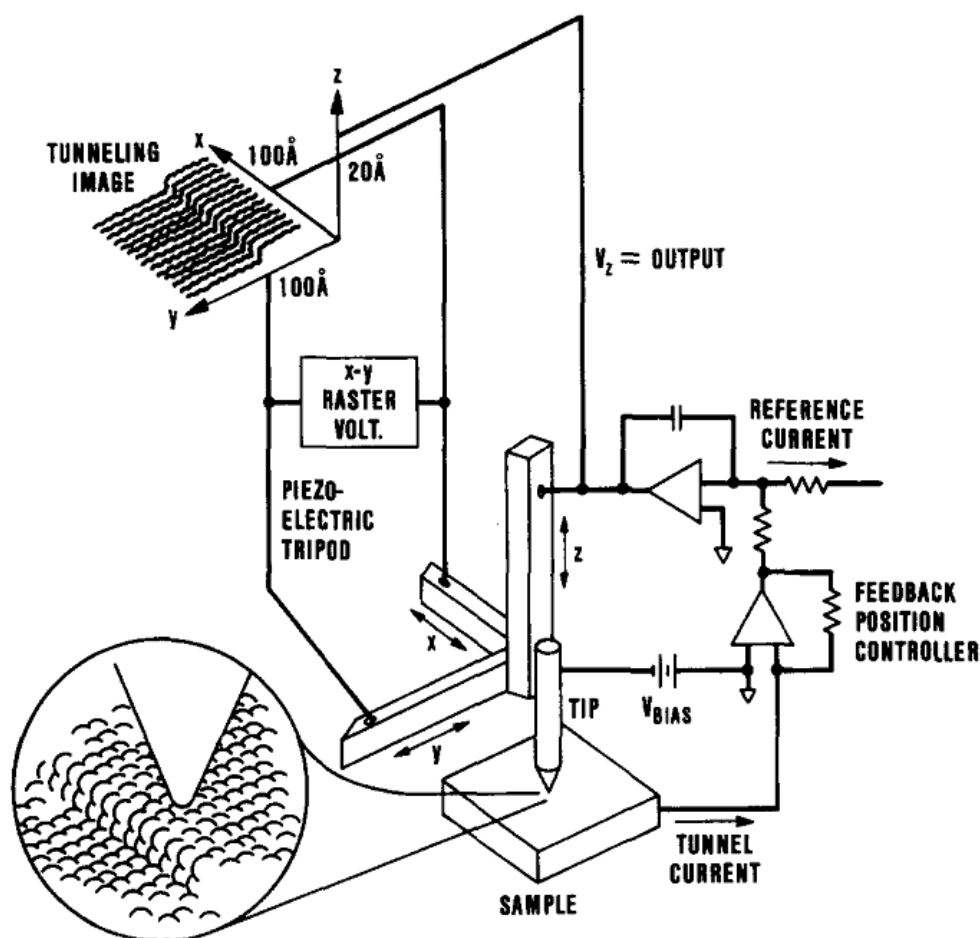


Fig. 2.4: Schematic diagram of a typical scanning tunneling microscope (STM). An atomically sharp metallic tip is mounted on a piezoelectric tripod scanner which is capable of moving the tip in the x-y (parallel to the sample surface) and z (perpendicular to the sample surface) directions with atomic resolution. Movement of the tip in the x-y plane is driven by the x-y raster scan generator and the z movement is driven by the feedback position controller. In constant current mode, a map of the surface is obtained by plotting the feedback voltage as a function of x-y tip position on surface [2, 3] (image taken from [2]).

both low and high frequency vibrations. These includes vibration isolation legs, suspending the STM with metal springs, eddy-current dampers and also use of cryogenic temperatures for STM operations.

There are two principle modes of STM operation: constant height (CH) mode and constant current (CC) mode. In CH mode the height of the tip above the surface is held constant and in CC mode the tunneling current is held constant. CH mode allows faster scans but the tip is susceptible to crashing into the surface if the surface roughness is high. Therefore CH mode is best suited for atomically flat surfaces.

In STM, electrons tunnel from tip to sample or vice versa, depending on the polarity of the voltage applied between them. Fig. 2.5 shows different energy level configuration of the tip and the sample. Fig. 2.5(a) shows the sample and the tip separated by a small vacuum gap in equilibrium. Based on the polarity of the applied bias, two current modes can be categorized. Filled state imaging, where the filled state of the sample is probed while a negative bias is applied to the sample with respect to the tip, electron from the filled state of the sample (below E_F) tunnel into the empty states of the tip (above E_F) as shown in Fig. 2.5 (b). For empty state imaging, a positive bias is applied to the sample. The Fermi level of the sample shifts below the Fermi level of the tip and thus the electrons tunnel from the filled state of the tip to empty states of the sample (Fig. 2.5 (c)).

2.2.6 Tunneling spectroscopy

In addition to topographic information, STM can also be used to perform local dynamic conductance dI/dV measurements to provide a rich body of information on the electronic states and energies of the surface [24]. This method is known as scanning tunneling spectroscopy (STS). The conductance spectra are obtained by measuring the tunnel current while the tip is placed at a fixed height over a specific site on the surface and the bias voltage is swept over a specified range. Assuming a free electron metal tip, Eq. (2.5) implies that

$$\frac{dI}{dV} \propto \rho_s(E_F - eV) \quad (2.13)$$

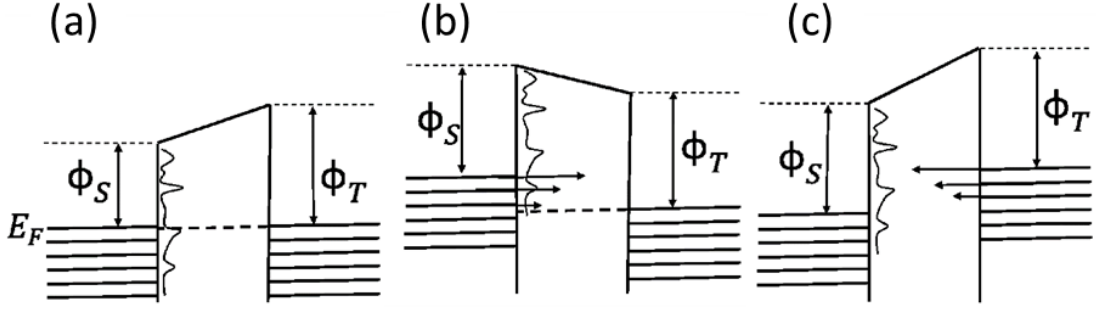


Fig. 2.5: Energy level diagrams for sample and tip. In STM, electrons will tunnel from tip to sample or vice versa, depending on the polarity of the voltage between tip and sample. (a) Sample and tip at equilibrium, separated by small vacuum gap. (b) Negative sample bias: electrons tunnel from the sample into the tip, (c) Positive sample bias: electrons tunnel from the tip to sample.

which shows that the conductance spectra is proportional to the density of states (DOS) of the sample (ρ_s). Tunnel current measured at varying voltage can be differentiated post measurement to extract conductance data as shown in Fig. 2.6(a). In order to improve energy resolution, a lock-in amplifier can be used to

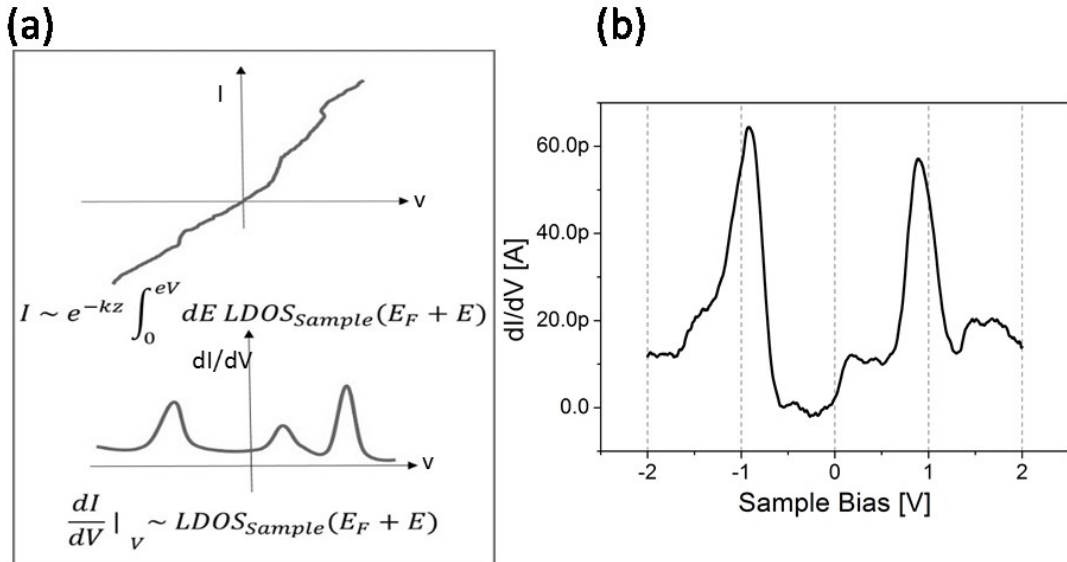


Fig. 2.6: Example of scanning tunneling spectroscopy data. In STS, tunnel current is measured as a function of the bias voltage. The plot describes the conducting property of the sample. The first derivative, $\frac{dI}{dV}$, is directly proportional to the local density of states (LDOS) of the sample. (For all practical purposes we assume that LDOS of the tip is constant) [11]. (a) shows the relation between tunneling current and conductance spectra. (b) shows a STS of a clean bulk Si(100) surface.

modulate V and measure dI/dV directly. Fig. 2.6 (b) shows a typical tunneling conductance spectra obtained from a clean bulk Si(100) [25-33].

2.2.7 Field emission spectroscopy (FES)

The energy region above the vacuum level can be accessed in STM through field emission spectroscopy. This spectroscopy is carried out with the applied bias voltage exceeding the averaged work function. At these biases, electron standing waves are formed which manifest as oscillations in the field emission current as bias or gap distance are varied [34]. The oscillations are due to the reflection of the electrons in the region between the trapezoidal barrier and the surface of the sample, as shown in Fig. 2.7(a). The condition for the standing wave formation depends mainly on three factors: a) electronic potential in the gap, b) the energy of the field-emitted electrons, and c) the electron reflectance at the surface [5]. As electron reflectance varies with surface, field emission spectroscopy allows characterization of the tunneling barrier of various samples and surfaces. Fig. 2.7(b) shows an example of FES recorded on a Si (100) surface. The dotted and the solid lines indicate $z(V)$ and dz/dV spectra respectively. The first peak in the dz/dV spectra gives the approximate value of the work function of the surface [34, 35].

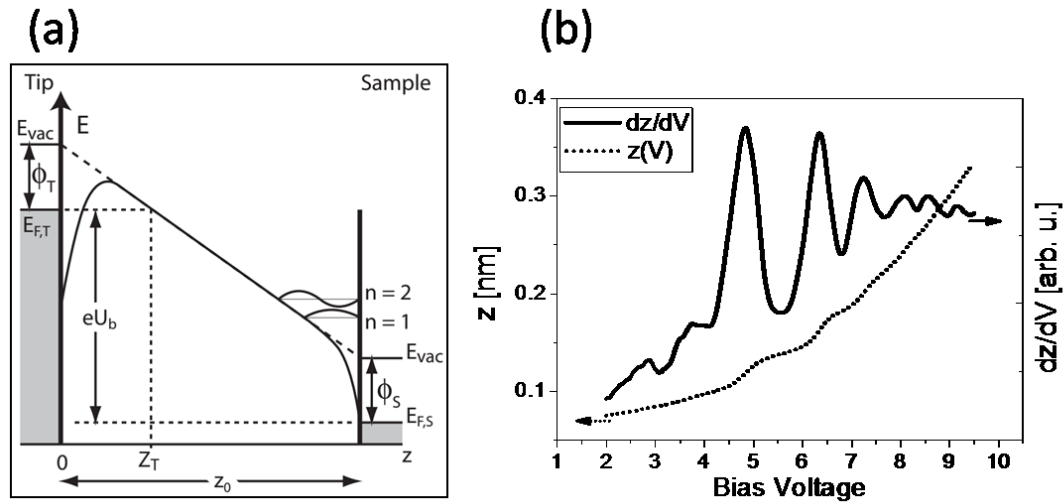


Fig. 2.7: (a) Energy diagram for field emission [7] (image from [12]), (b) typical $z(U)$ and dz/dU spectra for Si(100) taken with a Pt tip.

2.2.8 Experimental details

All STM results presented in this thesis were obtained under ultra-high vacuum conditions at pressures lower than 1×10^{-10} mbar. In this section, the UHV chambers and STM system used in the present work will be discussed.

A schematic of the Createc STM/AFM system is depicted in Fig. 2.8(a) and (b). The system consists of an analysis and a preparation chamber with a gate valve isolating one from the other. It also has a fast entry load lock that is used to load samples into the system without breaking the vacuum in the inner chambers. The analysis and preparation chambers have a base pressure better than 1×10^{-11} and 5×10^{-11} mbar respectively, which is maintained by ion pumps and titanium sublimation pumps (TSP). The load lock is connected with a turbo molecular pump which is used to achieve pressures in the 10^{-7} mbar range. Once a high vacuum has been obtained, the system is baked at approximately 120 °C for 48 – 72 hours. Ion pumps and TSPs are turned on at the end of baking which reduces the pressure to the UHV regime.

The preparation chamber is equipped with a manipulator to transfer and process samples, a carousel to store tips and samples, Ar^+ sputtering gun, a low energy electron diffraction (LEED) system, a mass spectrometer, and a Hydrogen cracker. The manipulator is capable of working either at room temperature or at low temperatures. Liquid nitrogen is passed through the inner tube of the manipulator in order to cool it down to approximately 80 K. Cooling the manipulator during the thermal treatment of the sample reduces outgassing of the sample holder and manipulator. The manipulator is equipped for thermal processing of samples through resistive heating (Fig. 2.9(a)) and also indirect heating over button heaters (Fig. 2.9(b)).

The Createc LT-STM/AFM can be operated at liquid Nitrogen (77 K) or liquid Helium (4.7 K) temperatures; however all STM results presented in this thesis were measured at liquid Nitrogen temperature. The STM cryostat is a typical bath-type cryostat made of two concentric chambers or dewars isolated with vacuum to minimize the boil-off rate. The STM scanner, housed in a temperature-shielded STM chamber, is attached to the inner cryostat. When operating the STM

at liquid Nitrogen temperature, both the dewars are filled with liquid nitrogen. The STM scanner along with the sample is suspended on springs during scanning to lower the high frequency mechanical noise. The piezo-driven scanner has a scan

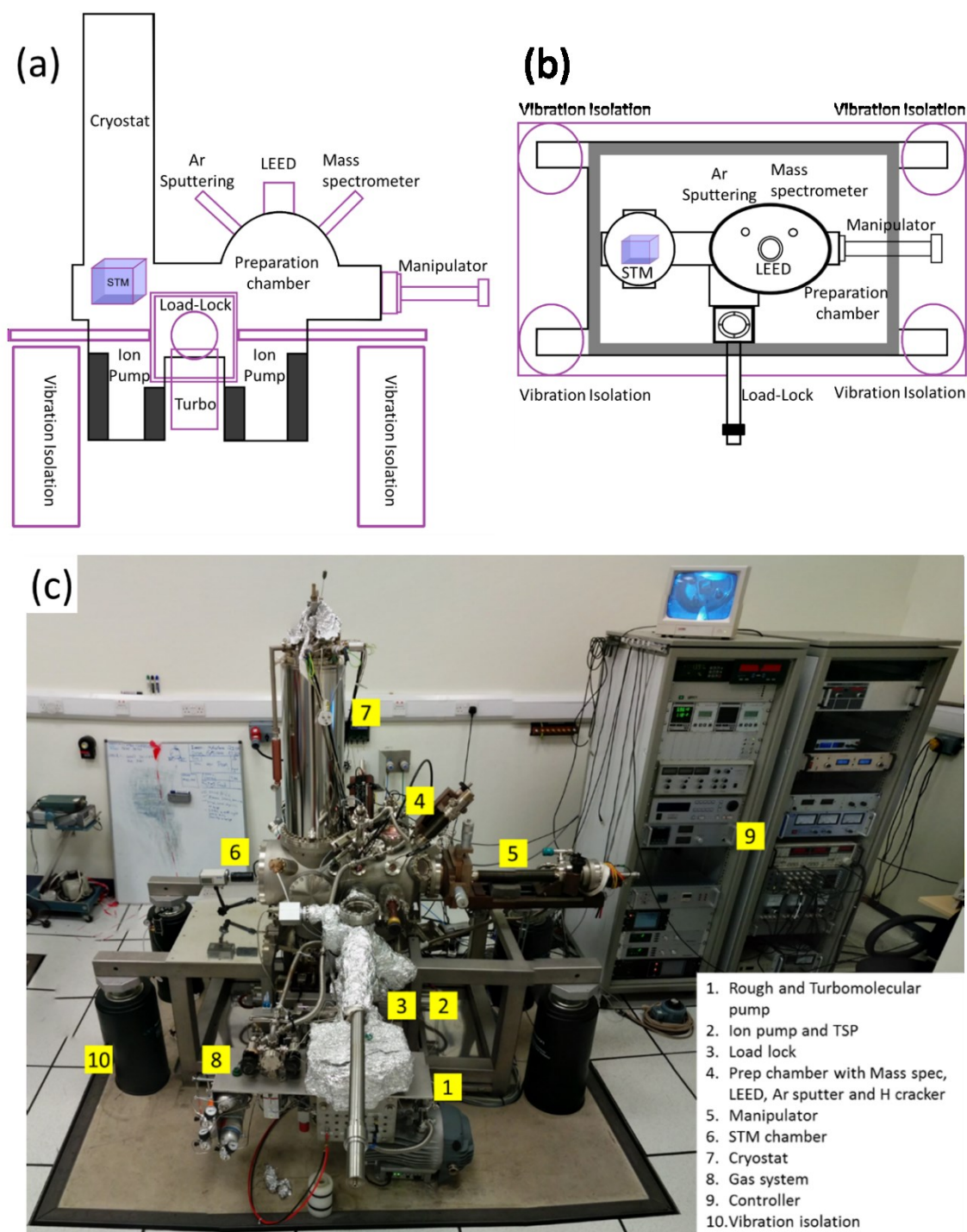


Fig. 2.8: Schematics of the LT-STM. (a) Side view illustrating pumping system, preparation chamber, STM chamber and vibration isolation system. (b) Top view showing the load-lock and manipulator. (c) shows the Createc LT STM.

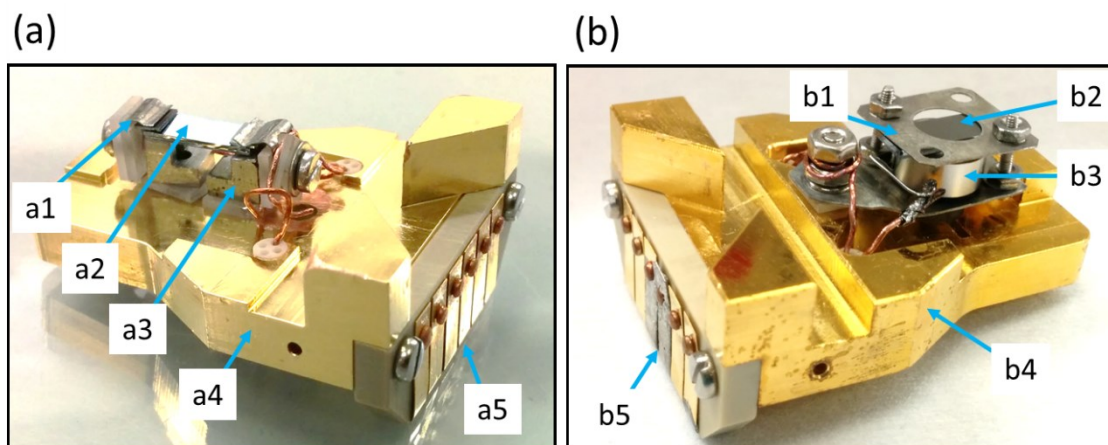


Fig. 2.9: (a) shows a direct heating STM sample holder. Here (a1) a metal spring for electric contact and to hold the sample, (a2) an SOI sample, (a3) molybdenum base to support the sample, (a4) sample holder, and (a5) electrodes. (b) shows an indirect heating sample holder. (b1) a molybdenum plate that holds the sample, (b2) an SOI sample, (b3) button heater, (b4) sample holder, and (b5) electrodes.

range of $4.2 \mu\text{m} \times 4.2 \mu\text{m} \times 0.4 \mu\text{m}$ in the x, y and z directions respectively. A platinum-coated tungsten tip is used to measure STM and STS data.

2.2.9 Tip preparation

The tip formation of a probe is an important aspect of tunneling microscopy as the operating characteristics of the entire microscope depends upon the single atom at the very end of the probe tip. The shape, size and chemical composition of the tip determines the quality of the data acquired by the STM [36]. The primary requirement of a high quality probe tip is its sharpness. UHV-STM probe tips are typically made from tungsten by electrochemical etching of a wire either by an AC or a DC field. The most widely used etchants are aqueous solutions of sodium hydroxide or potassium hydroxide.

A tungsten wire of about 10 mm length and 0.05 – 0.25 mm diameter was mounted lengthwise on a vertical manipulator and positioned at the center of a small beaker containing 4 M sodium hydroxide solution, as shown in Fig. 2.10. A ring of platinum wire was immersed in the solution. The tungsten wire acts as the anode and the platinum ring as the cathode. The tungsten wire was lowered 2 – 3 mm below the surface of the solution and a potential difference of 2 – 6 V was applied between the tip and the ring to initiate the reaction. The etching occurs

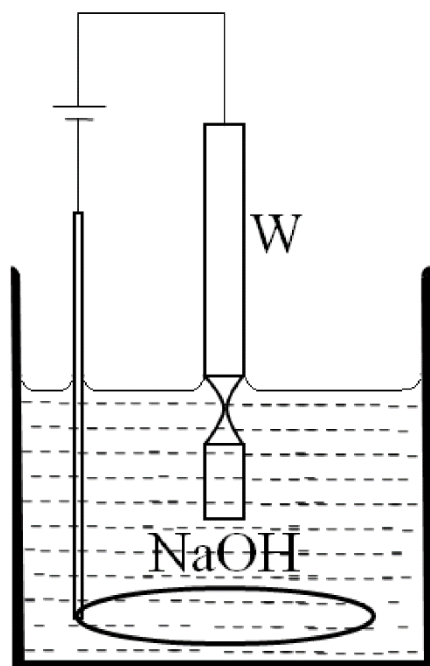


Fig. 2.10: Schematic representation of an electrochemical cell showing the etching of a tungsten wire in sodium hydroxide solution. The tungsten wire acts as the anode, while the stainless steel ring acts as the cathode.

mainly at the meniscus. When the weight of the immersed tungsten overcomes the tensile strength of the etched section of the wire, the wire breaks at the necked region leaving a sharp tip at the end. A differential current monitoring circuit measuring the etching current was used to cut off the potential difference when a sharp change in the current was sensed. The tip was then washed in deionized water to remove residual salt on the wire. After the probe tip was loaded into the UHV chamber, the tip was bombarded with electrons to remove any contaminants. Finally, after the tip was mounted on the STM scanner the apex of the tip was coated with platinum by a sequence of controlled crashes on a platinum crystal sample. A thorough analysis and confirmation of the tip quality by spectroscopic measurements was performed to ensure that the tip was suitable for semiconductor sample measurements [37].

2.3 Low energy electron diffraction (LEED)

LEED is a surface analysis technique based on diffraction of electrons from periodic surface structures. When the electron beam incident on the surface has a

de Broglie wavelength comparable to the interatomic spacing on the surface, diffraction will occur. The resulting diffraction pattern describes the periodicity of

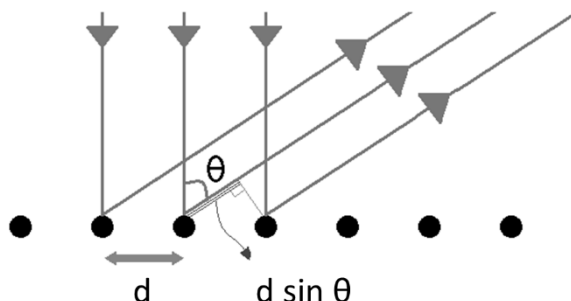


Fig. 2.11: Bragg diffraction. Electron beam of wavelength λ incident upon and scattered by a 1-D chain of atoms with an atomic separation a . A path difference of $d \sin(\theta)$ when equal to $n\lambda$ results in constructive interference.

the surface atoms. The diffraction of the electrons from the surface atoms is defined by Bragg's law [38]. A beam of electrons with a wavelength λ incident on a crystal scatters and undergoes diffraction from an atomic structure with an interatomic distance of a , as shown in the Fig. 2.11. Depending on the angle of diffraction, the path length difference between the scattered waves from different atomic planes of the crystal can lead to constructive or destructive interference. The path

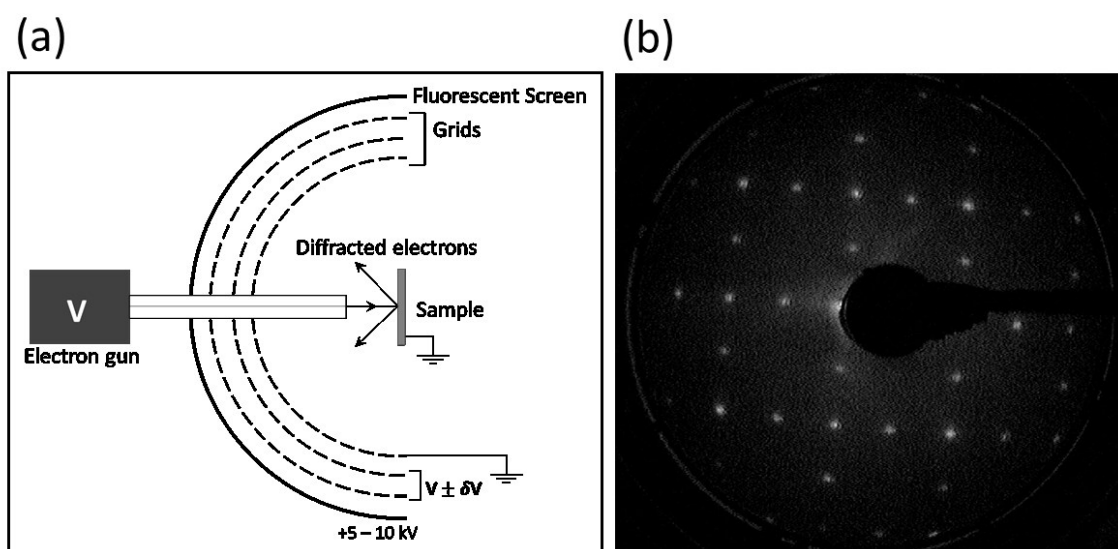


Fig. 2.12: (a) Schematic of a LEED experimental set-up. (b) LEED pattern recorded from a clean Si(100) surface at an energy of 100 eV.

difference is given by $d \sin(\theta)$ where θ is the angle between the incident and diffracted waves (Fig. 2.11). A path difference equivalent to an integer multiple (n) of the wavelength leads to constructive interference. The relation for constructive interference between two waves at normal incidence is given by

$$n\lambda = d \sin(\theta)$$

The Bragg diffraction measures the atomic distances in inverse space and therefore the LEED pattern describes the reciprocal space.

The experimental set-up for LEED is shown in Fig. 2.12(a). The instrument consists of an electron gun, a fluorescent screen and a series of grids. Electrons emitted from the gun are accelerated towards the sample with a voltage V between 10 – 500 V. The electrons that are scattered and diffracted by the sample then pass through a series of grids and finally hit the fluorescent screen resulting in scintillations. The outer grid is held at the ground potential to confine the field and the inner grids are kept at voltage $V \pm \delta V$ in order to ensure that only the elastically scattered electrons reach the screen. Fig. 2.12(b) shows a 2×1 LEED pattern recorded from a clean Si(100) surface at 100 eV.

2.4 X-ray photoelectron spectroscopy (XPS)

XPS is a widely used qualitative surface analysis technique that yields chemical information about the surface of the sample. XPS is based on the photoelectric effect: photons of known energy incident on the sample causing the emission of photoelectrons from atomic orbitals. The binding energy of the photoelectrons in the material can be calculated using the known energy of the x-rays and the measured kinetic energy of the emitted electrons, as described in the following equation [39]:

$$E_{K.E} = h\nu - E_b - \phi_s \quad (2.14)$$

where, $E_{K.E}$ is the kinetic energy of the emitted electron, $h\nu$ is the energy of the incident photon, E_b is the binding energy of the electron and ϕ_s is the work function of the spectrometer, since the sample and the spectrometer are connected to a common ground. For a known $h\nu$ and ϕ_s and a measured $E_{K.E}$, the binding energy E_b of the photoelectron can be calculated. In an XPS experiment, a monochromatic x-ray source of known energy $h\nu$ is used. Mg and Al are chosen for

anode materials as the characteristic x-ray emission spectrum for each element is dominated by a single emission line. The energy of the main Mg x-ray emission line is 1253.6 eV, while the main Al line is at 1486.7 eV [39]. Each element has a characteristic set of core level binding energies. In addition, the binding energy is sensitive to the chemical environment of the element. Therefore, XPS can be used to determine both the elemental composition of the sample surface material and also analyze the chemical states of the atoms [19, 20, 40]. As the electron has a low mean free path in a material, only the electrons emitted by the top few layers of the sample reach the detector and therefore XPS is a surface-sensitive technique. However, the surface sensitivity or the depth range of XPS measurements can be varied to a certain extent with angle dependent XPS measurements. The surface sensitivity of the measurements increases as the measurement angle with respect to the analyzer decreases. Angle-dependent XPS measurements have been used in this work to study the oxide desorption and surface morphology of the SOI device layer under various thermal processing conditions.

A VG Scienta ESCALab MKII XPS system equipped with a Mg/Al twin anode x-ray source was used in this work. The energy of the Mg x-ray emission line is 1253.6 eV, while the main Al emission line is at 1486.7 eV. The system has a concentric hemispherical analyser with an array of three channeltron detectors. The data acquisition and processing was performed using the Thermo Scientific Advantage software. Details about the XPS measurements and the data processing is described in Chapter 3 in greater detail.

2.5.1 Atomic Force Microscopy (AFM)

AFM is a powerful scanning probe microscopy technique similar to STM that is used to visualize and measure surface structure and properties with an extraordinary resolution [41]. However, unlike STM, AFM measurements are seldom affected by the measuring environment or the type of sample [42]. Therefore AFM can be performed in air, liquid or vacuum [42] on any material, irrespective of its opaqueness, hardness [43, 44] or electrical conductivity. In an AFM, unlike a conventional microscope, the surface morphology is imaged not using light but rather by ‘touching’ the surface using a sharp probe or a tip. The

height of surface features are recorded at every point or pixel within a 2D array over the surface. The height data acquired is then processed by an image processing software and the 3D data is displayed with a colour gradient or grey scale indicating the height features. A typical height measurement range in an AFM extends up to a 10s of micrometres with a sub-nanometre resolution in z direction and in the x-y plane the scanning range can be as high as 100 μm with a resolution of 1nm or lesser. The highest achievable resolution is mainly limited by the sharpness of the probe tip - with an atomically sharp tip, atomic resolution can be achieved [45-49]. As the AFM probe physically interacts with the sample, AFM can also be used as an analytical tool to quantitatively study and map mechanical, electrical and magnetic properties of samples [8].

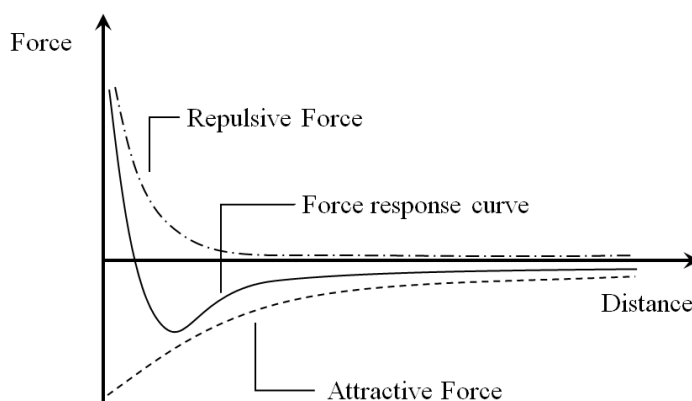


Fig. 2.13: Force – Distance plot showing the interaction of an AFM tip with the surface. The dashed and dashed-dotted curves show the attractive and repulsive forces respectively, and the solid curve shows the resultant force response [8].

The two principal modes of operation for AFM are contact mode and tapping mode. In contact mode the tip is in continuous contact with the sample surface. In this mode the tip is in the repulsive regime of the van der Waals interaction curve, as indicated in Fig. 2.13. A constant force is maintained between the tip and the surface during scanning by maintaining a constant laser deflection from the cantilever. This is achieved via the feedback system connected to the z-axis piezo system. In tapping mode the tip cantilever is allowed to oscillate at or near its resonance frequency and the cantilever oscillation amplitude or frequency is monitored. As the tip approaches the surface, the tip oscillation amplitude, phase,

and frequency changes. The amplitude, frequency or phase can be used by the feedback circuit to control and record the tip position during scanning and also extract significant details about the sample such as the stiffness [50], adhesion and chemical inhomogeneity on the sample surface [8].

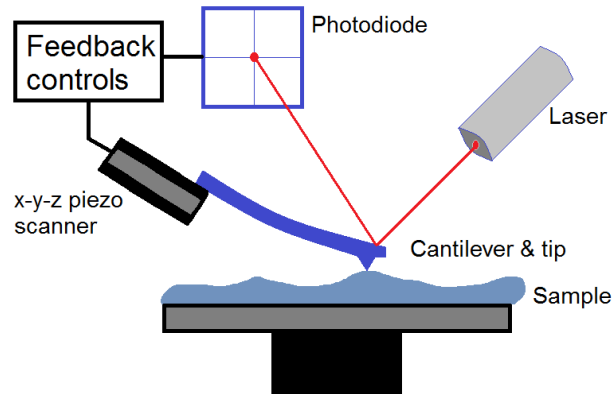


Fig. 2.14: Illustration of the basic components of an AFM. x- and y- piezoelectric scanners move the tip across a surface while the z- piezo oscillates the cantilever and also controls the height of the tip over the sample. A laser is reflected off the reflective coating on the back of the cantilever onto a photodiode that detects the changes in the oscillation amplitude, causing a feedback mechanism to move the tip in the z-axis [8].

An AFM operates by raster-scanning a sharp probe tip over the surface of the sample while measuring the sample height at every pixel point. Usually the probe tip is attached to a flexible micro-cantilever which bends on reaching the surface due to van der Waal forces (see Fig. 2.13). A laser beam is made to reflect off the back of the cantilever, which is coated with reflective material to maximize

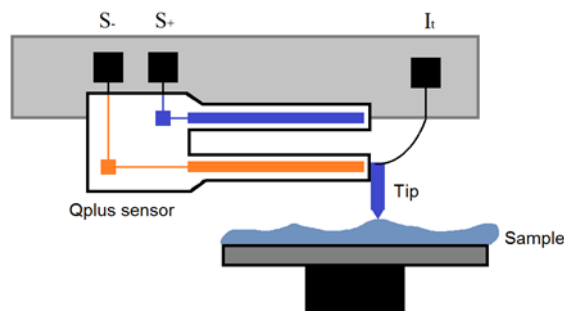


Fig. 2.15: Schematic of a Q-plus AFM/STM sensor.

the laser reflection, as shown in Fig. 2.14, and fall onto a quadrant detector. The bending of the cantilever and thus the tip movement is measured and quantified

by recording the position of the laser spot on the detector. Alternatively, the surface feature height can also be measured by a tip mounted on a quartz tuning fork (see Fig. 2.15) [51]. The tuning fork system is generally called a qplus sensor and is commonly used in ultra-high vacuum AFM and AFM-STM systems. The tuning fork is allowed to oscillate at its resonance frequency and as the tip approaches the surface, a shift in resonance frequency is observed due to van der Waals interaction between the tip and the surface.

2.5.2 Phase contrast imaging

When operating an AFM in tapping mode, it is possible to record changes in the amplitude, phase and excitation voltage of the cantilever oscillation. These signals define the tip-sample interaction. In addition to sample topography, properties such as material stiffness, tip-sample adhesion, and friction can be characterized [50, 52-54]. As the probe ‘taps’ the sample surface, the amplitude and phase response relative to the driving oscillation is recorded. The phase signal shifts as the tip encounters variation in the surface material properties (see Fig. 2.16) and this variation is depicted with color contrast in the phase image. This

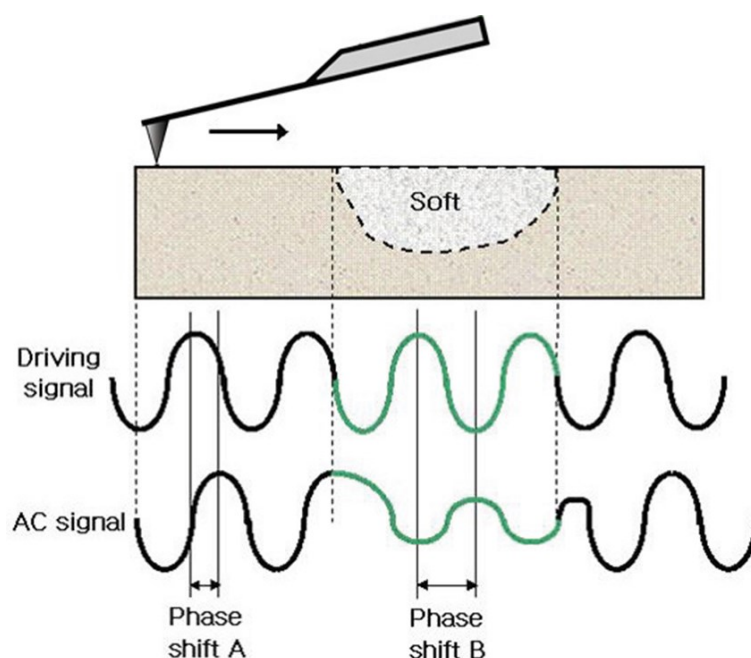


Fig. 2.16: The phase lag changes depending on the mechanical properties of the sample surface (Image from [6]).

allows AFM in tapping mode to measure ultra-low forces, determining the properties of the sample with high spatial resolution. For example, with the use of an appropriate tip, relative variation in the local stiffness of the sample can be mapped with high sensitivity through phase contrast imaging [55]. Therefore by combining AFM phase contrast imaging with chemical analysis like XPS, the nature of surface inhomogeneity on the sample can be studied.

In tapping mode, a probe oscillating at high frequency is employed for imaging. In each oscillation cycle, the tip apex spends some time close to and in contact with the sample surface resulting in the tip experiencing attractive and repulsive forces [50]. A freely oscillating cantilever with resonance frequency ω_0 , mass m and quality factor Q , its spring constant k is given by

$$k = m\omega_0^2 \quad (2.15)$$

As a function of vibrational frequency ω , the phase angle ϕ (in radians) of the free cantilever oscillation is expressed as [50]

$$\phi = \tan^{-1} \left(\frac{m\omega\omega_0}{Q(k - m\omega^2)} \right) \quad (2.16)$$

As a function of ω , this angle varies sharply around ω_0 . At $\omega = \omega_0$, ϕ is $\pi/2$; ϕ is smaller than $\pi/2$ for $\omega < \omega_0$, and larger than $\pi/2$ for $\omega > \omega_0$. The interaction of tip and sample changes the vibrational characteristics. Essentially, the tip-sample force interaction changes the force constant of the cantilever to a new effective value $k_{eff} = k + \sigma$, where σ represents the sum of the force derivatives of all the forces F_i acting on the cantilever

$$\sigma = \sum_i \partial F_i / \partial z \quad (2.17)$$

where z represents the relative displacement between the tip and sample [50]. Therefore Eq. 2.16 can be expressed as

$$\phi = \tan^{-1} \left(\frac{m\omega\omega_0}{Q(k + \sigma - m\omega^2)} \right) \quad (2.18)$$

when σ is very small in magnitude compared with k , ϕ_0 the phase angle ϕ at ω_0 is given by [50]

$$\phi_0 = \tan^{-1} \left(\frac{k}{Q\sigma} \right) \quad (2.19)$$

and the phase shift $\Delta\phi_0$, between the free and interacting cantilever can be defined as [50]

$$\Delta\phi_0 = \frac{\pi}{2} \tan^{-1} \left(\frac{k}{Q\sigma} \right) \approx \frac{Q\sigma}{k} \quad (2.20)$$

Thus the phase shift is positive when the overall force acting on the tip is repulsive, and negative when the overall force is attractive [50]. When overall force derivative σ is dominated by the surface stiffness, the phase image can provide a map of stiffness variation on the surface of the sample: stiffer region showing more positive phase shift and hence appearing brighter in phase image. Phase contrast imaging has been used in this work to study the effect of thermal treatment on the morphology and chemical composition of SOI [33].

2.5.3 Kelvin probe microscopy (KPM)

Kelvin Probe Microscopy (KPM) is a tool that enables imaging of local contact potential difference and surface potential or the work function of samples. KPM can be used on a wide range of materials and is incorporated in most research grade AFMs as an additional mode. Since its first introduction in 1991 by

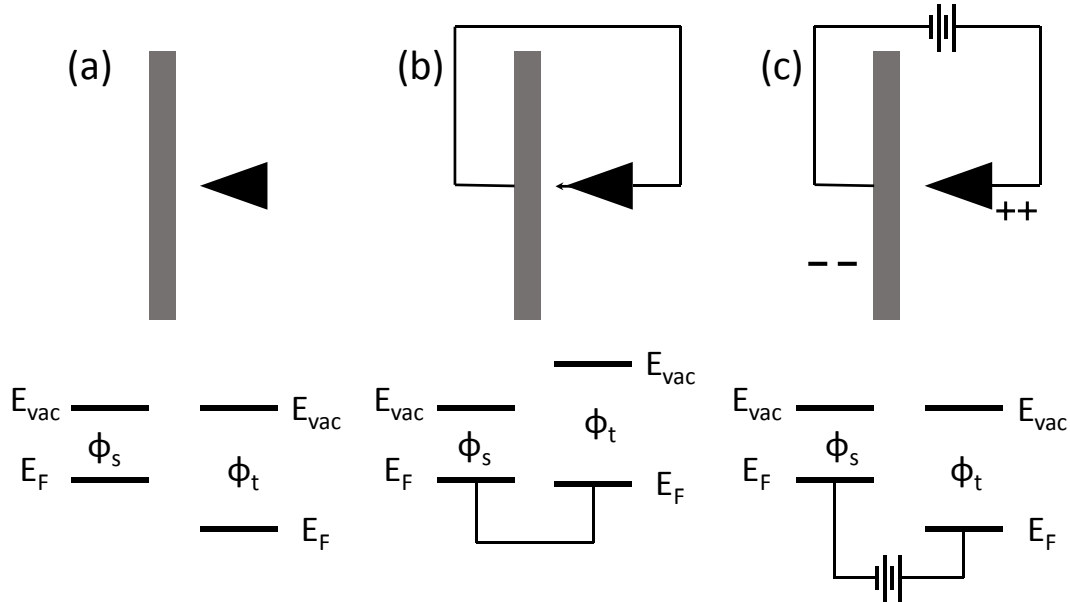


Fig. 2.17: Ideal tip and sample electronic energies at the vacuum level E_{vac} and Fermi level E_F , for the case of dissimilar work function. Materials that are a) not electrically grounded, b) electrically grounded, and c) electrically connected with a battery in between, of the exact potential difference needed to match the work-function difference and thus align vacuum levels [10]. Φ_s and Φ_t are the work function of sample and tip, respectively.

Nonnenmacher et al. [56], KPM has been extensively used in the research community as a tool to characterize, with nanometre scale resolution, a diverse range of materials, including metals, semiconductors [57], organic materials [58-60] and also biological materials [61, 62]. One of the main advantages of the tool is its ability to study the electronic properties of individual metal and semiconductor nano-structures and devices with nanometre spatial resolution.

When two conductors are brought into electrical contact the Fermi energies of conductors line up (see Fig. 2.17). This happens through transfer of electrons from the material with lower work function to that with a higher work function. If the conductors are brought close together so that they form a parallel plate capacitor, equal and opposite charges are induced on the surfaces [8]. This built-up potential is called the surface potential or the Contact Potential Difference (CPD). CPD is equal to the potential difference of the two materials. CPD can be measured by applying an external potential to the capacitor until the surface charges disappear [1]. This can be done using a vibrating electrode technique and the nulling concept [63]. When the tip is made to vibrate vertically over the sample, the capacitance varies with the distance and this leads to an AC current. The external potential that nullifies this AC current will be equal to the CPD.

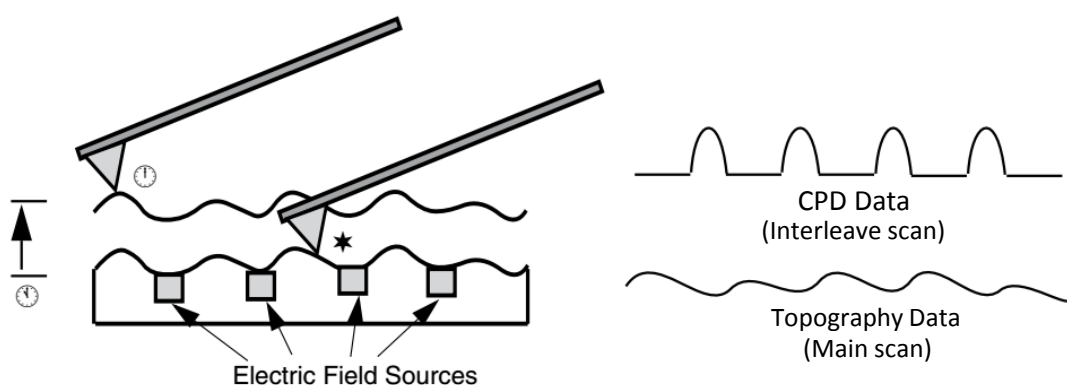


Fig. 2.18: LiftMode principles used in CPD measurements (Image from [1])

The KPM measurements reported in this thesis were carried out in a Bruker AFM system. This system uses a two-pass interleaved process for CPD measurements called LiftMode (see Fig. 2.18). The surface topography is obtained

by tapping mode in the first pass and on the second pass the tapping drive piezo is turned off and an oscillating voltage $V_{AC} \sin \omega t$ is applied to the probe tip. When there is a DC voltage difference between the tip and sample, an oscillating electric force with frequency ω is observed. This oscillating force vibrates the tip cantilever whose amplitude can be detected. Further, a DC voltage is applied to the tip to bring the cantilever vibration to zero and this DC voltage is equal to the local CPD. CPD measurements have also been done in the UHV STM-AFM system with a qplus tip. In this case, while the tip is allowed to oscillate at the resonance frequency at a fixed distance from the surface, the change in force, df , is recorded as the voltage is varied. At the voltage corresponding to CPD, a minimum is obtained in the df curve. CPD and KPM data were recorded at both UHV and atmosphere in order to observe the variation in SOI work function and are described in Chapters 2 and 3 of this thesis.

2.6 Electron microscopy

Electron microscopy is a powerful characterization technique that uses beam of electrons to generate high resolution nano-scale images of samples. Since electrons have considerably smaller (de Broglie) wavelengths than light, electron microscopes can achieve much higher magnification and greater resolution in comparison to optical microscopes. Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) are the two main types of electron microscopy.

2.6.1 Scanning electron microscopy (SEM)

One of the first commercial scanning electron microscope was developed by Charles Oatley, in 1965 [64]. SEM uses a focused electron beam to scan line by line over the sample in a rectangular raster pattern, collecting the reflected and scattered electrons through various detectors to form an image of the sample. The high energy incident electrons on the sample leads to various elastic and inelastic interactions with the sample atoms leading to emission of *backscattered electrons* (BSE) and *secondary electrons* (SE) respectively. While a contrast in SE image gives the morphology of the sample, BSE image contrast is produced due to the variation in the atomic number of the elements in the sample. The interaction of

the electrons with the sample also leads to the emission of characteristic x-rays which permits a quantitative elemental analysis of the sample. This analysis technique is known as Energy Dispersive X-ray Spectroscopy (EDXS or EDS). SEM

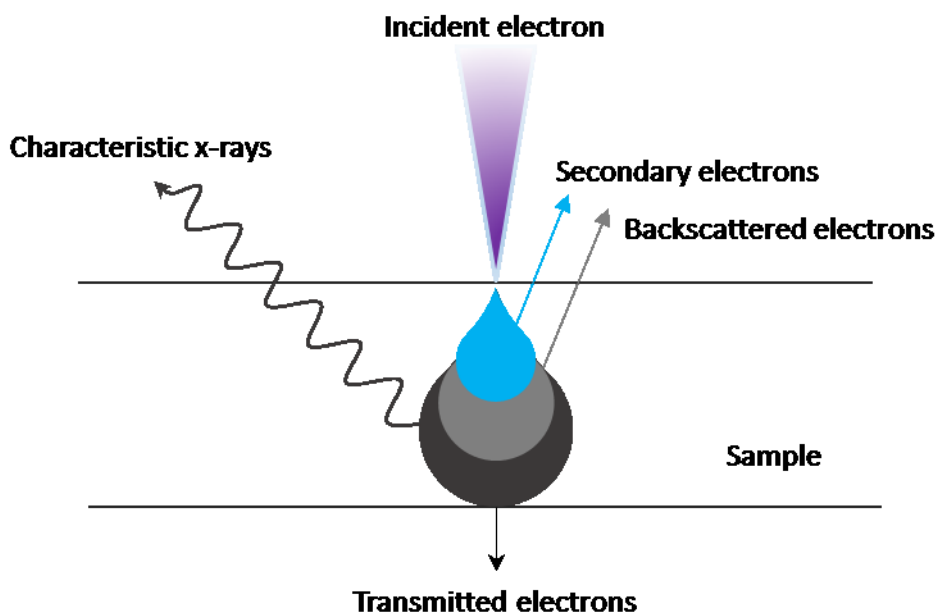


Fig. 2.19: Schematic of the various interactions between the electron beam and the sample.

has been extensively used in this work to image the fabricated nano-structures and devices and also to study the varying surface morphology of SOI due to thermal processing. All SEM analysis were carried out in a Zeiss Ultra FE-SEM and Zeiss Supra FE-SEM.

2.6.2 Electron beam lithography (EBL)

The scanning electron microscope can also be used for fabrication of nano-structures using a processes known as Electron Beam Lithography (EBL). In order to carry out EBL, the sample is initially coated with an EBL resist. An EBL resist is an electron sensitive material, i.e. a material that undergoes chemical changes such as crosslinking when exposed to a beam of electrons. Typically, the chemical changes in the resist material due to exposure results in the alteration of its solubility property. A resist that dissolves in a solvent after the exposure is used as a positive resist while a resist that loses its solubility property after the exposure is used as a negative resist. A thin film of resist, usually several tens of nanometres

thick, is coated on sample wafer using a spin coater and the focused electron beam in a SEM is used to write patterns on the resist. Samples are then developed by rinsing in a solvent for a specified time. This process, depending on the type of resist used, will leave either a nano-sized resist pattern on the sample surface or nano-sized hole or etch pattern on the resist film. In the experiments described in this thesis, EBL resists such as ma-N 2403, Hydrogen silsesquioxane (HSQ) and PMMA were used to fabricate nano-structures on SOI. The SOI samples with the patterned resist were further processed with reactive ion etching to obtain nano-structures on SOI. All EBL processes were carried out with a Zeiss Supra FE-SEM in the Advanced Microscopy Laboratory (AML) at Trinity College Dublin and Vistec EBPG 5000 Plus system in Helmholtz Nanoelectronic Facility (HNF), Jülich, Germany.

2.6.3 Transmission electron microscopy (TEM)

A Transmission electron microscope, as the name suggests, is a type of electron microscope that operates in a transmission mode where a beam of high energy electrons, typically ranging from 50 – 300 keV, is transmitted through the sample and collected by detectors on the other side. Due to the higher electron acceleration voltage used, a TEM can generally attain magnification and resolution that is orders of magnitude higher than SEM. Apart from imaging, TEM can also be used in to study the crystallinity of nano-structure samples using a technique called selected area diffraction (SAD). For electrons to be able to pass through a sample, it must be less than 100 nm thick. Nanostructure samples are transferred on to a TEM grid either by drop casting or by lamella preparation. Thin film samples such as SOI are thinned and processed into lamella using a Focused Ion Beam (FIB) tool. For this work, SOI samples were processed into lamellae in a Zeiss Auriga FIB system, using a reactive gas injection system for reactive ion etching and deposition of a Pt capping layer. The cross section TEM analysis of SOI was carried out in an FEI Titan 80-300 (S) TEM system.

2.7 Inductively coupled plasma – Reactive ion etching (ICP-RIE)

Plasma etching is a process of modifying the sample surface by exposing it to a plasma of appropriate gas mixtures which is either charged or neutral. A

plasma chamber typically uses a capacitively or inductively coupled radio-frequency voltage to excite the plasma. Reactive ion etching (RIE) is a type of plasma etching that contains large number of high energy ions impinging on the etch surface. Materials can be etched with a plasma of gases composing of a neutral feed gas and dissociated molecules including some radicals. Reactive F radicals used in the ICP process chemically react with silicon, forming highly volatile product such as SiF_4 which then etches the wafer. RIE has an increased etch rate due to the additional ion bombardment compared to the normal chemical plasma etching and this results in the vertical anisotropic etch profile [14]. Additionally, a mixture of CHF_3 and SF_6 feed gas used in the RIE process increases the anisotropy in the etching. An etch-resistant polymer is deposited on the side walls of the structures during etching, which enables fabrication of structures tens of nanometers wide and etched hundreds of nanometres deep. To fabricate structures and clean the samples an Oxford Instruments ICP-RIE system was used, with feed gasses such as SF_6 , CHF_3 , Ar and O_2 .

2.8 Spectroscopic Ellipsometry

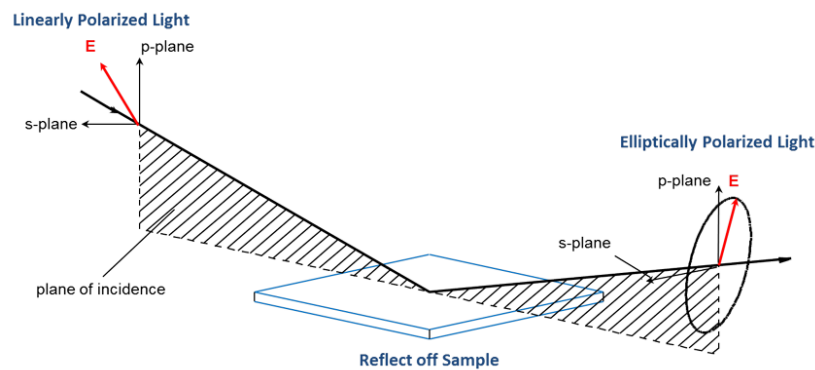


Fig. 2.20: Interaction of the linearly polarized light with the sample [4].

Spectroscopic Ellipsometry (SE) is a non-contact optical technique that is mainly used to determine the thickness and optical constants of thin film materials. SE can also be used to characterize the material composition, crystallinity, roughness, doping concentration and several other material properties that are associated with the changes in optical response [4]. The polarization of a beam of

light is altered when it is reflected from the surface of a material or transmitted through it. An ellipsometer measures the change in polarization state induced by reflection from the sample by recording the amplitude ratio ψ and the phase difference Δ between the s and p components of the polarized light. The relation between ψ and Δ is given by [65]

$$\tan(\psi) e^{i\Delta} = \rho = \frac{r_p}{r_s}$$

where ρ is the ratio of the reflectivity of p-polarized (r_p) and s-polarized (r_s) light and $\tan(\psi)$ is the magnitude of the reflectivity ratio. In SE, ψ and Δ values are recorded as a function of wavelength which enables simultaneous determination of various physical properties. SE was used in this work to determine the thickness of the SOI films. Measurements were carried out in an Alpha-SE Ellipsometer by J. A. Woollam Co., in a rotating compensator (RCE) configuration and attached with charge coupled detector (CCD) detector. The angle of incidence of the polarized light was set to 65°, 70° and 75° in turn and scanned through the wavelength range of 380 - 900 nm. Acquired data were fit with an SOI model. The accuracy of the ellipsometry data were independently verified using standard commercial samples and cross-sectional TEM analysis. The deviation of the measured SOI and BOX thickness between SE and other techniques were found to be less than ± 0.5 nm for a broad range of samples.

2.9 Secondary Ion Mass Spectroscopy

Secondary Ion Mass Spectroscopy (SIMS) is an extremely sensitive material analytical tool that is used to characterize the composition of solid material surfaces or thin films. The surface of the material under investigation is sputtered with a focused ion beam where the highly energetic interaction of the primary ions with the sample material ionises the elements in the sample. A negatively charged primary ion produces positively charged secondary ions and vice versa. Thus ejected secondary ions are collected and analysed with a mass spectrometer. SIMS analysis was adopted in this work to determine the doping density and doping concentration profile in ion implanted SOI. The variation in the doping concentration profile was studied as a function of annealing at various high temperatures to understand the diffusion and segregation of dopants in SOI films.

The SIMS data were also compared with the electrical resistivity measurements of thinned SOIs to determine the effective doping concentration in the ultra-thin films. All SIMS measurements were performed in a TOF SIMS 5 system at University of Limerick Ireland.

2.10 References

1. *Dimension 3100 Manual*. 2005: Veeco Instruments Inc. / Bruker.
2. Kubby, J.A. and J.J. Boland, *Scanning tunneling microscopy of semiconductor surfaces*. Surface Science Reports, 1996. **26**(3): p. 61-204.
3. GOLOVCHENKO, J.A., *The Tunneling Microscope: A New Look at the Atomic World*. Science, 1986. **232**(4746): p. 48-53.
4. *Spectroscopic Ellipsometry*. Available from: <https://www.jawoollam.com/resources/ellipsometry-tutorial/what-is-ellipsometry>.
5. Chen, C.J., *Introduction to scanning tunneling microscopy*. Vol. 4. 1993: Oxford University Press on Demand.
6. *Phase Imaging*. Available from: <http://www.parkafm.com/index.php/park-spm-modes/91-standard-imaging-mode/221-phase-imaging-phase-detection-microscopy-pdm>.
7. Coombs, J. and J. Gimzewski, *Fine structure in field emission resonances at surfaces*. Journal of Microscopy, 1988. **152**(3): p. 841-851.
8. Eaton, P.J. and P. West, *Atomic force microscopy*. 2010, Oxford; New York: Oxford University Press.
9. Simmons, J.G., *Generalized Formula for the Electric Tunnel Effect between Similar Electrodes Separated by a Thin Insulating Film*. Journal of Applied Physics, 1963. **34**(6): p. 1793-1803.
10. Haugstad, G., *Atomic Force Microscopy: Understanding Basic Modes and Advanced Applications*. 2012: Wiley.
11. Tersoff, J. and D.R. Hamann, *Theory and Application for the Scanning Tunneling Microscope*. Physical Review Letters, 1983. **50**(25): p. 1998-2001.
12. Shantyr, R., *Scanning tunneling microscopy/scanning tunneling spectroscopy on growth, atomic and electronic structure of Co oxide and Mn oxide films on Ag(001)*. 2004.
13. *Introduction to Vacuum Technology* Available from: <https://www.pfeiffer-vacuum.com/en/know-how/introduction-to-vacuum-technology/fundamentals/>.

14. *Inductively Coupled Plasma*. April 2017]; Available from: <http://www.oxford-instruments.com/products/etching-deposition-and-growth/plasmaetch-deposition/icp-etch>.
15. Binnig, G., et al., *Tunneling through a controllable vacuum gap*. Applied Physics Letters, 1982. **40**(2): p. 178-180.
16. Binnig, G., et al., *Surface Studies by Scanning Tunneling Microscopy*. Physical Review Letters, 1982. **49**(1): p. 57-61.
17. Wiesendanger, R., *Scanning Probe Microscopy and Spectroscopy: Methods and Applications*. 1994: Cambridge University Press.
18. Tersoff, J. and N.D. Lang, *1 - THEORY OF SCANNING TUNNELING MICROSCOPY A2 - Stroscio, Joseph A*, in *Scanning Tunneling Microscopy*, W.J. Kaiser, Editor. 1993, Academic Press: San Diego. p. 1-29.
19. Woodruff, D.P. and T.A. Delchar, *Modern Techniques of Surface Science*. 1994: Cambridge University Press.
20. Vickerman, J.C., *Surface analysis: the principal techniques*. 1997: John Wiley.
21. Bardeen, J., *Tunnelling from a Many-Particle Point of View*. Physical Review Letters, 1961. **6**(2): p. 57-59.
22. Reittu, H.J., *Fermi's golden rule and Bardeen's tunneling theory*. American Journal of Physics, 1995. **63**(10): p. 940-944.
23. Tersoff, J. and D.R. Hamann, *Theory of the scanning tunneling microscope*. Physical Review B, 1985. **31**(2): p. 805-813.
24. Chen, C.J., *Theory of scanning tunneling spectroscopy*. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 1988. **6**(2): p. 319-322.
25. Bussmann, E., et al., *Thermal instability of silicon-on-insulator thin films measured by low-energy electron microscopy*. IOP Conference Series: Materials Science and Engineering, 2010. **12**: p. 012016.
26. Legrand, B., et al., *Formation of silicon islands on a silicon on insulator substrate upon thermal annealing*. Applied Physics Letters, 2000. **76**(22): p. 3271.
27. Yang, B., et al., *Self-organization of semiconductor nanocrystals by selective surface faceting*. Physical Review B, 2005. **72**(23).

28. Legrand, B., et al., *Thermally assisted formation of silicon islands on a silicon-on-insulator substrate*. Journal of Applied Physics, 2002. **91**(1): p. 106.
29. Aouassa, M., et al., *The kinetics of dewetting ultra-thin Si layers from silicon dioxide*. New Journal of Physics, 2012. **14**(6): p. 063038.
30. Leroy, F., et al., *Dynamics, anisotropy, and stability of silicon-on-insulator dewetting fronts*. Physical Review B, 2012. **85**(19).
31. Tabe, M., et al., *Formation of high-density silicon dots on a silicon-on-insulator substrate*. Applied Surface Science, 1999. **142**(1–4): p. 553-557.
32. Nuryadi, R., Y. Ishikawa, and M. Tabe, *Formation and ordering of self-assembled Si islands by ultrahigh vacuum annealing of ultrathin bonded silicon-on-insulator structure*. Applied Surface Science, 2000. **159–160**: p. 121-126.
33. Barimar, P.S.N., et al., *Study of the effect of thermal treatment on morphology and chemical composition of silicon-on-insulator*. Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena, 2016. **34**(4): p. 041806.
34. Becker, R.S., J.A. Golovchenko, and B.S. Swartzentruber, *Electron Interferometry at Crystal Surfaces*. Physical Review Letters, 1985. **55**(9): p. 987-990.
35. Binnig, G., et al., *Tunneling Spectroscopy and Inverse Photoemission: Image and Field States*. Physical Review Letters, 1985. **55**(9): p. 991-994.
36. Ibe, J.P., et al., *On the electrochemical etching of tips for scanning tunneling microscopy*. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 1990. **8**(4): p. 3570-3575.
37. Naydenov, B. and J.J. Boland, *Variable-height scanning tunneling spectroscopy for local density of states recovery based on the one-dimensional WKB approximation*. Physical Review B, 2010. **82**(24): p. 245411.
38. Hubbard, A.T., *The Handbook of Surface Imaging and Visualization*.
39. Woodruff, D.P.a.D., T.A., *Modern Techniques of Surface Science*. 1994, Cambridge: Cambridge University Press.

40. Moulder, J.F. and J. Chastain, *Handbook of X-ray Photoelectron Spectroscopy: A Reference Book of Standard Spectra for Identification and Interpretation of XPS Data*. 1992: Physical Electronics Division, Perkin-Elmer Corporation.
41. Giessibl, F.J., *AFM's path to atomic resolution*. *Materials Today*, 2005. **8**(5): p. 32-41.
42. Frederix, P.L.T.M., P.D. Bosshart, and A. Engel, *Atomic Force Microscopy of Biological Membranes*. *Biophysical Journal*, 2009. **96**(2): p. 329-338.
43. Vinckier, A. and G. Semenza, *Measuring elasticity of biological materials by atomic force microscopy*. *FEBS Letters*, 1998. **430**(1-2): p. 12-16.
44. Tranchida, D., et al., *Nanoscale mechanical characterization of polymers by atomic force microscopy (AFM) nanoindentations: viscoelastic characterization of a model material*. *Measurement Science and Technology*, 2009. **20**(9): p. 095702.
45. Gross, L., et al., *The Chemical Structure of a Molecule Resolved by Atomic Force Microscopy*. *Science*, 2009. **325**(5944): p. 1110-1114.
46. Mohn, F., et al., *Reversible Bond Formation in a Gold-Atom\char21{}Organic-Molecule Complex as a Molecular Switch*. *Physical Review Letters*, 2010. **105**(26): p. 266102.
47. Zhang, J., et al., *Real-Space Identification of Intermolecular Bonding with Atomic Force Microscopy*. *Science*, 2013.
48. de Oteyza, D.G., et al., *Direct Imaging of Covalent Bond Structure in Single-Molecule Chemical Reactions*. *Science*, 2013. **340**(6139): p. 1434-1437.
49. Riss, A., et al., *Local Electronic and Chemical Structure of Oligo-acetylene Derivatives Formed Through Radical Cyclizations at a Surface*. *Nano Letters*, 2014. **14**(5): p. 2251-2255.
50. Magonov, S.N., V. Elings, and M.H. Whangbo, *Phase imaging and stiffness in tapping-mode atomic force microscopy*. *Surface Science*, 1997. **375**(2): p. L385-L391.
51. Makky, A., et al., *Piezoelectric tuning fork probe for atomic force microscopy imaging and specific recognition force spectroscopy of an enzyme and its ligand*. *Journal of Molecular Recognition*, 2013. **26**(11): p. 521-531.

52. Anczykowski, B., D. Krüger, and H. Fuchs, *Cantilever dynamics in quasinoncontact force microscopy: Spectroscopic aspects*. Physical Review B, 1996. **53**(23): p. 15485-15488.
53. Winkler, R.G., et al., *Imaging material properties by resonant tapping-force microscopy: A model investigation*. Physical Review B, 1996. **54**(12): p. 8908-8912.
54. Tamayo, J. and R. García, *Effects of elastic and inelastic interactions on phase contrast images in tapping-mode scanning force microscopy*. Applied Physics Letters, 1997. **71**(16): p. 2394-2396.
55. Ahn, H.S., et al., *Application of phase contrast imaging atomic force microscopy to tribofilms on DLC coatings*. Wear, 2001. **249**(7): p. 617-625.
56. Nonnenmacher, M., M.P. O'Boyle, and H.K. Wickramasinghe, *Kelvin probe force microscopy*. Applied Physics Letters, 1991. **58**(25): p. 2921-2923.
57. Zhang, Z., et al., *Cross sections of operating Cu(In,Ga)Se₂ thin-film solar cells under defined white light illumination analyzed by Kelvin probe force microscopy*. Applied Physics Letters, 2013. **102**(2): p. 023903.
58. Hoppe, H., et al., *Kelvin Probe Force Microscopy Study on Conjugated Polymer/Fullerene Bulk Heterojunction Organic Solar Cells*. Nano Letters, 2005. **5**(2): p. 269-274.
59. Hallam, T., et al., *A scanning Kelvin probe study of charge trapping in zone-cast pentacene thin film transistors*. Nanotechnology, 2009. **20**(2): p. 025203.
60. Liu, L. and G. Li, *Electrical characterization of single-walled carbon nanotubes in organic solar cells by Kelvin probe force microscopy*. Applied Physics Letters, 2010. **96**(8): p. 083302.
61. Clack, N.G., K. Salaita, and J.T. Groves, *Electrostatic readout of DNA microarrays with charged microspheres*. Nat Biotech, 2008. **26**(7): p. 825-830.
62. Finot, E., et al., *Effect of Cholesterol on Electrostatics in Lipid-Protein Films of a Pulmonary Surfactant*. Langmuir, 2010. **26**(3): p. 1929-1935.
63. Zisman, W.A., *A NEW METHOD OF MEASURING CONTACT POTENTIAL DIFFERENCES IN METALS*. Review of Scientific Instruments, 1932. **3**(7): p. 367-370.

- 64.Oatley, C.W., *The early history of the scanning electron microscope*. Journal of Applied Physics, 1982. **53**(2): p. R1-R13.
- 65.Woollam, J.A., et al. *Overview of variable-angle spectroscopic ellipsometry (VASE): I. Basic theory and typical applications*. in *Optical Metrology*. 1999.

3

THERMAL TREATMENT OF SILICON-ON-INSULATOR

A freshly formed silicon surface is highly reactive and therefore the surface is immediately covered with a thin layer of oxide known as native oxide on exposure to atmosphere. Surface analysis of silicon samples in STM requires removal of the native oxide before the measurements. Removing the thin native oxide layer from silicon in an UHV environment involves annealing the samples at extremely high temperatures. Processing SOI at elevated temperature without damaging the device layer is a significant challenge. Changing chemical composition on the surface and loss of integrity of the device layer during the high temperature annealing are major issues. In order to address these challenges, a low thermal budget process was developed and the thermal decomposition of the native oxide in UHV was investigated using SEM, AFM, STM and XPS analysis. The evolving morphology and chemical composition of the native oxide and the SOI device layer were investigated as a function of anneal temperature and duration. An elaborate *ex-situ* cleaning process was developed to both reduce the contamination and cap the surface with a chemically grown ultra-thin oxide. An effective annealing process that desorbs oxide without disturbing the integrity of device layer was subsequently optimised. The *ex-situ* and the *in-situ* processing parameters and the results of their surface analysis are discussed in detail in this chapter.

3.1 Introduction

In situ preparation of Si samples in UHV is usually accomplished via thermal annealing at high temperature. This process removes the native oxide from the sample, resulting in an atomically clean surface [2-8]. At high temperatures Si adatoms are created which then diffuse on the surface and react with SiO₂ to produce SiO via the equation [10, 11]



The silicon monoxide then sublimates from the surface [12]. While the oxide can easily be desorbed from the surface of bulk silicon, there are several challenges involved in doing the same from an SOI surface. There are additional challenges associated with lower SOI thicknesses and engineered SOI surfaces.

Thin films are susceptible to a phenomenon known as “dewetting,” whereby the film agglomerates into small islands in order to minimize surface energy, exposing the underlying low surface energy layer [13-20]. Once the native oxide has been removed from the SOI, the Si device layer becomes mechanically unstable and exhibits dewetting behaviour on annealing, peeling back to uncover the BOX [21, 22]. The recognized procedure for *in-situ* cleaning of bulk Si in UHV involves heating samples to temperatures of approximately 1200 °C [23]. These thermal conditions are extreme in the case of SOI and therefore a low thermal budget process of removing the oxide from SOI is essential in order to avoid dewetting of the device layer [24, 25].

In this chapter, oxide desorption from the Si(100) SOI device layer and the challenges involved in doing so have been discussed in detail. During the course of this work, low thermal budget processes were investigated in order to facilitate oxide removal while avoiding dewetting of the device layer. The effects of annealing of SOI in UHV at varying temperatures, for different durations and the resultant oxide desorption and surface morphology were studied using SEM, AFM, STM, and angle-dependent XPS measurements. Pre-anneal cleaning steps were also investigated, with the aim of reducing the amount of carbides present on annealed SOI samples. The pre-anneal cleaning conditions and UHV annealing

parameters developed and optimised for ultra-thin SOI down to 5 nm thickness are presented in this chapter.

3.2 Experimental details

All thermal process optimizations were carried out in the custom-built UHV chamber described in section 3.3. The optimised conditions were then used for experimental work carried out in the STM preparation chamber. The base pressure of all the vacuum systems used in this work was better than 1×10^{-10} mbar. Highly doped n-type SOI with phosphorous concentration of 10^{19} cm^{-3} , with an initial Si(100) device layer thickness of 50 nm and 12 nm were studied. While the native oxide thickness was around 2 nm, the buried oxide (BOX) thickness was 130 nm in case of the 50 nm SOI and 25 nm in case of the 12 nm SOI. Samples were cut into a standard size of 11 mm $\times$ 4 mm using a diamond wafer cutting tool.

Techniques such as direct resistive heating and indirect heating on a button heater were used for the thermal treatment. Sample temperature for both direct and indirect heating system were measured with a thermocouple and a Resistance Temperature Detector (RTD) for a standard sample, where the heating power and temperature relationship was calibrated. Labview annealing software was developed to control the heating current, power and time. The software enabled reproducibility in the ramp rate and anneal time thus ensuring consistency in the annealing results. The temperature ramp rate for the thermal treatment was fixed for all experiments while the annealing power and hold time were varied. For certain experiments, the experimental setup was designed such that a thermal gradient of $\sim 50 \text{ }^{\circ}\text{C}$ was present along the sample during annealing. The gradient measurements were carried out on a direct resistive heating set-up, with the gradient created by increased dissipation on one side of the sample. Multiple anneal cycles were adopted for some thermal treatments in order to avoid dewetting.

An Oxford Instruments ICP-100 plasma system was used for plasma cleaning and thinning of SOI. Several different plasma recipes were used to thin the device layer thickness. A feed gas mixture of SF_6 and CHF_3 were used in the fluorine based plasma etching recipes and pure oxygen was used in the oxygen

plasma etch recipes. Post-anneal characterization such as surface morphology was investigated using a Zeiss SEM system and a Bruker AFM system, while chemical analysis of the surface was carried out in a VG scientific ESCALab XPS system. All AFM measurements were performed in tapping mode with Silicon AFM tips acquired from BudgetSensors. Stiffer tip cantilever with resonance frequency of approximately 300 kHz were used for phase analysis measurements to lower the influence of tip-surface adhesion.

Ex situ XPS measurements were carried out in a UHV chamber with a base pressure lower than 1×10^{-9} mbar. Turnaround time between removal of samples from the UHV chamber following annealing and their introduction into the XPS chamber was approximately 20 min. An aluminium anode with $K_{\alpha} = 1486.7$ eV was used as the x-ray source. The measurements were carried out at three different angles, corresponding to near-normal and grazing incidence with respect to the analyser, as well as an angle of intermediate incidence. STM measurements were also carried out to analyse the surface quality of SOI after it had undergone the *ex situ* cleaning and *in situ* thermal processes.

3.3 Test chamber

In order to carry out the optimization study, a customized UHV chamber

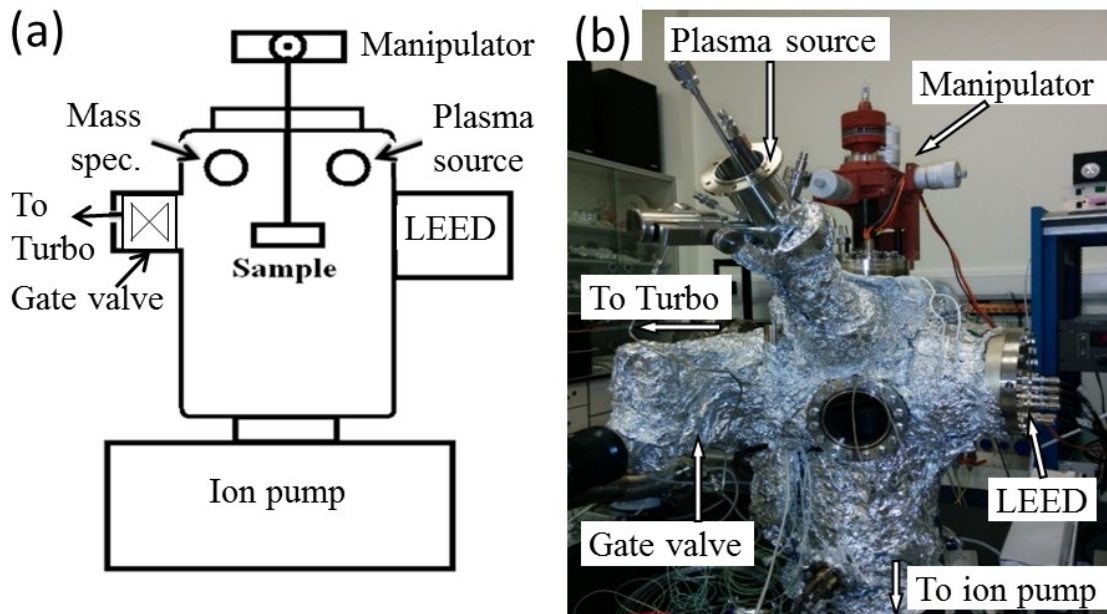


Fig. 3.1: Schematic (a) and an image (b) of the standalone UHV chamber demonstrating different parts.

was built. Fig. 3.1 (a) and 3.1(b) shows the schematic and image of the chamber, detailing different parts of the system. The UHV system is made up of a single chamber with a turbo molecular pump, ion pump and TSP. The chamber had a gate valve that could isolate the chamber from the turbo molecular pump. The base pressure of the chamber was lower than 1×10^{-10} mbar. The chamber comprised of a manipulator that could process four samples through direct current heating, a LEED system, a mass spectrometer and a plasma source. The chamber also had a cold finger that could cool the manipulator down to approximately 180 K. Following thermal processing, the samples were analysed *in situ* with LEED. Successful desorption of oxide from the sample surface was confirmed with a 2×1 LEED pattern. Samples were then analysed *ex situ* with SEM, AFM and XPS.

3.4 Chemical etching of oxide

A simple approach to remove the native oxide on silicon is etching the oxide in dil. HF. This process leaves the silicon surface passivated with hydrogen. The passivated hydrogen can then be desorbed in UHV from Si surface at around 530°C [26-28].

Oxide capping on SOI samples were etched with HF treatment and rinsed in DI water. The samples were loaded into the UHV load-lock within 20 – 30 mins following the HF treatment. A good 2×1 LEED pattern was observed following annealing, however, the surface showed presence of narrow protrusions. Fig. 3.2(a) and 3.2(b) shows STM images, with different magnifications, of the surface of SOI following flash annealing at round 700 °C to desorb all hydrogen. The STM images were recorded with 7 V bias and 5 pA current setpoint. The STM images clearly showed several protrusions with flat regions between them. Fig. 3.2(c) shows the tunnelling spectra recorded from a protrusion (black) and the flat region between the protrusions (grey). The band gap of protrusions were around 2 eV, which was similar to the band gap reported in the literature for SiC [29-32]. However, the region between protrusions were silicon. The SiC contamination was probably due to the reaction of hydrocarbons with the hydrogen passivated surface and the residual dangling bonds of Si dimers [33-38] while the sample was exposed to the atmosphere during the sample transfer into UHV following HF etching.

Several attempts were made to produce a clean surface from a H-passivated surface, however, the surface contamination could not be avoided. Furthermore, the hydrogen passivated silicon surface also oxidised within short time of exposure to atmospheric air [39]. Therefore, H-passivation of SOI prior to UHV flash annealing was found to be an unsuitable approach to obtain a clean and oxide free SOI surface or even to lower the processing thermal budget.

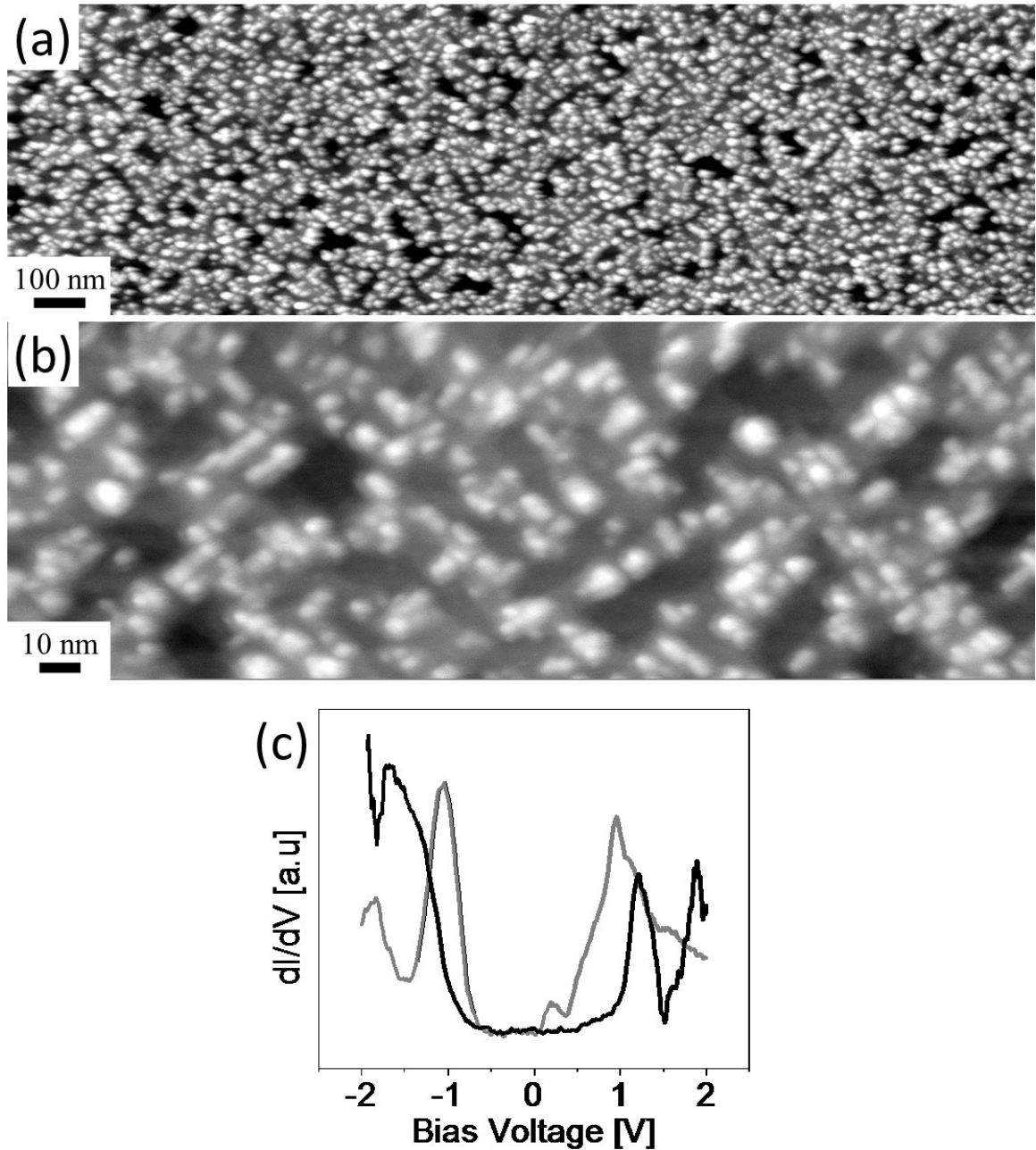


Fig. 3.2: H-passivated 12 nm SOI surface after flash annealing at 700 °C. (a) and (b) shows the STM image with different magnification. (c) shows the tunneling spectra recorded from the protrusions (black) and the region between the protrusions (grey). The STS data suggests that the protrusions are probably carbides and the region between is silicon.

3.5 Thermal desorption of oxide layer

The native oxide layer on the silicon surface can be desorbed by annealing the sample at temperatures above 800 °C for a short duration depending on the thickness of the oxide layer. This process is known as flash annealing or flashing. The desorption mechanism of native oxide on silicon is widely accepted to be a four step process [7, 40, 41]. At first, voids or oxide free regions (OFR) are formed on the oxide film exposing the silicon underneath, subsequently producing silicon monomers on the OFR surface. Secondly, silicon monomers diffuse and migrate towards the reaction site which is the Si-oxide interface at the perimeter of the OFR. After reaching the Si-oxide interface, adatoms react to form Si-rich oxide and finally volatile SiO is formed. Creation of the voids on the oxide film is a spatially

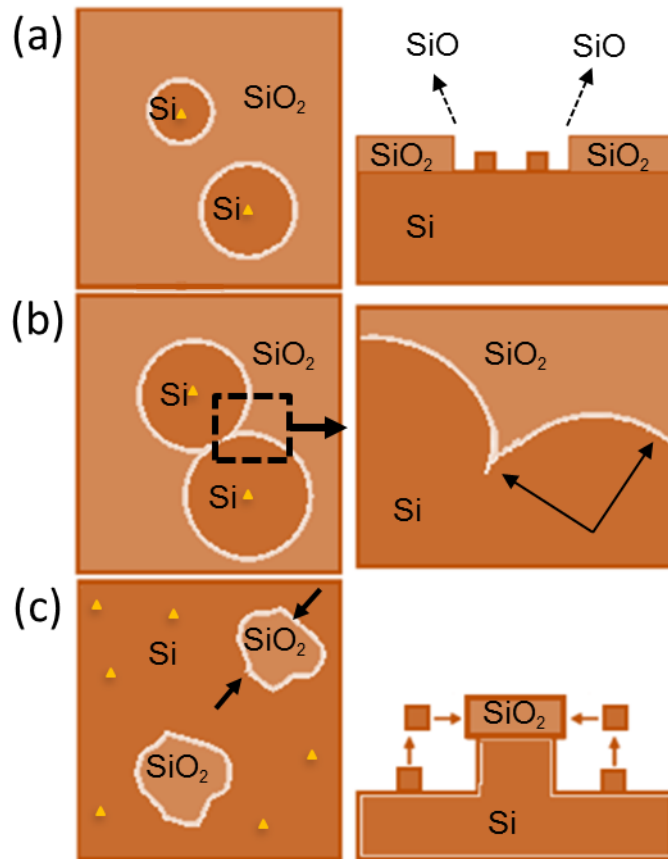


Fig. 3.3: Schematic of the stages of thermal desorption. (a) The initial stage where voids are formed and grow. (b) The middle stage where the voids merge and form irregular reaction fronts, indicated by the arrows in the panel on the right. (c) The final stage where only oxide islands are left. The panel on the right depicts the increased vertical distance from the silicon surface to the oxide (image from Xue et. al. [1]).

inhomogeneous process. Voids are believed to nucleate at defects in the oxide [1, 42]. Void growth and propagation largely depends on factors such as the anneal temperature [2, 40, 43], surface contamination [44, 45], oxide formation methods [46, 47] and oxide interface quality [48]. Growth of voids and thermal decomposition of the oxide is demonstrated in Fig. 3.3. Once a void is created (see

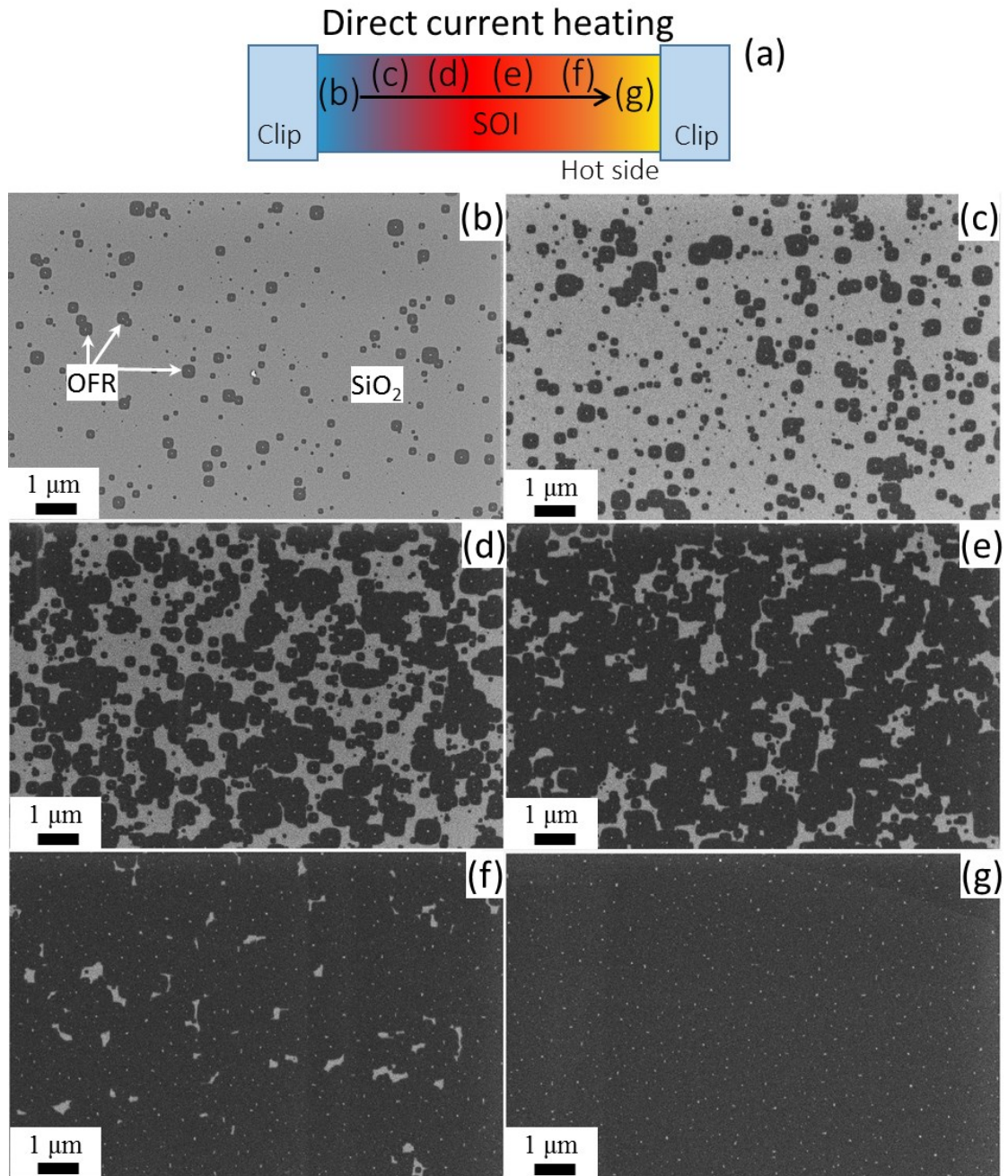


Fig. 3.4: SEM images showing six different regions along the centre of a 50 nm SOI samples after annealing at 750 °C, ten cycles of 60 s duration each. (a) shows the approximate location where each image (b) to (g) was recorded [9].

Fig. 3.3(a)), reaction continues at the silicon-oxide interface at the edges of the OFR and hence the void increases in size. This further leads to the overlapping of OFRs as shown in Fig. 3.3(b). During this process silicon adatoms which are formed at the edges of the atomic steps are consumed by the reaction layer by layer. Eventually, as shown in Fig. 3.3(c), the reaction reaches a stage where only islands of oxide are left. When two adjacent voids overlap and continue to grow, a vertical height of several angstrom ($\sim 12 \text{ \AA}$) may be present between the silicon surface and the oxide island trapped atop a Si pillar [1]. This increases the activation energy of the reaction. Annealing at further higher temperature results in desorption of all oxide exposing atomically clean Si underneath [12].

The experimental set up to optimise the thermal processing was designed such that a temperature gradient of $\sim 50 \text{ }^\circ\text{C}$ was maintained along the sample during annealing. The temperature gradient allowed the study of different stages of oxide desorption on a single sample [12]. Fig. 3.4 shows SEM data recorded at different points along a single SOI sample following ten anneal cycles at $750 \text{ }^\circ\text{C}$, each of 60 seconds duration. The temperature of $750 \text{ }^\circ\text{C}$ was measured at the centre of the sample. The six images, labelled (b) – (g), were recorded along the middle of the sample, moving from the lower temperature end to the higher temperature end, as indicated in the schematic shown in Fig. 3.4(a). The first stage of the oxide desorption process can be seen in Fig. 3.4(b). Here the lighter grey colour signifies areas of native oxide, while the darker areas are OFRs [1, 10, 11].

Fig. 3.4(c) was recorded from an area whose temperature was slightly higher than that shown in Fig. 3.4(b). There are a greater number of OFRs seen in Fig. 3.4(c) and also the average size of the OFRs is comparatively larger, indicating that both the number and the size of voids increase with annealing temperature. The OFR size distribution in Fig. 3.4(c) indicates that OFR nucleation continues throughout the duration of the anneal [1, 2].

The density and size of OFRs also continues to increase with the temperature. Fig. 3.4(d) and 4(e) shows the progression of the oxide desorption. As the size and number increases the OFRs start to overlap and coalesce. In Fig. 3.4(e), oxide is desorbed from more than 50% of the visible surface area, leaving

only some irregularly shaped oxide islands trapped atop silicon pillars between adjacent voids, as shown in Fig. 3.3(c). These oxide islands decrease in size as the oxide desorption continues (Fig. 3.4(f)).

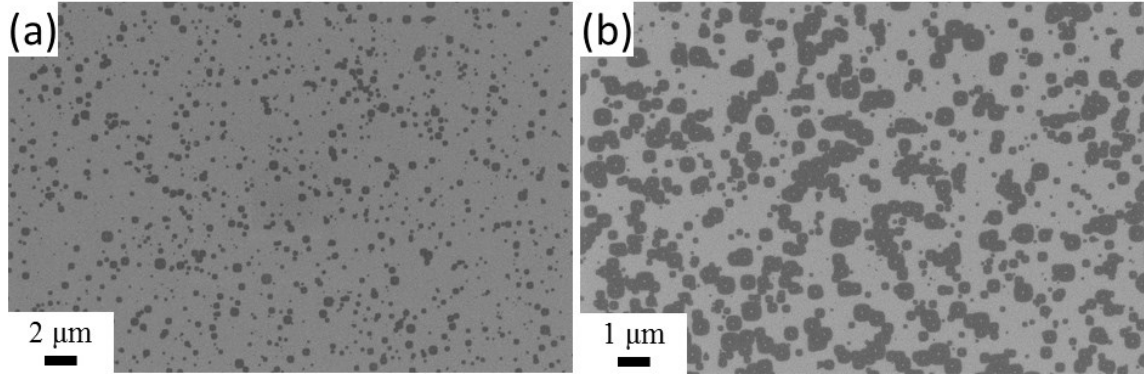


Fig. 3.5: SEM images of a 50 nm SOI sample after ten anneal cycles at 750 °C, each lasting 30 s. (a) A region near the centre of the sample, and (b) a region near the end of the sample that reached the highest temperature[9].

On the hotter end of the sample (Fig. 3.4(g)) oxide has been completely desorbed, leaving behind small protrusions. The protrusions can also be seen in previous cases in Fig. 3.4(b) to 3.4(g). These protrusions have been shown clearly in a magnified SEM image of a different sample in Fig. 3.6(b). Two alternating explanations for these protrusions are available in the literature. One proposal is that they are the SiC islands that acted as nucleation sites for the OFRs [1, 29], while the second is that they are remaining oxide islands that developed as neighbouring voids connected. The latter explanation follows on from the observation that the OFRs become deeper as well as wider as they expand [1, 40, 41]. When voids merge, the oxide trapped on top of a Si pillar, as shown in Fig 3.2(c), the increased separation between the oxide and silicon monomers creates for a barrier to silicon monomers from the base of the void to react with the oxide and form SiO. In order to determine the nature of these protrusions, and to study their origin, a detailed chemical, mechanical and electron LDOS analysis was carried out with XPS, AFM and STS characterization. Results of these characterizations are discussed in a following section.

In order to investigate the relationship between anneal duration and anneal temperature, samples were annealed at different temperatures for varying lengths of time. Fig. 3.5 shows SEM images recorded from a sample that was subjected to ten anneal cycles at 750 °C, each lasting for 30 s. Fig. 3.5(a) shows an area near the centre of the sample, while Fig. 3.5(b) shows an area from the end of the sample which reached the highest temperature during the anneal. The effect of temperature gradient across the sample can be observed. Barely any oxide has desorbed at the low temperature side while desorption is at an early stage in the centre shown in Fig. 3.5(a). Even at the hottest end of this sample (Fig. 3.5(b)), desorption is at a comparatively early stage, with a high density of OFRs and some examples of OFRs coalescence with their neighbours. Nowhere on the sample is the oxide completely desorbed, as is seen in Fig. 3.4(g). Hence, the anneal duration is a significant factor, as ten 30 s anneal cycles at 750 °C are not sufficient to fully desorb the oxide anywhere Fig. 3.6 shows SEM images recorded from a sample after ten cycles of annealing at 750 °C for 90 s. Fig. 3.6(a) and 3.6(b) show regions close to the centre of the sample, but are representative of the entire surface. The thermal gradient effect is no longer significant at this anneal condition as oxide has been desorbed at every point of the sample. Fig. 3.6(b) was recorded at higher magnification which clearly shows the irregular and approximately linear shaped protrusions. It is clear that ten 90 s anneal cycles at 750 °C are sufficient for the oxide desorption to progress to completion.

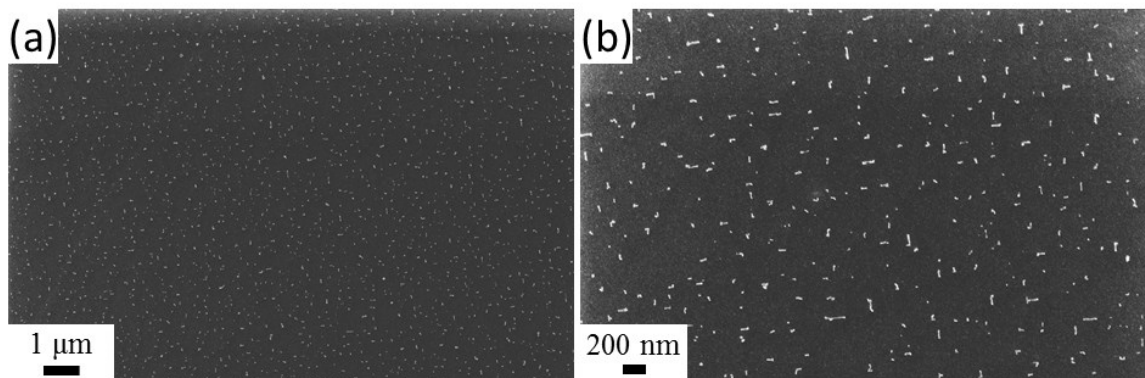


Fig. 3.6: SEM images of a 50 nm SOI after ten cycles of annealing at 750 °C, each for a duration of 90 s. (a) and (b) regions near the centre of the sample. (b) also shows the protrusions on the SOI surface following annealing.

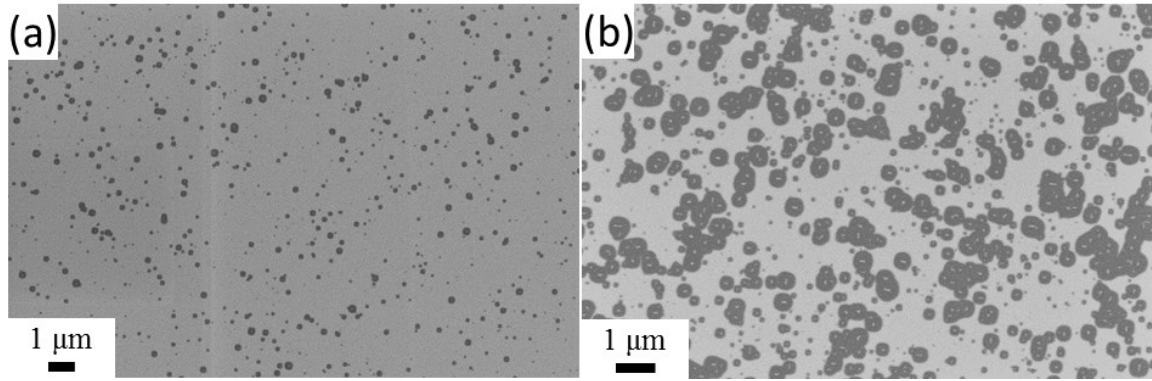


Fig. 3.7: SEM data for a 50 nm SOI sample annealed at 690 °C for 60 min. (a) A region near the centre of the sample, (b) Area at the end of the sample that reached the highest temperature [9].

In order to study the effects of longer duration anneals at lower temperature on desorption of the oxide layer, a sample was annealed at 690 °C continuously for 1 hour (Fig. 3.7). The temperature gradient still plays a significant role, especially for this longer anneal. At the lower temperature side of the sample, no oxide is desorbed. At the centre, shown in Fig. 3.7(a), OFs have nucleated and started to grow, but are still at a very early stage in the desorption process. The oxide desorption has progressed further along at the end of the sample exposed to higher temperature, shown in Fig. 3.7(b), but are still at quite an early stage. Hence, the anneal temperature is very important. If the temperature is not sufficiently high, desorption is not effective even after annealing for long durations.

3.6 Surface compositional analysis after annealing

3.6.1 X-ray photoelectron spectroscopy

Angle-dependent X-ray photoelectron spectroscopy was employed to study the SOI surface composition before and after flash annealing. Si 2p core level spectra were recorded at multiple angles to study the various oxidation states of silicon. Fig. 3.8 shows the Si 2p XPS data for pristine (Fig. 3.8(a)) and a sample flashed twice at 900 °C for 10 s (Fig. 3.8(b)). The spectra are recorded at 10° (near-normal incidence), 40° (intermediate incidence) and 70° (grazing incidence) with respect to the analyser to obtain surface sensitive measurements. The main feature in the spectrum recorded at 10° for the pristine sample (Fig. 3.8(a)) is fitted with a Voigt doublet at a $2p_{3/2}$ binding energy of 99.7 ± 0.1 eV, with a spin-orbit splitting

of 0.6 eV [49, 50]. Another major component of the spectrum at a binding energy of 103.9 ± 0.1 eV is fitted with a Voigt lineshape and is assigned to Si in the +4 oxidation state, i.e., in the SiO_2 chemical environment [49, 51]. Voigt lineshapes with binding energies of 100.7 ± 0.1 eV, 101.5 ± 0.1 eV, and 102.9 ± 0.1 eV are assigned to Si in the +1, +2, and +3 oxidation states corresponding to the Si_2O , SiO and Si_2O_3 suboxides respectively [49, 51, 52]. However, the contributions from Si^{2+} and Si^{3+} are negligible at near-normal incidence. The contributions from Si in the +1, +2 and +3 oxidation states increases comparatively as the angle between the surface normal and the analyser increases to 40° (Fig. 3.8(a)). The overall signal in the Si 2p region however decreases dramatically as the measurement angle moves from near-normal to grazing incidence, i.e., as the surface sensitivity increases. The data recorded at higher angles have lower signal-to-noise ratio compared to the data measured at 10° and therefore the 40° and 70° data have been multiplied by a factor of 10 to display all the spectra on one scale as noted in Fig. 3.8(a). This indicates the presence of a thick layer of oxide on the surface of the pristine sample, which has the effect of attenuating the Si 2p signal as the measurement becomes increasingly surface sensitive. In addition, contribution from +1, +2, +3 and +4 oxidation states account for over half (62%) of the total intensity of the spectra measured at 40° and 70° , confirming the presence of a thick oxide layer.

In case of the flashed sample (Fig. 3.8(b)), the Si 2p signal is dominated by the doublet with $2p_{3/2}$ binding energy of 99.8 ± 0.1 eV and a spin-orbit splitting at 0.6 eV [49-51]. The contribution from Si in oxidation states related to silicon suboxides (Si_2O , SiO and Si_2O_3) are negligible at all angles. However, there is a significant contribution from the Si in the +4 oxidation state, assigned to the SiO_2 chemical environment [49-51], at higher angles of incidence. In addition, the signal measured from the flashed sample at 40° does not show the marked attenuation of intensity observed for the analogous spectrum recorded from pristine sample. However, there is an attenuation of the Si 2p signal for grazing incidence, requiring the data to be multiplied by a factor of 7 in order to display all three spectra on one scale. This indicates the presence of a very thin oxide layer

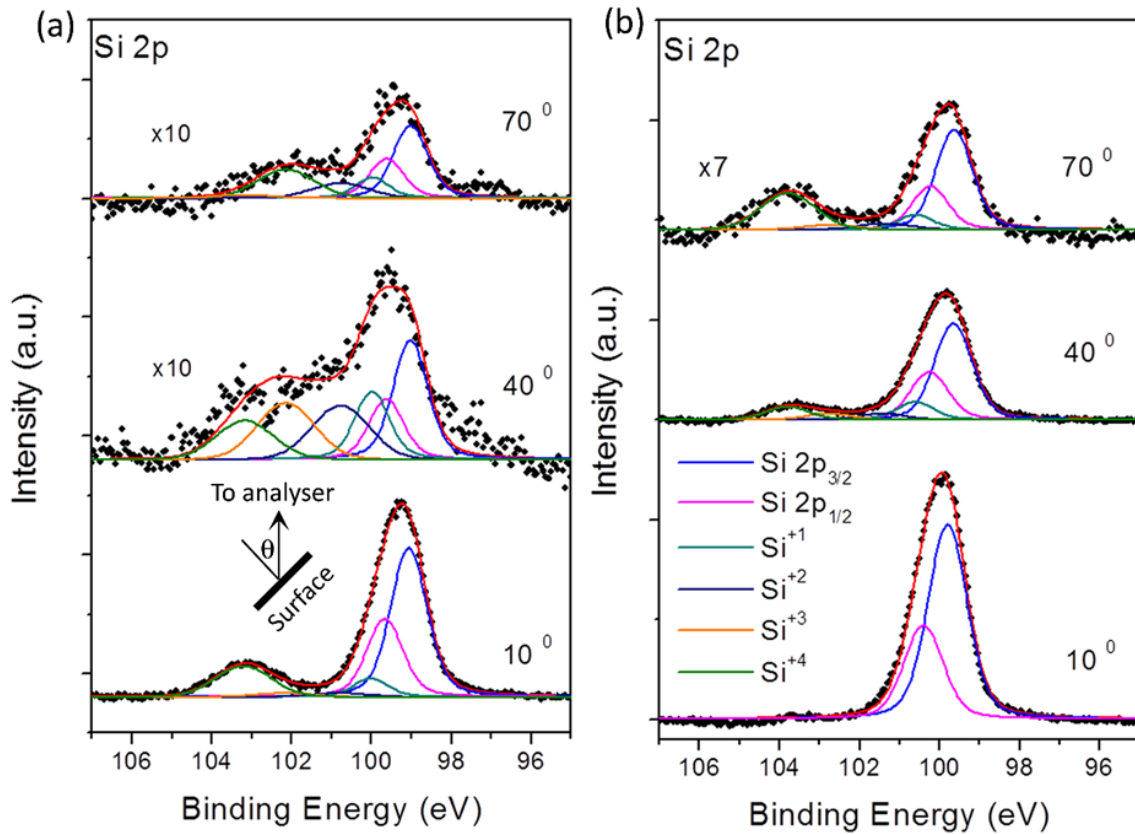


Fig. 3.8: XPS measurements showing the Si 2p core level for (a) pristine and (b) flashed (two anneal cycles at 900°C for 10 s) SOI recorded at different angles of incidence (see inset). Components fitted as follows: Si $2p_{3/2}$ (blue), Si $2p_{1/2}$ (magenta), Si^{+1} (dark cyan), Si^{+2} (navy), Si^{+3} (orange), and Si^{+4} (olive). Inset in (a) shows measurement angle θ with respect to analyser and surface normal [9].

on the surface. This thin layer of oxide is most likely formed during the process of transferring the sample from the preparation chamber to the XPS chamber. The growth of a thin oxide layer on the sample surface is likely unavoidable in the case of *ex situ* XPS measurements, even taking into account the short turnaround time of 20 min.

In order to elucidate the character of the structures observed on the SOI surface (Figs. 3.4-3.6) following the flash annealing, angle-dependent XPS data were also recorded for the C 1s region. A weak C 1s signal is observed for measurements recorded from a pristine sample at normal incidence (Fig. 3.9(a)). The spectrum is fitted with two Voigt line-shapes at binding energies of 284.2 ± 0.1 eV and 285.2 ± 0.1 eV, assigned to C-Si and C-C respectively [53-55]. The

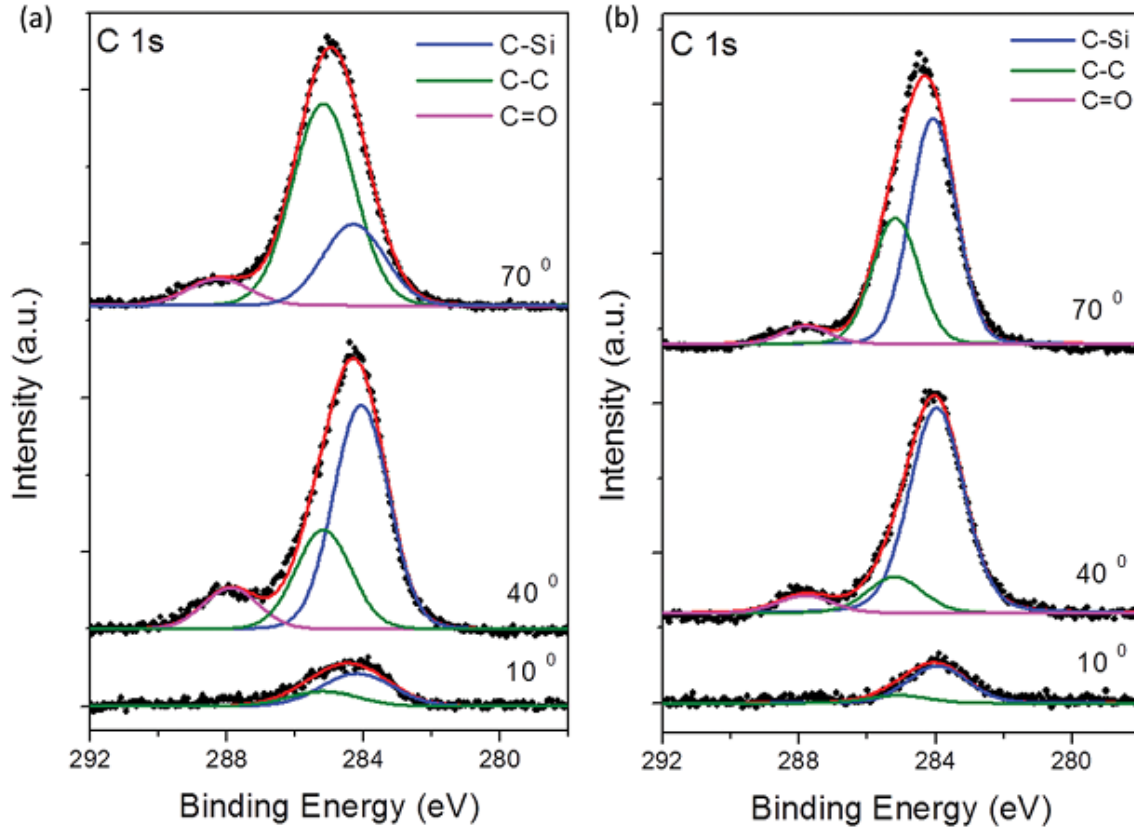


Fig. 3.9: XPS measurements showing the C 1s core level for (a) pristine and (b) flashed (two anneal cycles at 900 °C for 10 s) recorded at different angles of incidence. Components fitted as follows: C-Si (blue), C-C (olive), and C=O (magenta) [9]. The angle of incidence follow the inset shown in Fig. 7 (a).

overall signal intensity increases as the measurement angle moves from near-normal to grazing incidence, i.e., as the surface sensitivity increases. Also, a third feature with a binding energy of 287.9 ± 0.1 eV, which is assigned to C=O [56], is observed. For the spectrum recorded at 40°, the main contribution comes from C-Si, which accounts for 62% of the overall C 1s signal, compared to 27% for C-C. However, the inverse relationship is observed in the spectrum measured at 70°, with C-C contribution accounting for 65% of the total signal compared to 26% for C-Si (Fig. 3.9(a)). This indicates that for the pristine sample, while a proportion of carbon is interacting with silicon, carbon bonding exclusively with other carbon atoms is the dominant species.

XPS data for the C 1s region recorded after flash annealing the sample (Fig. 3.9(b)) is significantly different to the data obtained from the pristine sample. The

corresponding peaks in the Si2p is shown in Fig. 3.8(b). The total C 1s signal intensity recorded from the flashed sample is comparable to that measured for the pristine sample (Fig. 3.9(a)), indicating that sample processing has not resulted in significant carbon contamination. Also, for the flashed sample the contribution from C-Si is the main component at each measurement angle (Fig. 3.9(b)), which is in contrast to the spectra measured from the pristine sample (Fig. 3.9(a)). At measurement angles of 40° and 70° for the flashed sample, the C-Si contribution accounts for 79% and 61% respectively of the total signal. Hence, even at maximum surface sensitivity the majority of the carbon present is interacting with silicon. This indicates that the total amount of carbon present is not significantly altered by the annealing process; however, thermal treatment does alter the chemical interaction of carbon with silicon. While this XPS data does not preclude the protrusions observed at the centre of OFRs from being oxide islands, it is evident that SiC is present on the surface following flash annealing. This also supports the conjecture that the protrusions are SiC islands [29].

3.6.2 AFM phase analysis

Atomic force microscopy in tapping mode was adopted to investigate the nature of the surface features observed on the SOI device layer following the flash annealing process. AFM allows the qualitative study of inhomogeneity on the sample surface with high spatial resolution. Tapping mode AFM can measure ultra-low forces with high spatial resolution without significant influence on the tip-sample interaction from tip-sample contact adhesion and possible capillary effects by the adsorbed water layers. Tip-surface adhesion can be further reduced by the use of a stiff AFM cantilever tip, and resulting phase contrast images are highly sensitive to the relative variation in local stiffness of the sample. In addition, a stiff cantilever tip is minimally influenced by the tip-sample adhesion and therefore the phase shift observed is predominantly influenced by the elastic modulus of the inhomogeneity in the sample surface [57]. The nature of the inhomogeneity, such as chemical composition, can be explained quantitatively with the help of additional information supplied by other analysis [57]. AFM phase contrast imaging is used in this work to probe and identify the relative variation in the

stiffness of the protrusions and other features on the SOI surface with respect to the silicon device layer, following the flash annealing.

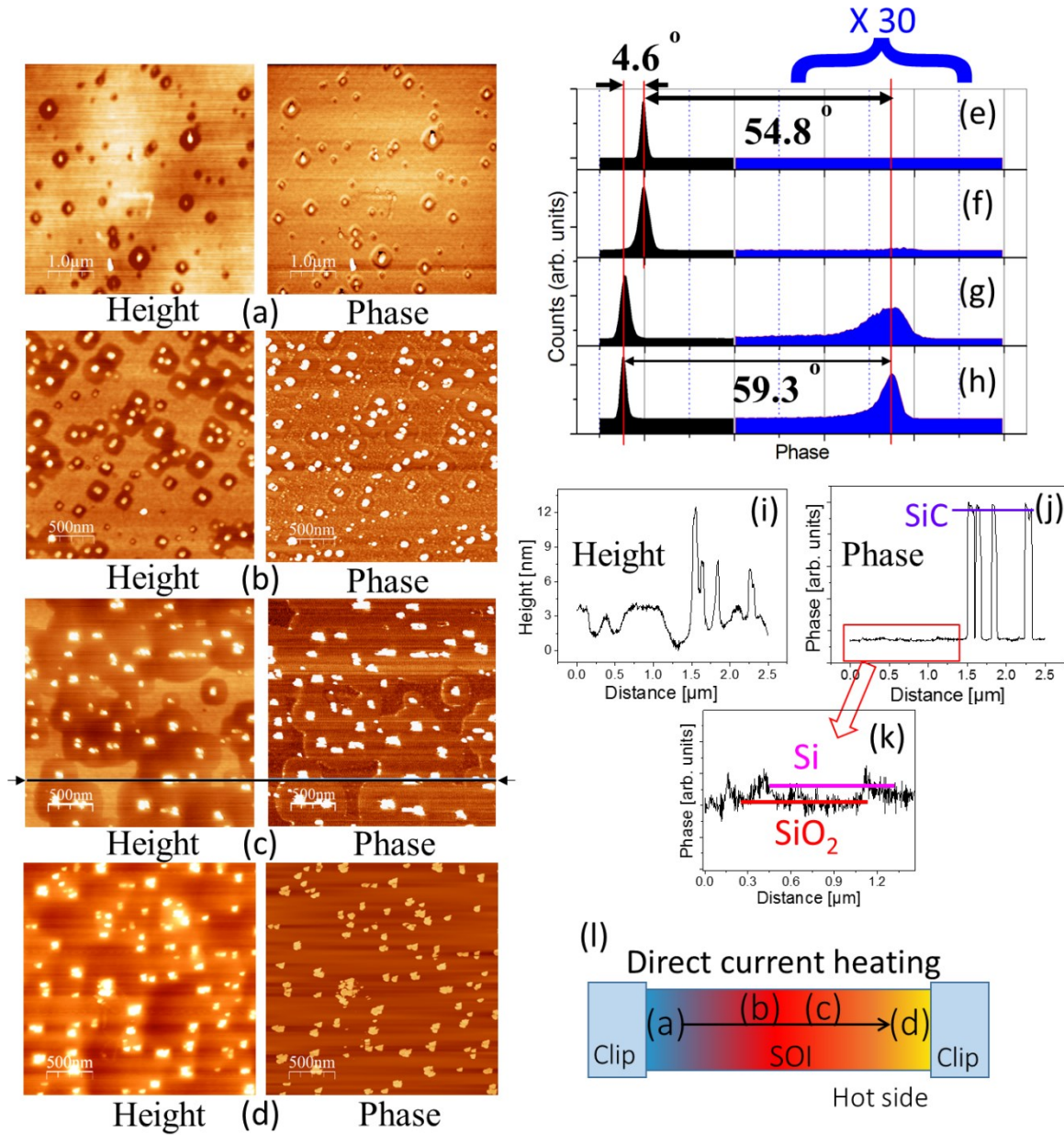


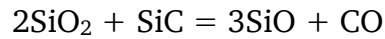
Fig. 3.10: Topography and phase contrast AFM images measured across a 50 nm SOI sample after 10 anneal cycles at 750 °C, each lasting 60 s. Oxide desorption process is captured at different stages (a)–(d) due to a thermal gradient across the sample as indicated by (l). (e) Phase histogram for a surface completely covered with oxide and (f)–(h) phase histogram for (a), (b), and (d), respectively. (i) and (j) Height and phase line profile across the line indicated in (c). (k) The zoom in of the phase profile indicated by the red box [9].

Fig. 3.10(a) – 3.10(d) shows topography and phase contrast images measured across the sample (as depicted in Fig. 3.10(l)) of a 50 nm SOI following annealing at 750 °C for 10 anneal cycles, each lasting 60 s. Similar to the SEM data presented in the section above, various stages of oxide desorption and the distribution of protrusion have been recorded by taking advantage of the thermal gradient across the sample during anneal cycles. A stiff cantilever tip with resonance frequency of ~ 300 kHz was used for all AFM measurements presented in this section.

An early stage of oxide desorption is shown in Fig. 3.10(a), where a small number of OFRs are present on the surface, while Fig. 3.10(d) shows complete desorption of oxide with high density of protrusions. The protrusions are visible in Fig. 3.10(a)-(d), on both height and phase images, at the centre of each OFR. The line profile of the height and phase data obtained across the line shown in Fig. 3.10(c), presented in Fig. 3.10(i) and 3.10(j), clearly shows the a difference in the phase angle between the protrusions and the silicon device layer, while a much smaller phase contrast is observed between the oxide and the silicon itself. The phase histograms presented in Fig. 3.10(e)-(h) show the distribution of phase angle for the phase contrast images. Fig. 3.10(e) is the phase histogram of a sample before annealing, which is completely covered with native oxide and Fig. 3.10(f) - (h) are the histogram data for the phase images in Fig. 3.10(a), 3.10(b) and 3.10(d), respectively. The intensity of the peak on the right, shown in blue, is multiplied 30 times in order to plot it on the same scale as the peak on the left, shown in black. The position of the peak on the left changes as the area of oxide and silicon coverage varies in the images. A phase difference of around 4.6° is observed between Fig. 3.10(e) which corresponds to a sample completely covered with oxide, and Fig. 3.10(h), recorded on the sample with all oxide desorbed, leaving the silicon device layer and a high density of protrusions, as seen in Fig. 3.10 (d). In addition, the intensity of the peaks on the right gradually increases from Fig. 3.10(e) - (h). These observations indicate that the two peaks on the left are the contributions of oxide and silicon while the peak on the right is the contribution from the protrusions. The peak on the right is shifted from the peaks

relating to the oxide and silicon by about 54° - 59° which indicates that the protrusions are comparatively stiffer than the silicon and the oxide islands [57, 58]. These relative stiffness data agree well with the data found in the literature for Si, SiO₂ and SiC [59, 60]. The AFM data, together with the XPS data showing the presence of carbon bonded to Si on the surface of the SOI (Fig. 3.9(b)), supports the hypothesis that these protrusions are SiC.

The location of the SiC protrusions at the centre of each OFR suggests that they may be the nucleation sites for the void formation and decomposition of native oxide [29]. One possible nucleation mechanism is a reaction between carbon impurities on the surface and SiO₂ to form SiC, which can then react with SiO₂ to form volatile SiO, according to the following equations [61-63]:



The volatile SiO desorbs and voids begin to open in the oxide around the SiC protrusion. The voids grow via the process described in sections 3.5 above. It is known from the literature that carbon reacts with silica to form a thin layer of SiC on silicon at temperatures above 650 °C [64-67]. Since the thermal treatment used in this experiment is over 650 °C, carbon contaminants on SOI could result in SiC islands.

3.7 Elimination of surface carbide and STM analysis

The thermal process presented in the section 3.5 desorbs the oxide layer on SOI without the loss of integrity of the device layer. However, the post-processed SOI surface showed numerous SiC protrusions. It is essential to reduce the SiC protrusions before the surface characterization. A high density of SiC protrusions severely hinders STM experiments as the tip can crash into the protrusions at low biases. Therefore, SOI samples were treated *ex situ* with so-called “Piranha” solution, which is a 4:1 concentrated solution of sulfuric acid and hydrogen peroxide [68]. Following Piranha treatment, samples were treated with RCA1 and RCA2 solutions. RCA solutions are 1:1:5 concentration solutions of ammonium hydroxide, hydrogen peroxide, and water (RCA1) and hydrochloric acid, hydrogen peroxide, and water (RCA2) [68]. While these chemical treatments can result in a

clean surface for UHV surface measurements [24], it is essential to maintain high clean-room standards and use ultra-pure electronic grade chemicals during the process. Failing to maintain the highest standards during the cleaning process results in a contaminated [68] and rough Si surface. These restrictions make the cleaning process time-consuming and expensive. A simple yet effective oxygen plasma-based cleaning process was developed during the course of this work to obtain atomically clean and smooth silicon surface. Additionally, the same process was optimised to reliably thin SOI with good precision. Pristine 50 nm SOI samples were exposed to an oxygen plasma in an ICP system for 30 s, followed by a 60 s dip in dilute hydrofluoric acid (HF) and were finally rinsed in water for 30 s. The oxygen plasma oxidizes carbon contaminants and leaves a layer of oxide on the

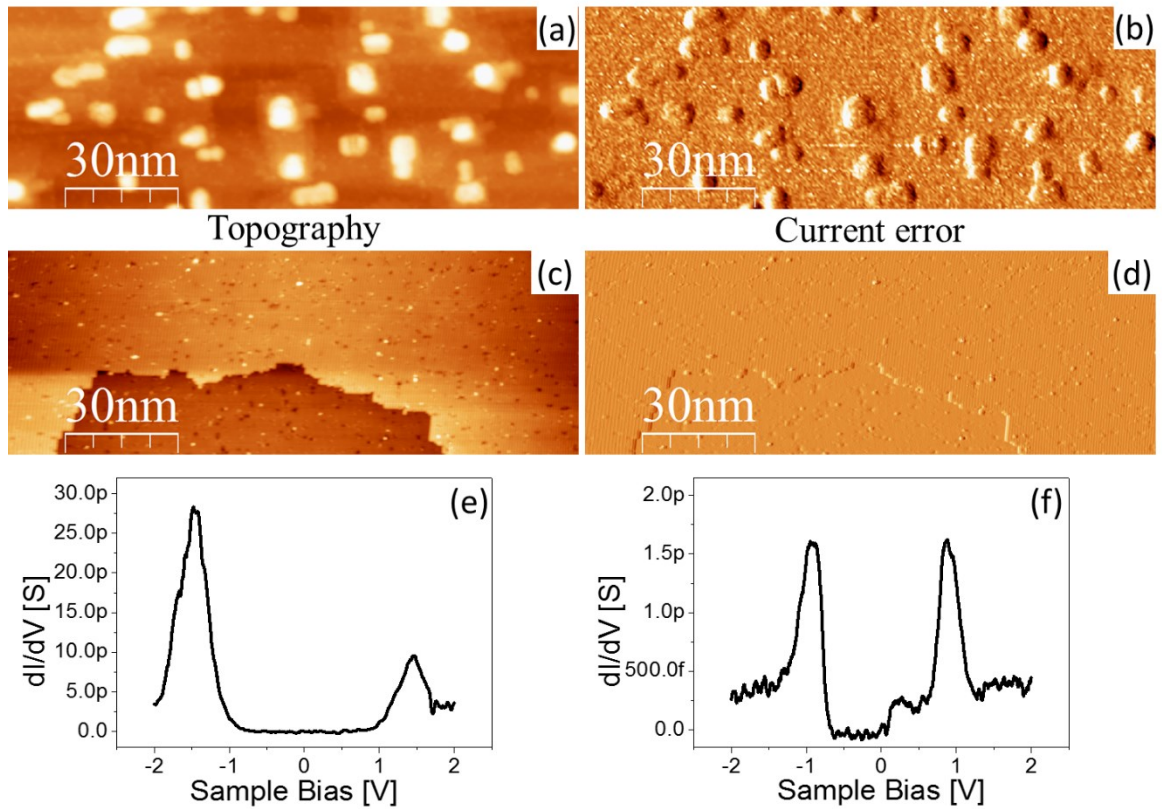


Fig. 3.11: Topography (a) and current error (b) STM images of a pristine 50 nm SOI sample after 10 anneal cycles at 750 °C, each lasting 90 s. Topography (c) and current error (d) STM images of 30s oxygen plasma cleaned 43 nm SOI sample annealed with the same parameters as above. All STM image dimensions are 150×54 nm and imaging set points (a) and (b): 3 V, 5 pA; (c) and (d): 2 V, 20 pA; (e) and (f) STS recorded on a SiC protrusion and on Si device layer of SOI following the 30 s oxygen plasma cleaning, respectively [9].

silicon surface, while the HF treatment etches off the oxide grown in the plasma chamber. Approximately 1 nm thick oxide layer was chemically grown on the SOI surface by rinsing it briefly in H_2O_2 solution before loading into the UHV chamber. Fig. 3.11 shows STM topography and current error images of a pristine 50 nm SOI and a plasma-cleaned 43 nm SOI. The bright regions seen in the topographic data for the pristine sample in Fig. 3.11(a) are the SiC protrusions. These protrusions can clearly be seen on the current error image shown in Fig. 3.11(b). There is a marked difference in the number of protrusions on the plasma-cleaned samples compared to the pristine samples. Fig. 3.10(e) shows the scanning tunneling spectra (STS) recorded on a SiC protrusion. The band gap of the SiC structure was observed to be around 2 eV, similar to the value reported in the literature [29-32]. The STS spectrum recorded on the clean Si surface is shown Fig. 3.11(f) for comparison. STM height and current error images for a cleaned 43 nm SOI are shown in Fig. 3.11(c) and 3.11(d) respectively, which clearly shows the reduction in the SiC protrusions on the silicon surface following the *ex situ* cleaning procedure.

The plasma power was varied so as to achieve a sputtering action in the ICP system. Exposure to a low energy oxygen plasma results in the growth of 4 – 5 nm of oxide on the Si surface, before saturation. However, with increased plasma power and forward voltage, the top layer of oxide is continuously sputtered, hence a greater thickness of oxide is grown, thinning the device layer. This plasma

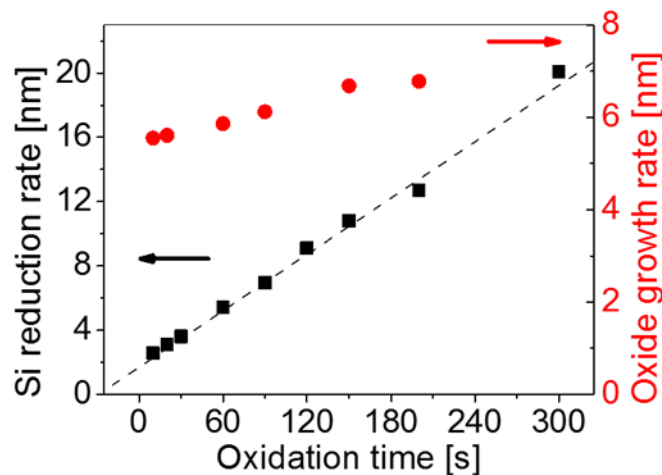


Fig. 3.12: Si thinning rate and oxide growth rate plotted against the ICP time.

thinning process was observed to result in an atomically smooth SOI surface (height and current error STM image shown in Fig. 3.11 (c) and 3.11(d)). Fig. 3.12 presents the Si thinning rate for a 2000 W oxygen plasma recipe. The SOI and the oxide thicknesses were measured using ellipsometry. It can be seen that while the oxide thickness (red dots) saturates at around 7 nm, the SOI thinning rate (black square) is linear with a slope of 5 nm/min. The plasma thinning process results in an atomically smooth SOI surface.

3.8 Conclusion

Oxide desorption from SOI in UHV conditions without dewetting of the device layer is a challenge due to its dependency on both anneal temperature and duration. Different anneal procedures were investigated in order to find an effective low thermal budget process. The mechanism of desorption at different stages of oxide removal was studied on individual sample by taking advantage of a thermal gradient of ~ 50 °C across the sample during annealing. Ten 90 s anneal cycles at 750 °C were found to remove oxide from the entire sample; however, surface protrusions were found on the thermally processed samples. XPS and AFM measurements performed on pristine and flashed samples confirmed the removal of the oxide layer during thermal treatment. Also, the measurements indicated that carbon present on the sample remains on the surface during annealing and reacts with silicon to form silicon carbide. A simple oxygen plasma cleaning followed by HF and H₂O₂ treatment carried out before *in situ* annealing was found to reduce the SiC protrusions substantially, resulting in an atomically smooth SOI surface. The oxygen plasma process was also utilised to thin the device layer. A simple low thermal budget annealing process has been developed to produce an atomically clean and oxide free SOI surface without dewetting.

3.9 References

1. Xue, K., J.B. Xu, and H.P. Ho, *Nanoscale in situ investigation of ultrathin silicon oxide thermal decomposition by high temperature scanning tunneling microscopy*. Nanotechnology, 2007. **18**(48): p. 485709.
2. Hibino, H., M. Uematsu, and Y. Watanabe, *Void growth during thermal decomposition of silicon oxide layers studied by low-energy electron microscopy*. Journal of Applied Physics, 2006. **100**(11): p. 113519.
3. Sun, Y.K., D.J. Bonser, and T. Engel, *Spatial inhomogeneity and void-growth kinetics in the decomposition of ultrathin oxide overlayers on Si(100)*. Physical Review B, 1991. **43**(17): p. 14309-14312.
4. Sun, Y.K., *Thermal decomposition of ultrathin oxide layers on Si(100)*. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 1992. **10**(4): p. 2314.
5. Johansson, U., H. Zhang, and R. Nyholm, *Thermal desorption of oxides on Si(100): a case study for the scanning photoelectron microscope at MAX-LAB*. Journal of Electron Spectroscopy and Related Phenomena, 1997. **84**(1–3): p. 45-52.
6. Ogawa, S., et al., *Consumption kinetics of Si atoms during growth and decomposition of very thin oxide on Si(001) surfaces*. Thin Solid Films, 2006. **508**(1-2): p. 169-174.
7. Johnson, K.E., et al., *The mesoscopic and microscopic structural consequences from decomposition and desorption of ultrathin oxide layers on Si(100) studied by scanning tunneling microscopy*. Surface Science, 1993. **290**(3): p. 213-231.
8. Kinefuchi, I., et al., *Inhomogeneous decomposition of ultrathin oxide films on Si(100): application of Avrami kinetics to thermal desorption spectra*. J Chem Phys, 2008. **128**(16): p. 164712.
9. Barimar, P.S.N., et al., *Study of the effect of thermal treatment on morphology and chemical composition of silicon-on-insulator*. Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena, 2016. **34**(4): p. 041806.

10. Tromp, R., et al., *High-temperature SiO₂ decomposition at the SiO₂/Si interface*. Phys Rev Lett, 1985. **55**(21): p. 2332-2335.
11. Liehr, M., *Kinetics of high-temperature thermal decomposition of SiO₂ on Si(100)*. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 1987. **5**(4): p. 1559.
12. Jones, D. and V. Palermo, *Production of nanostructures of silicon on silicon by atomic self-organization observed by scanning tunneling microscopy*. Applied Physics Letters, 2002. **80**(4): p. 673.
13. Danielson, D.T., et al., *Surface-energy-driven dewetting theory of silicon-on-insulator agglomeration*. Journal of Applied Physics, 2006. **100**(8): p. 083507.
14. Busmann, E., et al., *Thermal instability of silicon-on-insulator thin films measured by low-energy electron microscopy*. IOP Conference Series: Materials Science and Engineering, 2010. **12**: p. 012016.
15. Busmann, E., et al., *Dynamics of solid thin-film dewetting in the silicon-on-insulator system*. New Journal of Physics, 2011. **13**(4): p. 043017.
16. Legrand, B., et al., *Formation of silicon islands on a silicon on insulator substrate upon thermal annealing*. Applied Physics Letters, 2000. **76**(22): p. 3271.
17. Legrand, B., et al., *Thermally assisted formation of silicon islands on a silicon-on-insulator substrate*. Journal of Applied Physics, 2002. **91**(1): p. 106.
18. Nuryadi, R., Y. Ishikawa, and M. Tabe, *Formation and ordering of self-assembled Si islands by ultrahigh vacuum annealing of ultrathin bonded silicon-on-insulator structure*. Applied Surface Science, 2000. **159–160**: p. 121-126.
19. Aouassa, M., et al., *The kinetics of dewetting ultra-thin Si layers from silicon dioxide*. New Journal of Physics, 2012. **14**(6): p. 063038.
20. Leroy, F., et al., *Dynamics, anisotropy, and stability of silicon-on-insulator dewetting fronts*. Physical Review B, 2012. **85**(19).
21. Yang, B., et al., *Self-organization of semiconductor nanocrystals by selective surface faceting*. Physical Review B, 2005. **72**(23).
22. Tabe, M., et al., *Formation of high-density silicon dots on a silicon-on-insulator substrate*. Applied Surface Science, 1999. **142**(1–4): p. 553-557.

23. Ota, Y., *n-Type Doping Techniques in Silicon Molecular Beam Epitaxy by Simultaneous Arsenic Ion Implantation and by Antimony Evaporation*. J. Electrochem. Soc, 1979. **126**(10).
24. Zhang, P., et al., *Electronic transport in nanometre-scale silicon-on-insulator membranes*. Nature, 2006. **439**(7077): p. 703-706.
25. Sutter, P., W. Ernst, and E. Sutter, *Scanning tunneling microscopy on ultrathin silicon on insulator (100)*. Applied Physics Letters, 2004. **85**(15): p. 3148.
26. Sinniah, K., et al., *Hydrogen desorption from the monohydride phase on Si(100)*. The Journal of Chemical Physics, 1990. **92**(9): p. 5700-5711.
27. Gupta, P., V.L. Colvin, and S.M. George, *Hydrogen desorption kinetics from monohydride and dihydride species on silicon surfaces*. Physical Review B, 1988. **37**(14): p. 8234-8243.
28. Niwano, M., M. Terashi, and J. Kuge, *Hydrogen adsorption and desorption on Si(100) and Si(111) surfaces investigated by in situ surface infrared spectroscopy*. Surface Science, 1999. **420**(1): p. 6-16.
29. Young Park, J. and R.J. Phaneuf *Conductance imaging of thermally desorbed silicon oxide*. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, 2003. **21**(4): p. 1254.
30. Bonnell, D.A., G.S. Rohrer, and R.H. French, *tunneling spectroscopic analysis of optically-active wide band-gap semiconductors*. Journal of Vacuum Science & Technology B, 1991. **9**(2): p. 551-556.
31. Tawada, Y., *Properties and structure of a-SiC:H for high-efficiency a-Si solar cell*. Journal of Applied Physics, 1982. **53**(7): p. 5273.
32. Demichelis, F., C.F. Pirri, and E. Tresso, *Influence of doping on the structural and optoelectronic properties of amorphous and microcrystalline silicon carbide*. Journal of Applied Physics, 1992. **72**(4): p. 1327.
33. Bozack, M.J., et al., *Chemical activity of the C C double bond on silicon surfaces*. Surface Science, 1986. **177**(1): p. L933-L937.
34. Yoshinobu, J., et al., *The adsorbed states of ethylene on Si(100)c(4×2), Si(100)(2×1), and vicinal Si(100) 9°: Electron energy loss spectroscopy and*

- low-energy electron diffraction studies*. The Journal of Chemical Physics, 1987. **87**(12): p. 7332-7340.
35. Mayne, A.J., et al., *An STM study of the chemisorption of C₂H₄ on Si(001)(2 × 1)*. Surface Science, 1993. **284**(3): p. 247-256.
36. Bender, H., S. Verhaverbeke, and M. Heyns, *Hydrogen Passivation of HF-Last Cleaned (100) Silicon Surfaces Investigated by Multiple Internal Reflection Infrared Spectroscopy*. Journal of the Electrochemical Society, 1994. **141**(11): p. 3128-3136.
37. Fisher, A.J., P.E. Blöchl, and G.A.D. Briggs, *Hydrocarbon adsorption on Si(001): when does the Si dimer bond break?* Surface Science, 1997. **374**(1): p. 298-305.
38. Pan, W., T. Zhu, and W. Yang, *First-principles study of the structural and electronic properties of ethylene adsorption on Si(100)-(2×1) surface*. The Journal of Chemical Physics, 1997. **107**(10): p. 3981-3985.
39. Zhao, L., et al., *Characterization on the passivation stability of HF aqueous solution treated silicon surfaces for HIT solar cell application by the effective minority carrier lifetime measurement*. Chinese Journal of Physics, 2010. **48**(3): p. 392-399.
40. Johnson, K.E. and T. Engel, *Direct measurement of reaction kinetics for the decomposition of ultrathin oxide on Si(001) using scanning tunneling microscopy*. Phys Rev Lett, 1992. **69**(2): p. 339-342.
41. Miyata, N., H. Watanabe, and M. Ichikawa, *Thermal Decomposition of an Ultrathin Si Oxide Layer around a Si(001)- (2 × 1) Window*. Physical Review Letters, 2000. **84**(5): p. 1043-1046.
42. Wei, Y., R.M. Wallace, and A.C. Seabaugh, *Void formation on ultrathin thermal silicon oxide films on the Si(100) surface*. Applied Physics Letters, 1996. **69**(9): p. 1270.
43. Engstrom, J.R., et al., *The reaction of atomic oxygen with Si(100) and Si(111)*. Surface Science, 1991. **256**(3): p. 317-343.
44. Liehr, M., H. Dallaporta, and J.E. Lewis, *Defect formation in SiO₂/Si(100) by metal diffusion and reaction*. Applied Physics Letters, 1988. **53**(7): p. 589-591.

45. Gurevich, A.B., et al., *Thermal evolution of impurities in wet chemical silicon oxides*. Applied Physics Letters, 1999. **74**(9): p. 1257-1259.
46. Kobayashi, Y. and K. Sugii, *Scanning tunneling microscope study on mid-desorption stages of native oxides on Si(111)*. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 1991. **9**(2): p. 748-751.
47. Irajizad, A., et al., *Thermal desorption of ultrathin silicon oxide layers on Si(111)*. Semiconductor Science and Technology, 2000. **15**(2): p. 160.
48. Yamada, H., *Microscopic composition difference related to oxidizing humidity near the ultrathin silicon oxide–Si(100) interface*. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 2001. **19**(2): p. 627-632.
49. Bhargava, M., et al., *Bragg diffraction, synchrotron x-ray reflectance, and x-ray photoelectron spectroscopy studies of low temperature plasma oxidation of native SiO₂ on silicon on insulator*. Journal of Vacuum Science & Technology B, 2008. **26**(1): p. 305-309.
50. Himpsel, F.J., et al., *Microscopic structure of the SiO₂/Si interface*. Physical Review B, 1988. **38**(9): p. 6084-6096.
51. Bashouti, M.Y., et al., *A Non-Oxidative Approach Towards Hybrid Silicon Nanowire- Based Solar Cell Heterojunctions*. Hybrid Materials, 2014. **1**(1).
52. Hollinger, G. and F.J. Himpsel, *Oxygen chemisorption and oxide formation on Si(111) and Si(100) surfaces*. Journal of Vacuum Science & Technology A, 1983. **1**(2): p. 640-645.
53. Watanabe, H., K. Fujita, and M. Ichikawa, *Thermal decomposition of ultrathin oxide layers on Si(111) surfaces mediated by surface Si transport*. Applied Physics Letters, 1997. **70**(9): p. 1095-1097.
54. Bywalez, R., et al., *Stabilization of mid-sized silicon nanoparticles by functionalization with acrylic acid*. Nanoscale Research Letters, 2012. **7**(1): p. 1-7.
55. Merino, P., et al., *Graphene etching on SiC grains as a path to interstellar polycyclic aromatic hydrocarbons formation*. Nat Commun, 2014. **5**: p. 3054.

56. Popescu, A., et al., *The Role of Ambient Gas and Pressure on the Structuring of Hard Diamond-Like Carbon Films Synthesized by Pulsed Laser Deposition*. Materials, 2015. **8**(6): p. 3284-3305.
57. Ahn, H.S., et al., *Application of phase contrast imaging atomic force microscopy to tribofilms on DLC coatings*. Wear, 2001. **249**(7): p. 617-625.
58. Ye, Z. and X. Zhao, *Phase imaging atomic force microscopy in the characterization of biomaterials*. Journal of microscopy, 2010. **238**(1): p. 27-35.
59. Stoldt, C.R., et al., *Micromechanical properties of silicon-carbide thin films deposited using single-source chemical-vapor deposition*. Applied Physics Letters, 2001. **79**(3): p. 347.
60. Mehregany, M., et al., *Internal stress and elastic modulus measurements on micromachined 3C-SiC thin films*. IEEE Transactions on Electron Devices, 1997. **44**(1): p. 74-79.
61. SUJIROTE, K.L., P., *Silicon carbide formation from pretreated rice husks*. Journal of Materials Science, 2003. **38**(23): p. 4739-4744.
62. Krishnarao, R.V., Y.R. Mahajan, and T.J. Kumar, *Conversion of raw rice husks to SiC by pyrolysis in nitrogen atmosphere*. Journal of the European Ceramic Society, 1998. **18**(2): p. 147-152.
63. Opila, E.J. and Q.N. Nguyen, *Oxidation of Chemically-Vapor-Deposited Silicon Carbide in Carbon Dioxide*. Journal of the American Ceramic Society, 1998. **81**(7): p. 1949-1952.
64. Suzuki, T., D.C. Sorescu, and J.T. Yates, *The chemisorption of pentacene on Si(001)-2 x 1*. Surface Science, 2006. **600**(23): p. 5092-5103.
65. Jemander, S.T., et al., *STM study of the C-induced Si(100) - c(4 x 4) reconstruction*. Physical Review B, 2002. **65**(11): p. 115321.
66. Miki, K. and K. Sakamoto, *Is the c(4x4) reconstruction of Si(001) associated with the presence of carbon?* Applied Physics Letters, 1997. **71**(22): p. 3266.
67. Maeng, J.Y. and S. Kim, *Scanning tunneling microscopy study on c(4 x 4) structure of Si(100)*. Surface Science, 2001. **482**: p. 1445-1450.
68. Meuris, M., et al., *the imec clean - a new concept for particle and metal removal on si surfaces*. Solid State Technology, 1995. **38**(7): p. 109-&.

4

S P R E A D I N G R E S I S T A N C E A T T H E N A N O – S C A L E S T U D I E D B Y S C A N N I N G T U N N E L I N G A N D F I E L D E M I S S I O N S P E C T R O S C O P Y

In this chapter, the capability of scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) to study nanoscale Si(100) device layers in silicon-on-insulator (SOI) is explored. The device layer is a macroscopic 2D silicon sheet and understanding the effective coupling of charge in and out of this sheet determines whether it is possible to accurately measure the electronic properties of the sheet by STM techniques. Specifically, how spreading resistance manifests in STM following the processing of SOI device layers with various doping levels, is discussed in this chapter. Depending on the doping level, ultra-thin SOI can exhibit significant blue shifts of the peaks in the tunneling and field emission spectra. By comparing these peak shifts with the film resistivity it is possible to estimate the contribution of spreading resistance in STM and STS. It is also shown that STM can be used to study the effective n-type dopant concentrations in the 10^{13} - 10^{16} cm⁻³ range. Finally, it's shown that ultra-thin SOI with sufficiently high doping levels ($\sim 10^{20}$ cm⁻³) and device layer thicknesses down to 5 nm can be studied with STM and that these materials exhibit bulk like electronic characteristics.

4.1 Introduction

Silicon-on-Insulator (SOI) has attracted a great deal of scientific interest as it offers the opportunity to study nanoscale devices and electron confinement effects [4]. The device layer in SOI is essentially a macroscopic near-perfect 2D silicon sheet. The use of SOI in microelectronics is becoming prevalent and many of the expected advances in device technology depends essentially on attaining increasingly thinner device layers [4]. Due to charge traps at the device layer and buried oxide interface, thinner SOIs tend to be depleted of charge carriers, thus affecting their transport properties [4-6]. Depleted and heavily thinned SOI is difficult to characterize by STM due to charging effects [5, 6]. By heavily doping ($\sim 10^{19} \text{ cm}^{-3}$) the device layer, the carrier depletion in the layer can be reduced and STM measurements can be conducted out even at liquid nitrogen temperature, but these high doping levels are not of interest for device applications.

Before STM and STS can be used to characterize nanoscale devices, it is critical to be able to understand the influence of doping on the fundamental operation of STM. In standard STM operation, the tunnel gap resistance dominates and the sample resistance and spreading resistance play a negligible role [7]. Consequently the applied bias allows the determination of energy states around the Fermi energy (E_F), which is the basis of STS. Spreading resistance arises due to the small area of the tunneling contact but also depends on the sample resistivity [8]. When the resistivity of the sample is high, the spreading resistance can become comparable with the tunneling resistance [7] leading to a voltage drop within the sample that can be observed in both STM and STS [9]. Also, in the case of semiconductors, especially at low doping levels, the high field from the STM tip can penetrate into the sample and lead to a tip-field induced band bending in the semiconductor. Consequently, it is expected that an interplay between spreading resistance and band bending has the potential to affect the measured properties of SOI device layers [7, 10-12]. Tip-field induced band bending in a Si(100) device layer is limited to a maximum of 0.8 eV due to Fermi level pinning of the surface state [13]. However, contribution from the spreading resistance can in principle give rise to much higher voltage drops [13]. Spreading resistance adds in series [7] with the tunneling resistance and leads to a

drop in the applied voltage in the sample near the tip location. This local voltage drop in the device layer will shift the peaks in the tunneling and field emission spectra.

This chapter discusses the sensitivity of STM, STS and field emission spectroscopy to spreading resistance and tip-induced field effects in SOI device layers and thus to the effective resistivity of the subsurface substrate volume. Furthermore, it is demonstrated that by highly doping the ultra-thin SOI, the effects of tip-induced band bending and spreading resistance can be significantly reduced. Hence, SOI with sufficiently high doping level were thinned and studied with STM and STS in an attempt to understand size effects in ultra-thin device layers.

4.2 Experimental details

All STM measurements were performed in a CreaTec low temperature STM (LT-STM) operated at liquid nitrogen temperature in an UHV environment with a base pressure lower than 1×10^{-11} mbar. A 45 nm SOI doped with phosphorous to $\sim 10^{19} \text{ cm}^{-3}$ was used to study the spreading resistance effects. Further measurements were also carried out on SOI samples with thicknesses less than 12 nm and dopant concentrations up to $\sim 10^{20} \text{ cm}^{-3}$. All samples were cut into a standard size of 11 mm x 4 mm to ensure uniform processing conditions. Before loading into the UHV chamber, samples were subjected to an *ex-situ* cleaning process which involved oxygen plasma treatment and a rinse in hydrofluoric acid (HF) [14]. Samples treated with oxygen plasma had a 6 – 8 nm thick layer of oxide on the surface. This oxide layer was then etched in dilute ($\sim 1\%$) HF, leaving the surface passivated with hydrogen. Finally, samples were rinsed in 30% hydrogen peroxide (H_2O_2) solution to leave the surface terminated with a thin layer of oxide. The plasma treatment process was also used to thin SOI samples. SOI thickness was measured with an accuracy of ± 0.5 nm with a Woollam Alpha-SE ellipsometer calibrated using a cross sectional TEM analysis. The dopant concentration and resistivity profile in the device layer were characterized with secondary ion mass spectroscopy (SIMS) and 4-point probe electrical resistivity measurements. The contact potential difference (CPD) and work function of H-passivated SOI were measured with respect to a reference gold layer with a platinum coated AFM tip in a Bruker Enviroscope atomic force microscope (AFM) at room temperature in Kelvin probe microscopy (KPM) mode. The AFM chamber was pumped

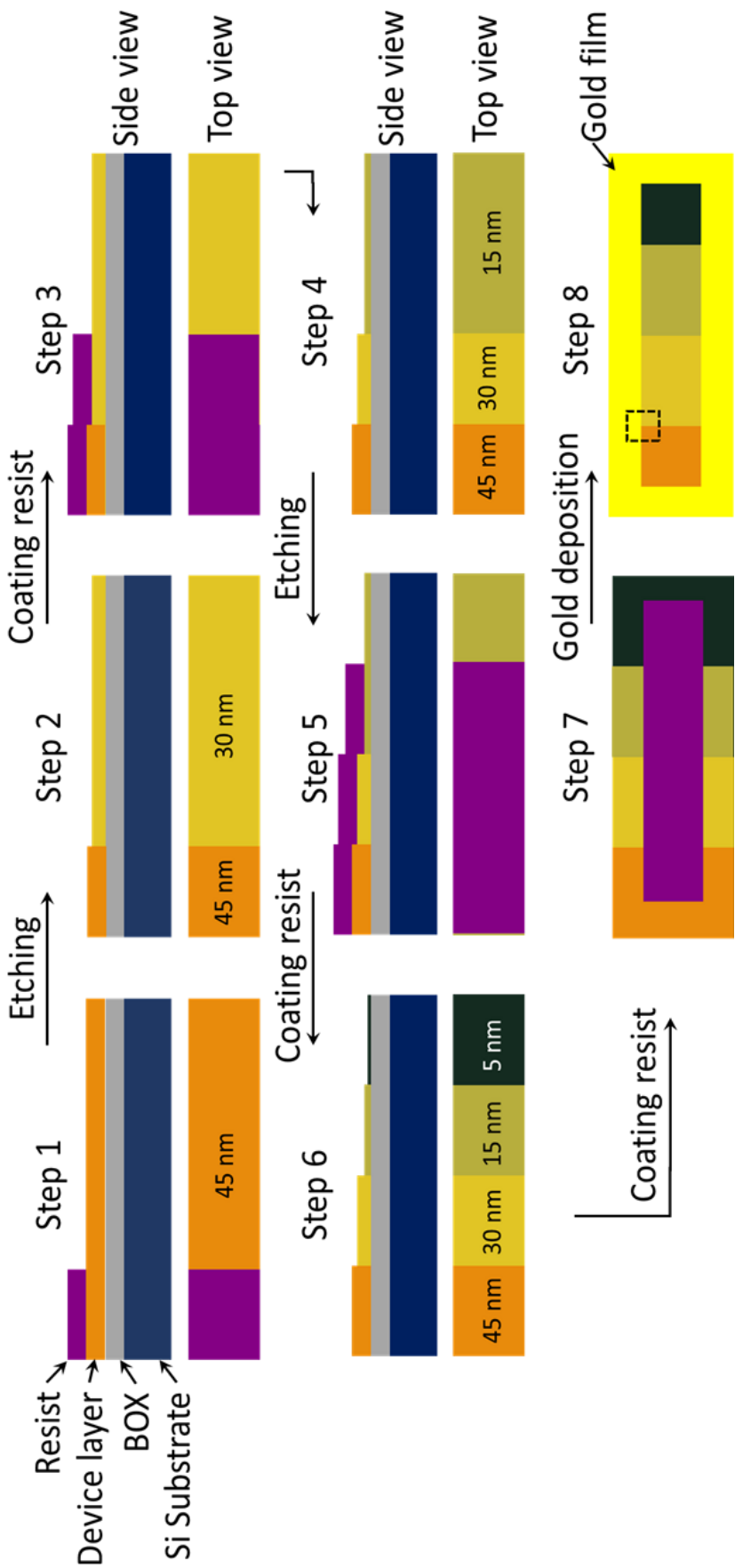


Fig. 4.1: Shows the schematic of sample preparation for KPM measurements, with device layer thickness varying between 45 nm and 3 nm. Firstly, a portion of SOI was coated with resist (step 1) and the uncoated area was etched to obtain two device layer thickness (step 2). This process was repeated multiple times such that, a continuous steps of various device layer thickness were obtained (step 3 – step 6). Finally, with the central region of the sample covered with resist, about 5 nm of titanium followed by 30 nm of gold was deposited (step 7). The Ti layer was used to improve Au adhesion on Si. As the resist at the middle of the sample was dissolved, SOI was left with a Ti/Au layer as shown in step 8. The dotted box in step 8 represents the KPM scan area covering two SOI thickness along with gold reference film.

down to mid- 10^{-6} mbar pressure and flushed with N_2 gas. This process was repeated several times to obtain an inert (estimated H_2O conc. of around 5-10 ppm) chamber. An inert AFM chamber ensured an oxide free H-passivated SOI surface for KPM measurements was maintained for several hours. SOI samples with device layer thicknesses varying between 45 nm and 4 nm were fabricated for KPM measurements. The sample fabrication process is outlined in Fig. 4.1. A portion of SOI was first coated with resist (step 1) while the uncoated area was etched using fluorine ($SF_6 + CHF_3$) plasma to obtain a step and two device layer thicknesses (step 2). The thinning process was repeated multiple times such that, continuous steps of various device layer thicknesses ranging from 45 nm – 3 nm were obtained (step 3 – step 6). This process was followed by oxygen plasma treatment to reduce the surface roughness. Finally, with the central region of the sample covered with resist, 30 nm of gold was deposited (step 7), with a 5 nm titanium buffer layer to improve Au adhesion on Si. The resist at the middle of the sample was later dissolved, in a process known as lift-off, leaving SOI with a Ti/Au layer as shown in step 8. The dotted box shown in step 8 of Fig. 4.1 depicts a typical KPM scan area covering at least two SOI thicknesses along with the gold reference film. The effects of annealing on dopant redistribution were studied in comparison to pristine and un-annealed samples with *ex situ* SIMS and electrical resistivity measurements.

The annealed samples were then investigated using STM. Samples were flash

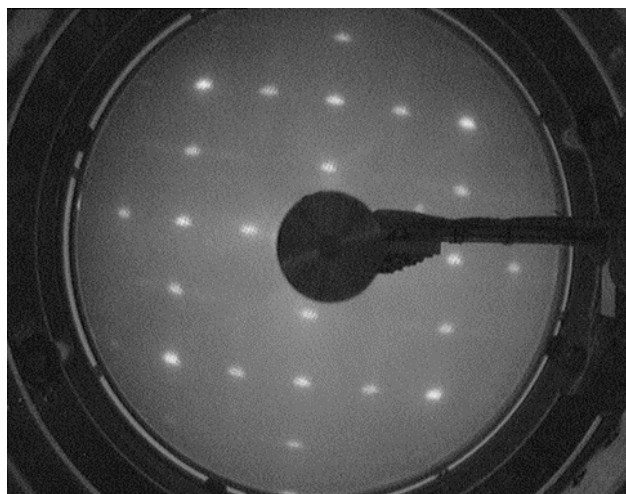


Fig. 4.2: Typical 2x1 LEED pattern observed at room temperature, for the Si(100) SOI samples of different device layer thickness after flashing.

annealed at approximately 750°C to desorb oxide. The cleanliness of the SOI was confirmed with low energy electron diffraction (LEED). All samples exhibited a sharp 2×1 LEED pattern (see Fig. 4.2) at room temperature following flash annealing. Electrochemically-etched tungsten tips inked with Pt were used for STM and STS measurements [15]. The quality of the tips was verified through imaging and spectroscopy as described in the section 4.3, before and after characterization of SOI to ensure that the probe was not modified. Tunneling and field emission spectra were obtained using STS techniques including field emission spectroscopy [16, 17] and variable height spectroscopy [15].

4.3 Tip quality determination

In STM, tunnelling occurs between a single atom at the apex of the STM probe tip and the sample and therefore, STM and STS data depends largely on the shape, size and chemical composition of the probe tip, especially the atom at the apex of the tip. The small separation and the high electric field of the tip along with the unreliable nature of the SOI samples poses a high risk of tip contamination. In this work, the quality of the STM tip was verified before and after every experiment, through imaging and tunneling spectroscopy on a sputter-cleaned Pt(111) crystal. (The tip etching

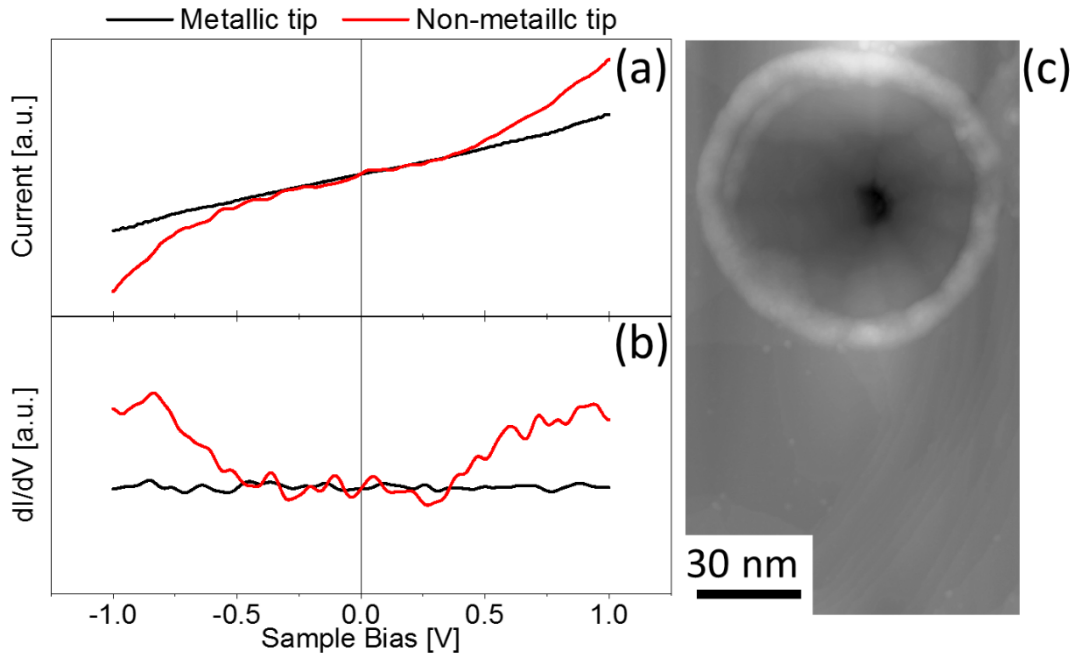


Fig. 4.3: (a) shows a I-V and (b) shows a dI/dV spectra of a metallic (black) and non-metallic tip (red). (c) is a STM image of the Pt(111) surface, showing the crater formed due to the tip-inking process.

process is described in Section 2.2.9 in Chapter 2.) The quality of the STM images were the primary indication of the sharpness of the tip. Repeating features and abnormal structures on the clean Pt(111) surface were common characteristics of a blunt or multiple tip. The tunneling spectra obtained using the tip on a clean Pt(111) surface was used to identify if the tip was metallic or not. Fig. 4.3(a) and Fig. 4.3(b) shows the I-V and dI/dV, respectively, of a metallic (black) and non-metallic (red) tip. The I-V spectra of a metallic tip on Pt surface gives a linear current response in the voltage range between -1 V and +1 V, hence the dI/dV spectra has no features. In contrary, a non-metallic tip shows a non-linear I-V curve on the Pt(111) surface which shows up like an energy gap in the dI/dV spectra. In cases where the tip was found to be non-metallic, it was coated with platinum by dipping the tip into the Pt(111) surface. A controlled tip-crash on a Pt surface can reshape the tip-apex and also coat the tip with metal [18, 19]. With the right voltage bias conditions during the controlled tip-crash, an atomically sharp Pt-coated tips can be obtained. Fig. 4.3(c) shows the crater formed on the Pt(111) surface following the tip-inking process. The crater roughly suggests the shape of the tip [19].

4.4 Topographic phase transition in Si (100) (2×1) STM

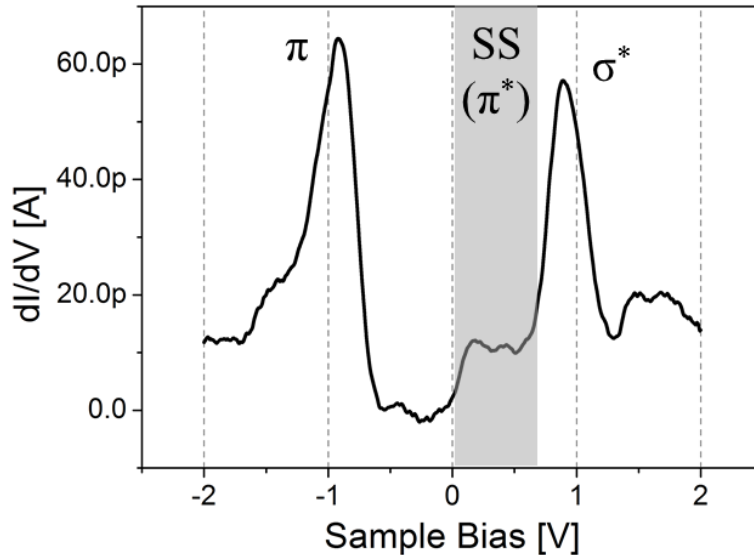


Fig. 4.4: Typical tunneling spectra for a bulk Si(100) (2×1) surface, indicating the occupied (π) and empty state (π^* and σ^*) spectral features. The shaded region depicts the surface states (SS).

A typical tunneling spectroscopy measurement on an ordered (2×1) region of the clean Si(100) surface is shown in Fig. 4.4 where the occupied state peak at approximately -0.8 eV below the Fermi level is due to the π -bonding orbital and the unoccupied state peak at 0.3 eV above the Fermi level is due to the π^* -anti-bonding orbital [2]. The sharp unoccupied state peak at +0.8 eV above the Fermi level is the contribution of back bond σ^* states. Fig. 4.5(a) and 4.5(b) show STM images recorded at biases corresponding to the two unoccupied state features of a LDOS spectra identified in Fig 4.5(c). Dimer backbond peaks are observed when imaging at a voltage

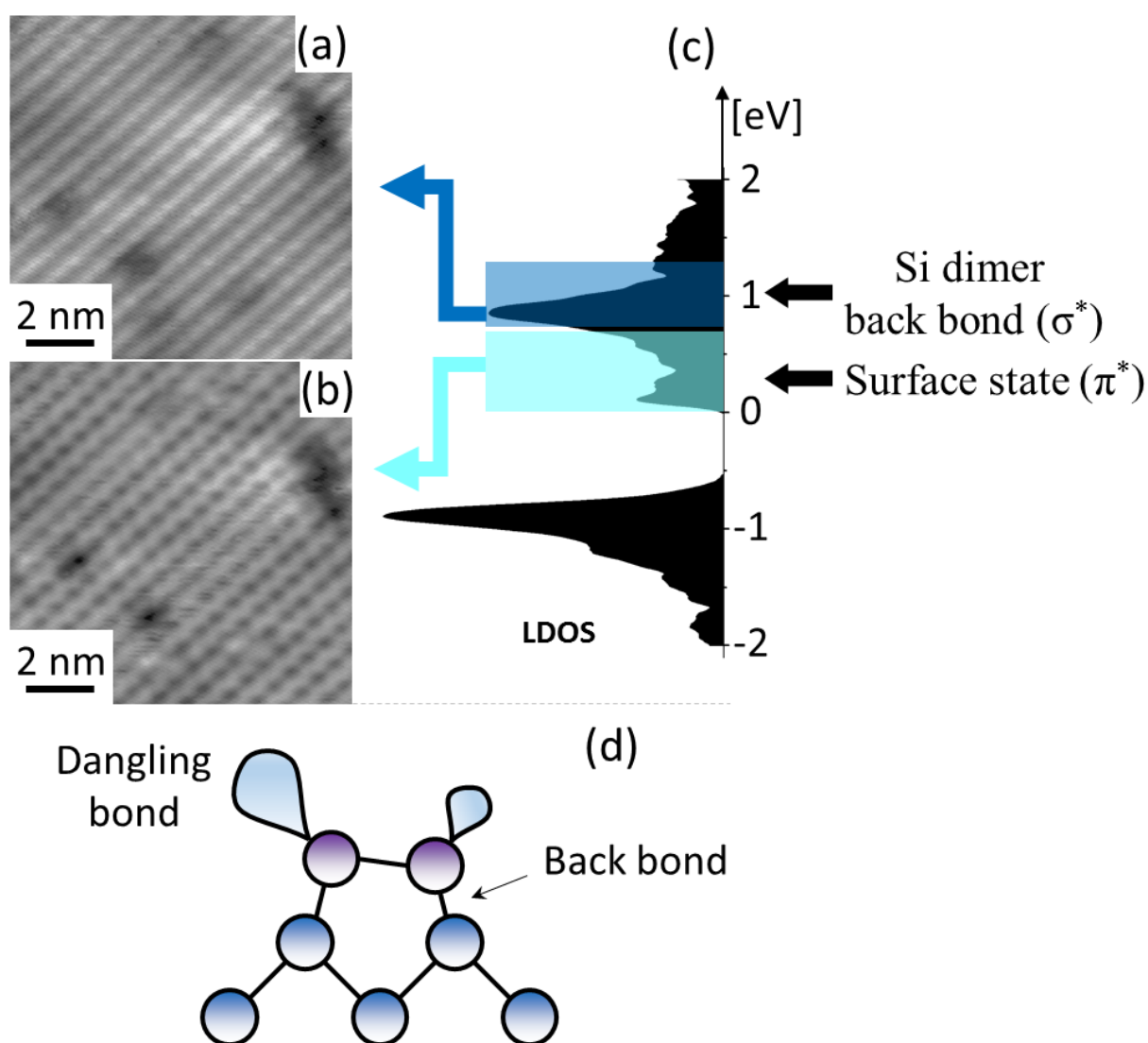


Fig. 4.5: (a) and (b) are constant-current filled state topographic images recorded at +1 V and +0.5 V, depicting the image contributions due to σ^* and π^* states, respectively. The σ^* and π^* states are marked in the LDOS spectra shown in (c). (d) Schematic representation of Si(100)-(2 $\times$ 1)[1] showing the dangling bonds and the back bonds [1, 2].

bias corresponding to the σ^* state (+1 V) (Fig. 4.5(a)), while the π^* dangling bond states (+0.5 V) exhibits a zig-zag pattern (Fig. 4.5(b)). Fig. 4.5(d) shows a schematic representation of dangling bonds and back bonds on Si(100) surface [2].

In the case of the bulk Si(100) sample the phase-transition (PT) in the topography occurs at an applied voltage of around 0.5 V. At voltages above 0.5 V, the Si dimer backbonds are imaged, while below 0.5 V, the empty π^* -bonds are imaged. The zig-zag pattern at <0.5 V is due to the Jahn-Teller distortion that form asymmetric dimers [2, 20]. It is possible to exploit the PT in the STM topography data to track apparent energy shifts observed in samples either due to varying material properties or as a result of an STM artefact. A particular advantage of this strategy is that the phase-transition can easily be observed in STM and does not require an exceptionally high resolution instrument. It also provides a means to track energy levels below the vacuum, in addition to the emission peaks that occur above the vacuum energy.

4.5 Voltage shift in STM and STS

With an aim to study the changing electronic structure of SOI as a function of its thickness, a 45 nm SOI was thinned (see Fig. 4.6(a)) and studied with STM and STS. The STS spectra for a 45 nm SOI was identical to that of the bulk Si (100). Even for the thinned SOI with thicknesses up to 16 nm, the STS spectra recorded was identical to bulk Si. However, SOI with thicknesses between 16 nm and 12 nm showed an unusual shift in the spectral features. Fig. 4.6(b) shows both the tunneling and field emission spectra obtained from the 45 nm device layer, along with samples made from the same SOI sample but thinned down to 16 nm, 14 nm, and 12 nm. For the 12 nm sample, the tunneling spectra were impossible to record due to the instability of the current at low biases. In all cases, emission spectra recorded at biases above 4 V reveal a systematic shift in the peak positions (indicated with lines marked as P1, P2 and P3) as the device layer thickness is decreased. The PT image for the 12 nm SOI is shown in Fig. 4.6(c); the transition occurs at an applied bias voltage between 2 V and 3 V, consistent with the blue shift of the emission peaks for thinner samples. This shift in the phase-transition voltage clearly identifies the peak marked (*) for the 12 nm SOI as originating from the σ^* state peak in the spectrum of the original 45nm sample. The shift in the

image phase-transition voltage is indicated by the red line in Fig. 4.4(a) and marked as PT.

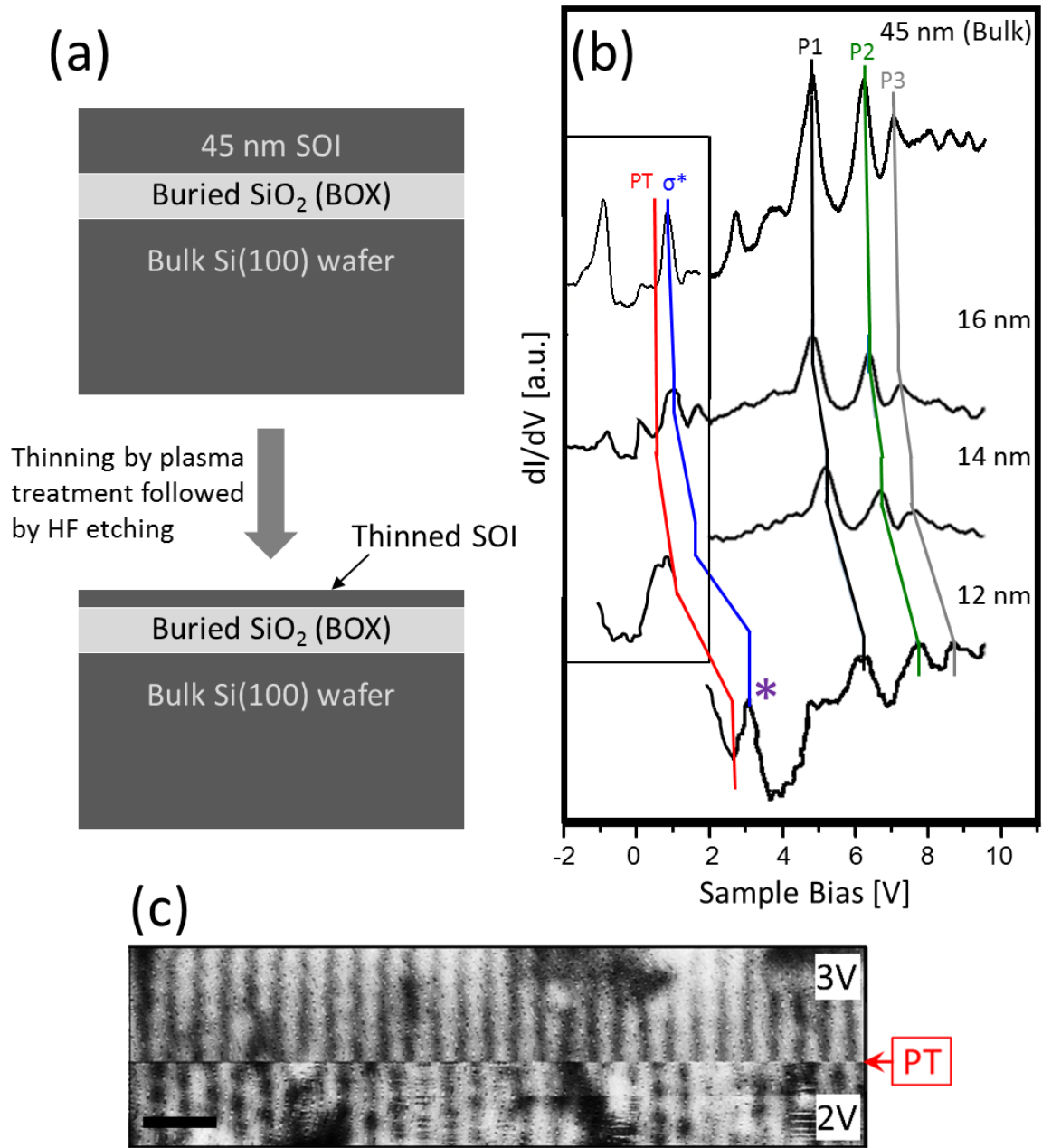


Fig. 4.6: (a) Schematic of SOI thinning. (b) Tunneling spectroscopy (IV) and field emission (z(V)) spectra of thinned SOI showing peak shifts. The blue line indicates the σ^* peak and the (*) symbol indicates the shifted σ^* peak for the 12 nm SOI. (b) Shows the ‘topographic phase transition’ (PT) between 3 V and 2 V for the 12 nm SOI.

Fig. 4.7 shows the measured voltage shifts observed in STM-PT and STS measurements in Fig 4.6(b) for different device layer thicknesses. The shifts observed

for the peaks in field emission spectra (Peaks 1, 2, and 3), the σ^* peak and the phase transition voltage, all show a gradual increase down to 14 nm, following which there is

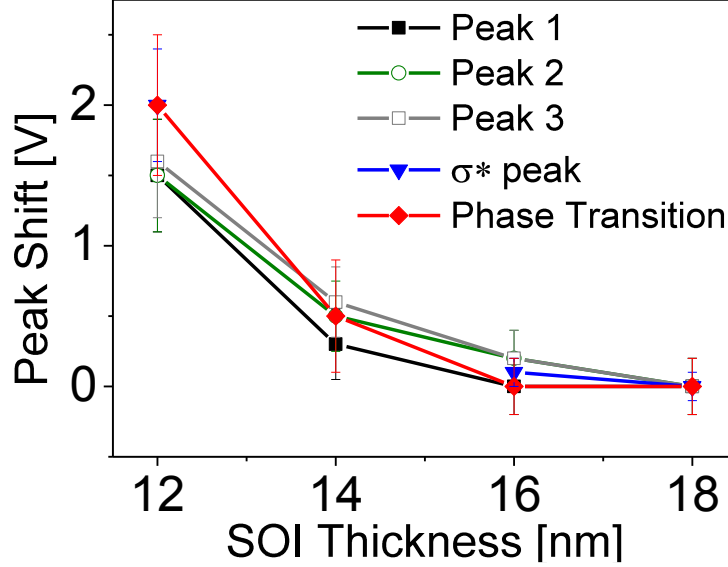


Fig. 4.7: Voltage shift observed in STM and STS measurements as a function of SOI film thickness. Peak 1, 2 and 3 are shown in Fig. 6(b) as P1, P2 and P3.

a sharp increase at 12 nm film thickness. A maximum voltage shift of approximately 1.5 – 2 V was observed for the 12 nm SOI. All tunneling and emission peaks in Fig. 4.7 experience similar blue shifts consistent with a translation of the entire spectrum, as shown by the shifting vertical lines in Fig. 4.6(b). The first peak (P1) in the field emission spectra gives the approximate position of the work function of the surface [16, 17, 21-24] and the position of P1 shifts sharply below 16 nm. If true, these measurements indicate a sharp rise in the SOI work function below 16 nm. In the following sections, different factors that can influence the STS and field emission spectra have been analysed.

4.6 STS blue shift vs band gap widening in Si thin film

As the size of nano structures decreases, the band gap of the material is known to increase due to the quantum confinement effect [25]. The band gap of ultra-thin silicon films have been reported to increase over 2 eV [25]. In order to understand the origin of the blue shift observed in the STS and field emission spectra, these data were compared with the electronic band gap widening data available in the literature. Fig.

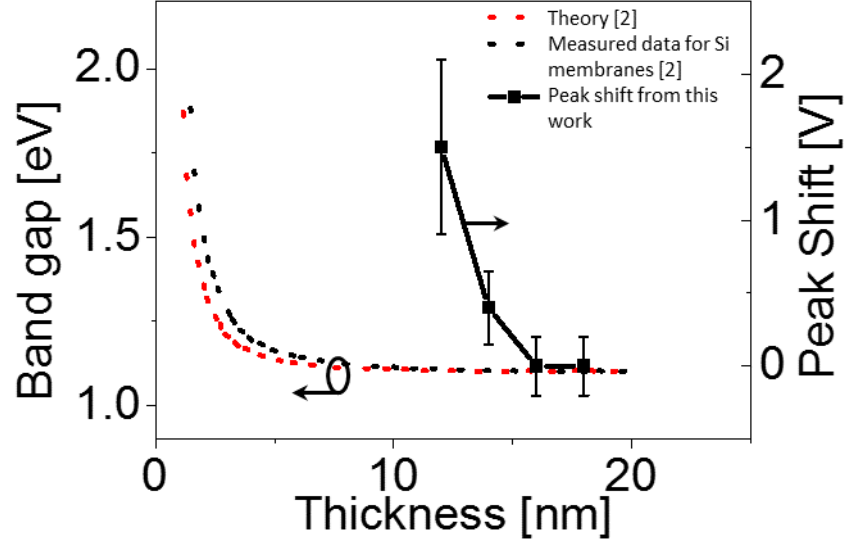


Fig. 4.8: Peak shift (black solid) observed in STM, STS and field emission spectroscopy plotted as a function of SOI thickness, showing a sharp increase in the shifted value below 16 nm. The peak shift data is compared with the theoretical (red dash) and experimental (black dash) bandgap of silicon as a function of thickness [3].

4.8 shows a comparison of the STS data and the bandgap of silicon thin films as a function of layer thickness, obtained from the literature. The energy gap of silicon thin films increases with decreasing film thickness. The energy gap thin films measured by the optical absorption spectroscopy [3] (shown by the black dotted line in Fig. 4.8), shows a systematic shift from the bulk band gap to higher values for film thickness below 10 nm [3, 25]. The theoretical values of the bandgap [3] as a function of thickness are also shown in Fig. 4.8 (red dotted line) for reference. The shift in the bandgap for thinner samples is due to the one dimensional confinement effect in ultra-thin silicon film. Both theoretical and the experimental band gap data are in close agreement. However, the shift in the STS and the field emission spectra, even though resembling the bandgap widening data reported for the silicon thin films, the onset of the band widening and the spectral blue shifts are separated by over 6 – 8 nm. This suggests that the blue shift in the STS and the field emission spectra are not a result of quantum size effects in the SOI thin film.

4.7 Sample resistance in STM

STM is an electron transport based technique, i.e., with the tip being grounded and a positive voltage applied to the sample, electrons that tunnel from the tip, flow through the sample. Hence, the sample is essentially a part of the STM circuit and the sample resistance adds in series to the tunneling resistance. In most cases, since the tunneling resistance is orders of magnitude higher than sample resistance, the contribution of sample resistance in the STM circuit is negligible. However, the resistance of thin film samples can be very high and this may contribute a significant

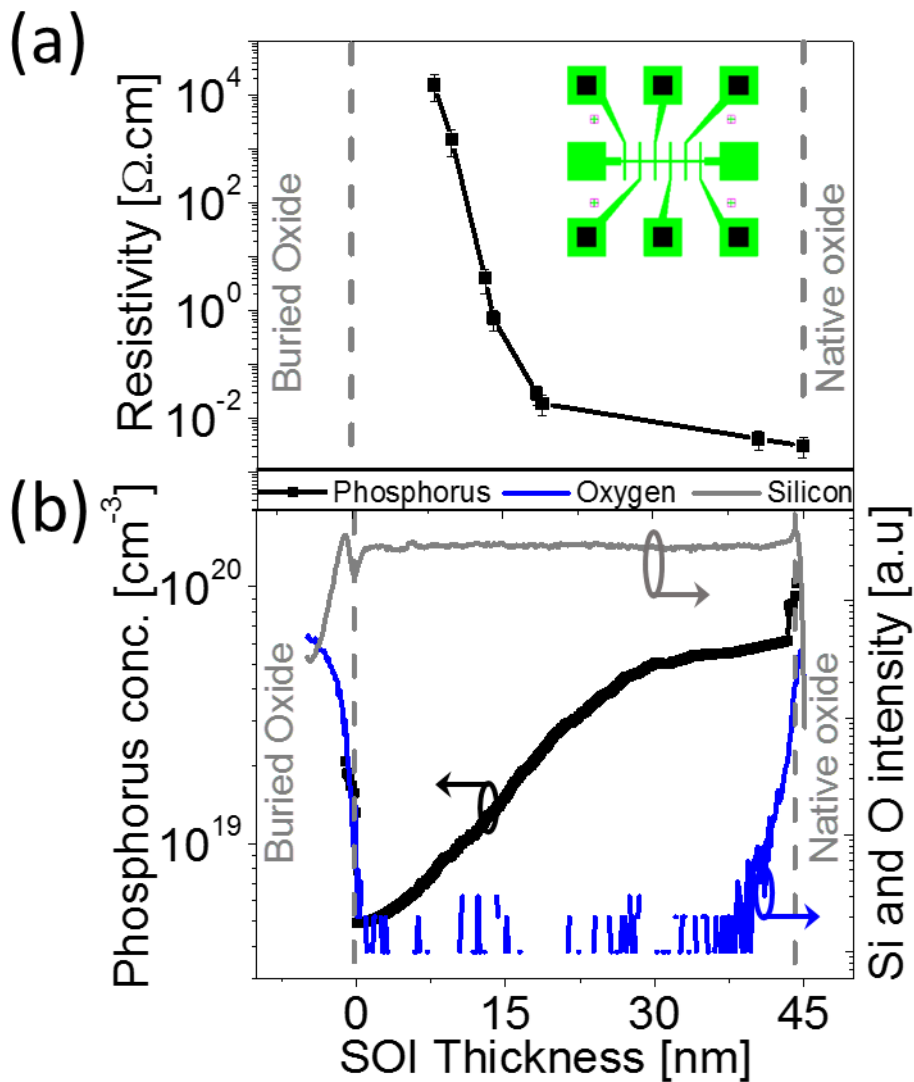


Fig. 4.9: (a) Four point resistivity of SOI as a function of device layer thickness. The grey dotted lines indicates the interfaces of the SOI films. The inset in (a) shows the typical UV lithography pattern used for electrical resistivity measurements. (b) Phosphorus concentration (black curve) of 45 nm SOI film recorded with SIMS depth analysis. Oxygen (blue) and silicon (grey) profile is also shown for reference.

series resistance in the STM circuit. To calculate the series resistance contribution of SOI in STM, the resistivity and dopant concentration in the device layer were studied through 4 probe electrical resistivity measurements and SIMS.

SOI samples were thinned and patterned into wires with a dimensions of 5 x 50 μm through UV lithography with Ti/Au electrodes deposited for electrical contacts. The inset in Fig. 4.9(a) shows the UV lithography pattern design used for the resistivity measurements. Fig. 4.9(a) shows the semi-log scale resistivity plot as a function of SOI thickness and Fig. 4.9(b) shows the SIMS depth profile (DP) analysis for Si (grey), P (black) and O (blue) in the device layer. The grey dotted lines in the graph indicate the physical boundaries of the device layer. The dotted line on the left indicates the SOI/BOX interface, the line on the right indicates the surface with native oxide. The resistivity of the device layer increased gradually as the device layer was progressively thinned from 45 nm to 16 nm but below 16 nm, it increased drastically. This is consistent with SIMS DP analysis for Si, P and O for the original 45 nm thick device layer (Fig. 4.9(b)). The phosphorous (n-type dopant) concentration in the device layer of the SOI decreases significantly towards the Si/BOX interface.

Fig. 4.10(a) shows a comparison between the phosphorus dopant concentration profile in the 45 nm device layer measured by SIMS and that estimated from electrical resistivity measurements at 300 K and 77 K. To calculate the dopant concentration from the resistivity data, the following formula was used,

$$\rho = \frac{1}{qn\mu_n} \quad (4.1)$$

where q is the elementary charge, n is the carrier concentration and μ_n the electron mobility [26]. The values for electron mobility in silicon at different temperatures and doping concentrations were taken from *Semiconductor devices., by S. M. Sze* [26]. While SIMS shows the chemical concentration of phosphorus in the device layer, resistivity reflects the active dopant concentration in the film [27]. Resistivity measurements were also influenced by the depletion caused by the buried oxide interface traps. The concentration of interface traps mainly depends on the chemical composition of the Si-SiO₂ interface [26]. Even for a high quality Si(100)-BOX interface, the interface trap density is typically on the order of 10^{10} - 10^{11} cm⁻² [6, 26, 28]. The

influence of interface traps increases with reduced device layer thickness since a thinner device layer will have lower carrier concentration.

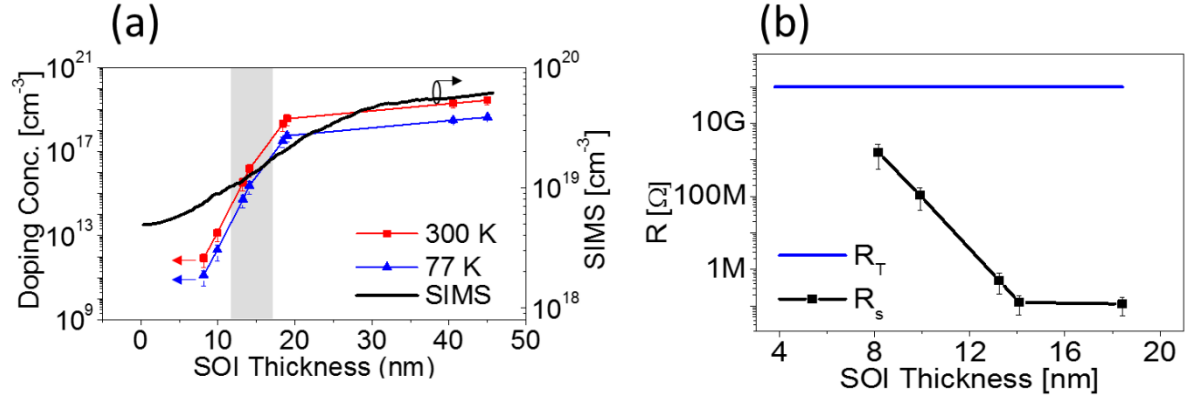


Fig. 4.10: (a) Doping concentration for SOI of varying thickness calculated from the resistivity data measured at 300 K (red) and 77 K (blue) plotted along with the SIMS data (black). The resistivity data indicates the electrically active dopant concentration which reduces towards the SOI/BOX interface due to the interface trap states. The resistivity data therefore deviates from the SIMS profile which shows the atomic concentration of phosphorous in the device layer. (b) Tunneling resistance R_T (blue) calculated at set point of 2V and 20 pA compared with sample resistance R_s (black) as a function of SOI thickness.

The concentration gradient measured by both techniques showed a similar trend with lower values at the SOI/BOX interface, but the drop in doping concentration predicted by resistivity measurement was many orders of magnitude greater than that measured by SIMS. For device layer thicknesses lower than 20 nm, the resistivity increased sharply. The grey region marked in the graph (see Fig. 4.10(a)), indicates the range of device layer thicknesses for which a voltage shift was observed in STM and STS. A sharply increasing device layer resistivity for these thicknesses suggests a possible connection between the device layer resistivity and the STM/STS voltage shift.

Fig. 4.10(b) compares the tunneling resistance R_T with the sample resistance R_s . The tunneling resistance, shown as a blue line in Fig 4.10(b), is calculated for a set point of 2 V and 20 pA. The sample resistance is calculated using the resistivity data obtained at 77 K and with a typical distances of 2 mm between the STM tip position over the sample and the sample electrode. In Fig. 4.10(b), even though a sharp increase in R_s is observed below 14 nm, R_s is still many orders of magnitude lower than R_T and therefore, R_s alone cannot be responsible for peak shifts in STM and STS.

4.8 Work function determination through KPM

The dopant concentration determines the position of the Fermi level in a semiconductor. For intrinsic silicon the Fermi level is at the centre of the energy gap which is midway between the valance band maxima (VBM) and conduction band minima (CBM). The Fermi level is above the intrinsic level for n-type silicon, moving towards the CBM for higher doping levels. Hence, the work function, which is the energy difference between the Fermi level and the vacuum level, decreases as the n-type doping concentration in the silicon increases and vice versa. The two observations, 1) blue shift in the field emission spectra, 2) the SIMS data revealing a decreasing dopant concentration in the SOI towards the BOX interface, both hint at an increase in the work function for thinned SOI. To quantitatively relate the two observations, a work function measurement was carried out on thinned SOI.

The work function of the film was measured independently via Kelvin probe microscopy (KPM) of the hydrogen passivated device layer. An elaborate sample preparation process, as discussed in the experimental section (Fig. 4.1), was used to obtain a stepped SOI sample. Since KPM data depends largely on the properties of the tip, it's very important to monitor and preserve the quality of the tip through-out the measurement. Fabrication of multiple steps with varying thicknesses on a single sample ensured an easy access to SOI of different thicknesses with the same tip and measurement conditions. Further, a gold reference layer on the film was used for calibration of the tip. KPM measures a contact potential difference (CPD) between the tip and the surface. A detailed description of KPM and CPD are given in section 2.5.2 and 2.5.3 of chapter 2. CPD is the work function difference between the tip and the sample surface i.e.,

$$V_{CPD} = \frac{\phi_{tip} - \phi_{sample}}{e} \text{ or } \phi_{sample} = \phi_{tip} - eV_{CPD}$$

Where the ϕ_{tip} is extracted using the reference gold film.

Fig. 4.11(a) shows an illustrative KPM CPD image of a 9 nm and 3 nm stepped SOI surface along with a gold reference layer. A clear distinction in the CPD was observed for various SOI thickness, which was normalized with respect to the CPD of the reference gold sample. Fig. 4.11(b) shows the variation in the CPD and work function of the film as a function of thickness. There is a clear increase in the work

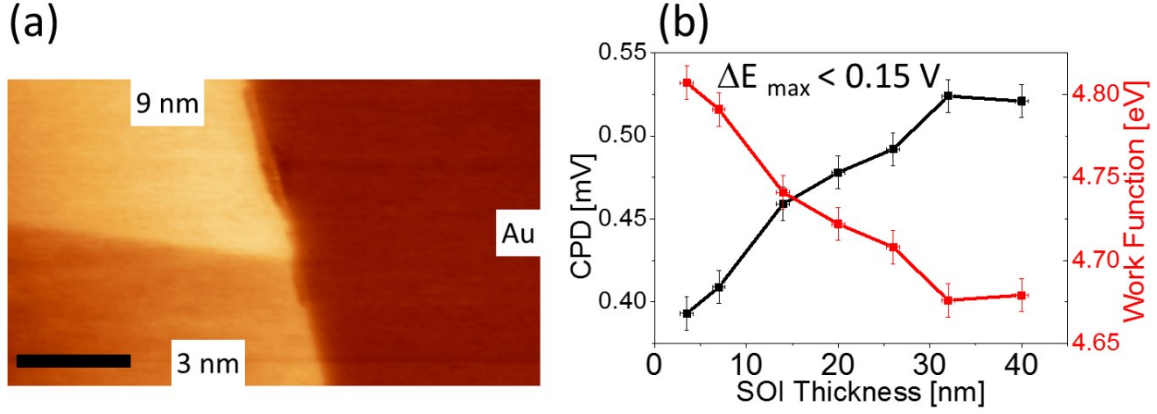


Fig. 4.11: (a) KPM image showing the contact potential difference (CPD) for two regions of SOI with respective thickness of 9 nm and 3 nm and a Au reference film. The scale bar in the image is 5 μm . (b) CPD (black) and work function (red) measured with ex-situ KPM on hydrogen-passivated thinned SOI plotted with respect to the thickness of the device layer.

function of the thinned SOI indicating a lower n-type phosphorus dopant concentration, consistent with the phosphorous SIMS profile measured in Fig. 4.9(b). However, the variation in work function observed over the entire range of device-layer thicknesses was less than 0.15 eV, in contrast to the 1.5 – 2 V shift observed in the case of STS and field emission measurements (Fig. 4.6(b) and Fig. 4.7). This indicates that the field emission peak shift observed in STM measurements, shown in Fig. 4.6(b), cannot be solely explained by the work function changes caused by the dopant profile in the film. Therefore, other factors that could cause these STS and field emission spectral shifts were explored.

4.9 Tip induced band bending in Si(100)

STM can be significantly affected by the high electric field of the STM tip which can penetrate into a semiconductor sample [11-13, 29, 30]. The penetrating field can lead to three dimensional tip-induced band bending extending not only in depth but also radially from the tip location [7]. The extent of bending is however determined by the carrier concentration in the semiconductor [7] and can lead to significant shifts in the peaks observed in the STS spectra [13], especially in high resistivity samples [7, 10, 12, 31]. For a 0.1 $\Omega \text{ cm}$ n-type Si(100) the presence of a tip with a radius of 10 Å at an applied bias of 1.5 V can induce band bending of 0.4 V [13]. However, the maximum band bending for a n-type Si(100)-(2 × 1) surface is restricted to 0.8 V [13]. This is a

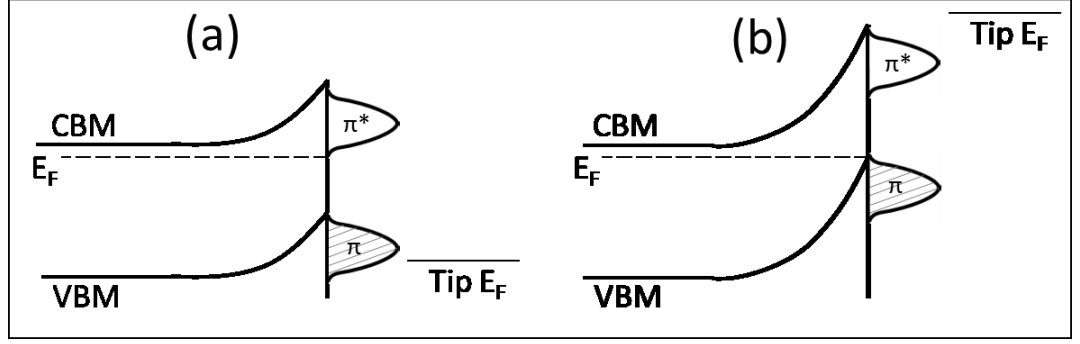


Fig. 4.12: Schematic illustration of tip-induced band bending for n-type Si(100)-(2 $\times$ 1) for (a) $V_{\text{sample}} \ll 0$ and (b) $V_{\text{sample}} \gg 0$.

consequence of the filled state π and the empty state π^* bands on the (2 $\times$ 1) surface being located at 0.2 eV below the valence band maximum (VBM) and 0.4 eV below the conduction band minima (CBM), respectively [32] (see Fig. 4.8), which constrains the E_F at the surface between the VBM and the empty π^* state. When scanning the surface with a positive sample bias, the electric field from the tip can locally unpin the surface and induce band bending until the Fermi level meets the VBM, resulting in a maximum bending of +0.8 V [13]. In contrast, a negative bias on the sample results in a small shift of +0.09 V as the E_F is pinned at the bottom of the π^* state [13]. However, the

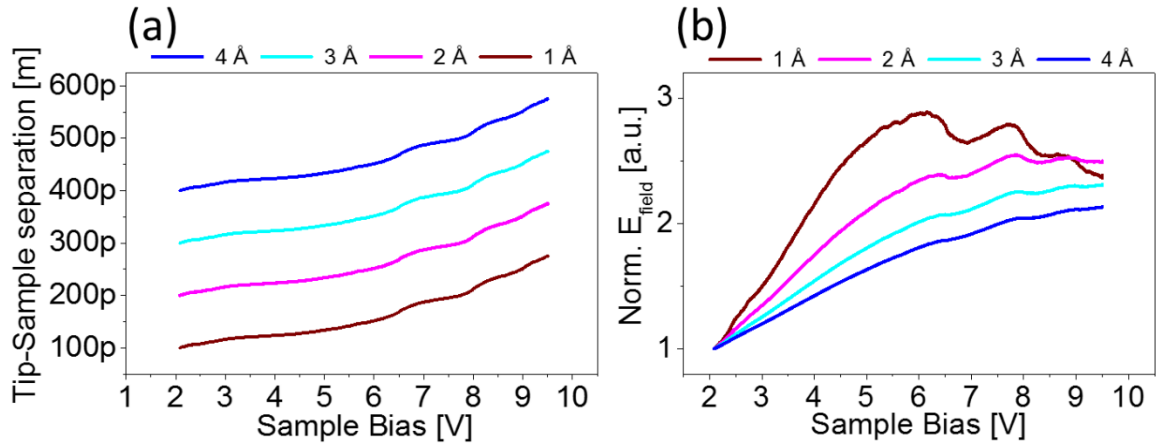


Fig. 4.13: (a) $z(V)$ spectra for 12 nm SOI showing the tip sample separation with the tip-sample separation off-set values between 1 – 4 Å. The tip-sample separation off-set depends on the set-point parameters, however, values between 1 and 4 Å have been used for demonstration propose. (b) Normalized electric field between the tip and the sample surface calculated using the $z(V)$ spectra in (a). For each spectra, the electric field at 6 V is almost twice the field at 2 V.

shifts observed in the STS spectra in Fig. 4.4(a) for different sample thicknesses are much larger than the contribution due to tip induced band bending.

Additionally, a tip-induced electric field effect would also show a voltage dependence in the peak shift observed in the field emission spectra, i.e., for a fixed set-point, a larger peak shift is expected at higher biases due to the larger field. Fig. 4.13(a) shows a $z(V)$ spectra obtained for a 12 nm SOI. Since, calculating the absolute separation between the tip and the surface is an arduous task, different off-set values between 1 – 4 Å have been chosen for demonstration purposes. Fig. 4.13(b) shows the normalized electric field calculated using the $z(V)$ spectra shown in Fig. 4.13(a). For each curve, the electric field at 6V is almost twice that at 2V. This suggests that if the blue shift observed in the STS and field emission spectra of thin SOI were due to the tip induced field, then the shift observed would be voltage dependent. In that case, the voltage spacing, for example, between the σ^* peak and the P1 for 12 nm SOI would be higher than that for the 45 nm SOI. A lack of such a bias dependent non-linearity in the peak-shift in Fig. 4.6(b), establishes that the blue shift in the STS and field emission spectra is not due to the tip induced band bending.

4.10 Spreading resistance

At this point it is clear that the dopant concentration profile in SOI and the charge depletion at the SOI/BOX interface results in higher film resistivity in progressively thinned SOI. The drastic change in the film resistivity below 16 nm and a blue shift in the STS and field emission spectra below 16 nm, seems to be related. Even though the factors such as the sample resistance, changing work function and the tip induced band bending may have some contribution to the STS blue shift, we now understand that these factors alone cannot explain the magnitude of blue shift observed in this work. Another factor that could result in a huge series resistance in STM measurements is the spreading resistance, which is directly proportional to the resistivity of the sample. Since the thinner SOI have a higher resistivity, the contribution of the spreading resistance is also bound to increase for these thinned samples. The following section quantitatively analyses the sensitivity of STM, STS and field emission spectroscopy to spreading resistance in SOI device layers.

Fig. 4.14(a) shows a schematic of various resistive components of an STM and the model for the tunneling current circuit proposed by M. B. Johnson et al., [7] including the spreading resistance in the STM circuit. Spreading resistance R_{SP} arises

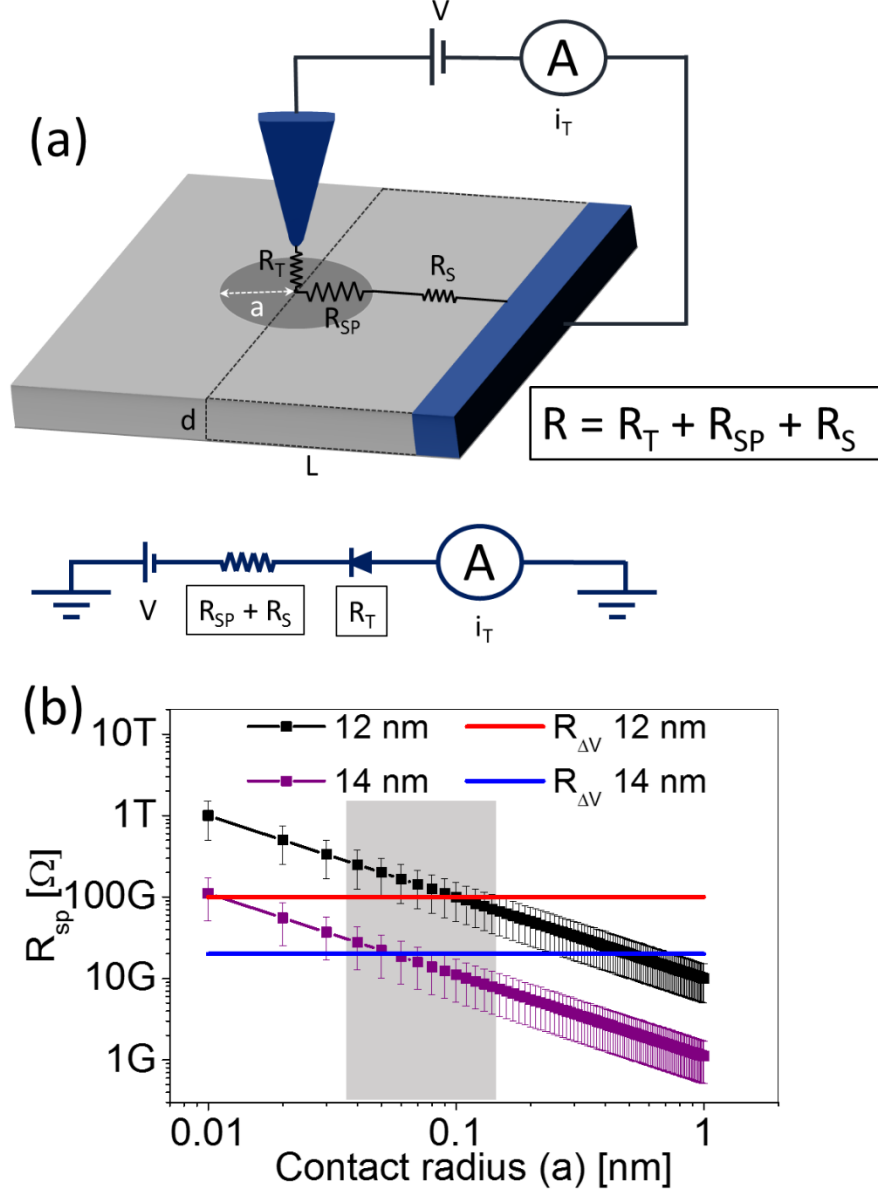


Fig. 4.14: Schematic representation of tunneling in STM demonstrating the tip position over the sample, the effective tunneling area and the resistive components such as tunneling resistance (R_T), spreading resistance (R_{SP}) and sample resistance (R_S). The effective tunneling area is indicated by the shaded circle on the sample. A schematic representation of the STM circuit model¹ is also presented. (b) The graph compares R_{SP} calculated from the spreading resistance model with $R_{\Delta V}$, the resistance calculated from the voltage blue shift observed in STM and STS. R_{SP} calculated from the spreading resistance for 14 nm (purple) and 12 nm (black) SOI is plotted on a log scale with respect to the contact aperture radius. $R_{\Delta V}$ is shown in blue and red for 14 nm and 12 nm, respectively.

due to the current spreading radially out into the “bulk” of the sample from the point of ‘contact’ on the surface [8]. R_{SP} depends on the size of the contact and the resistivity ρ of the sample. The relation is given by

$$R_{SP} = \frac{\rho}{4a} \quad 4.2$$

where a is the radius of the circular “contact” area [8]. R_{SP} causes up to 80% of the potential drop to occur within a distance of $5a$ from the point of contact in the sample [33]. In a typical STM sample holder configuration, R_S and R_{SP} along with R_T adds up in series to give a total resistance R (see Fig 4.14(a)). In an STM operation on a conductive sample, the voltage drop in the circuit is predominantly due to the tunneling resistance between the STM tip and the surface of the sample. Therefore the tunneling resistance R_T , which is typically between 1 and 200 G Ω , supersedes all other resistances in the circuit. However, for a high resistivity sample, spreading resistance becomes comparable with the tunneling resistance and therefore results in a significant voltage drop in the sample locally near the tip, potentially causing the spectral shifts found in Fig. 4.6(b). Fig. 4.14(b) compares R_{SP} calculated using the ρ obtained from 4-point probe resistivity and $R_{\Delta V}$ calculated using

$$R_{\Delta V} = \frac{\Delta V}{I} \quad 4.3$$

Where $R_{\Delta V}$ is the resistance calculated from the voltage shift (ΔV) observed in STM and STS measurements and I is the tunneling set-point current. The tunneling contact area a depends on the STM setpoint parameters and the shape of the tip, making it challenging to determine the exact value. Hence, in Fig. 4.14(b), R_{SP} is calculated for 14 nm (purple) and 12 nm (black) SOI using different values of a from 0.1 Å to 10 Å. R_T calculated for 14 nm SOI (blue) is around 20 G Ω and increases to between 75 G Ω – 100 G Ω for a 12 nm sample (red). It can be noted that R_T overlaps with R_{SP} for the contact radius between 0.6 Å – 2 Å so that the effects observed in STS and emission spectra (Fig. 4.4(a)) can indeed be accounted for by the spreading resistance [9]. These data suggests that for sample resistivity above ~ 1 Ωcm , STM can be extremely sensitive to factors such as doping concentration, depletion and resistivity.

4.11 Annealing and dopant re-distribution

In order to verify the results presented above, STM and STS measurements were repeated on SOI device layers with higher dopant concentration. A higher concentration of dopants in thinned SOI was achieved via two different processes: annealing original 45 nm SOI prior to thinning and ion implantation of thinned SOI. The original 45 nm doped SOI, whose dopant distribution profile is shown in Fig. 4.9, was annealed to allow redistribution of the dopants before thinning. Annealing led to redistribution (see Fig. 4.15) of the dopants, and also segregation at the SOI/BOX interface. This resulted in a higher carrier concentration near the SOI/BOX interface. More carriers at the interface reduced the depletion caused by the interface trap states and this resulted in a low resistivity in the thinned SOI. Alternatively, low resistivity in ultra-thin (≤ 12 nm) SOI was obtained by ion implantation of a high dose of dopants in the thinned films.

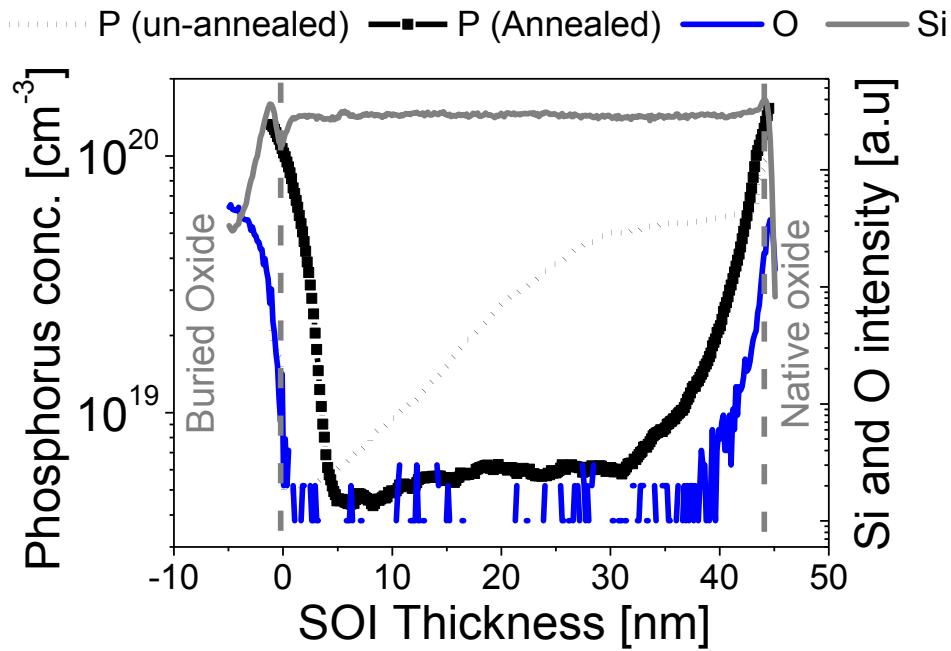


Fig. 4.15: Phosphorus concentration (black curve) of 45 nm SOI film recorded with SIMS depth analysis following ten anneal cycles at 750 °C. Oxygen (blue) and silicon (grey) profile is also shown for reference.

A shallow doped silicon with a layer of oxide on the surface, when annealed above 550 °C, results in pile-up of dopants on the silicon side of the Si-SiO₂ interface [34-36]. Fig. 4.15 shows the SIMS DP analysis for Si (grey), P (black) and O (blue) in

the device layer of the 45 nm SOI sample following ten anneal cycles at 750 °C, each of 60 seconds duration. The dotted curve shown in Fig. 4.15 is the DP of P obtained from the sample before annealing. The dotted lines indicate the two interfaces of SOI. The thin SOI is sandwiched between two oxide interfaces and the SIMS DP of P in the annealed sample shows a high level of segregation at both the interfaces. The concentration profile in the middle of the film is almost flat and below $6 \times 10^{19} \text{ cm}^{-3}$. The integral of the DP of P, before and after annealing, is around $1.33 \times 10^{21} \text{ cm}^{-3}$ and $8.62 \times 10^{20} \text{ cm}^{-3}$, respectively. The difference in the total dopant concentration in the film before and after annealing is low. Nevertheless, the difference in the dopant concentration could be due to (a) dopant loss from the film due to sublimation through the silicon surface during annealing [37] (b) error in the measurements and calculation. It is however beyond the capability of the resolution of the SIMS instrument used in this experiment to accurately determine the difference.

Generally, segregation has an adverse effect on the electrical properties of silicon [38, 39]. Dopants tend to accumulate at the interface and form clusters. Since clusters are not located on the silicon lattice sites, they do not increase the mobile

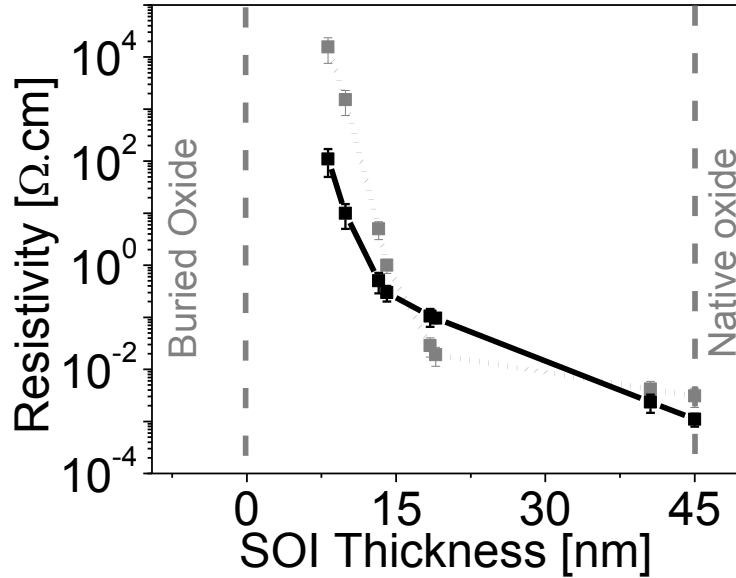


Fig. 4.16: Four point resistivity of SOI thinned after 10 anneal cycles at 750 °C (black solid), plotted as a function of device layer thickness. The grey dotted curve shows the SOI resistivity of SOI thinned without annealing, shown here for comparison.

charge density [40]. Therefore, accumulation and clustering leads to inactivation of dopants, termed as dose loss [38-40]. Dose loss in SOI results in a higher film resistivity [38, 39]. However, some studies [36, 41] have also shown that dose loss in annealed phosphorous is partially reversible. It is reported that annealing for an extended period of time [36] or multiple annealing cycles [41], results in reversal of dose loss, this process has been termed as detrapping. The interface trap at the SOI/BOX interface leads to a depletion of charge carriers in the film [5, 28, 42-44], which results in higher film resistivity [28, 42-44]. Having a higher carrier concentration near the interface could possibly lower the depletion length and increase the film conductivity. A multiple annealing cycle, similar to that adopted in this work, could result in a higher detrapping of the segregated dopants, which could lead to a higher number of charge carries at the interface. The detrapping of segregated dopants in SOI could lower the resistivity of the film.

Fig. 4.16 shows a semi-log scale resistivity plot as a function of device layer thickness for SOI thinned after annealing (black solid). For the sake of comparison, the resistivity plot of un-annealed samples is also shown (dotted grey) in Fig. 4.16. The graph clearly suggests a drastic change in the resistivity profile in the SOI after annealing. Resistivity of annealed SOI is significantly lower below 15 nm, with over 2

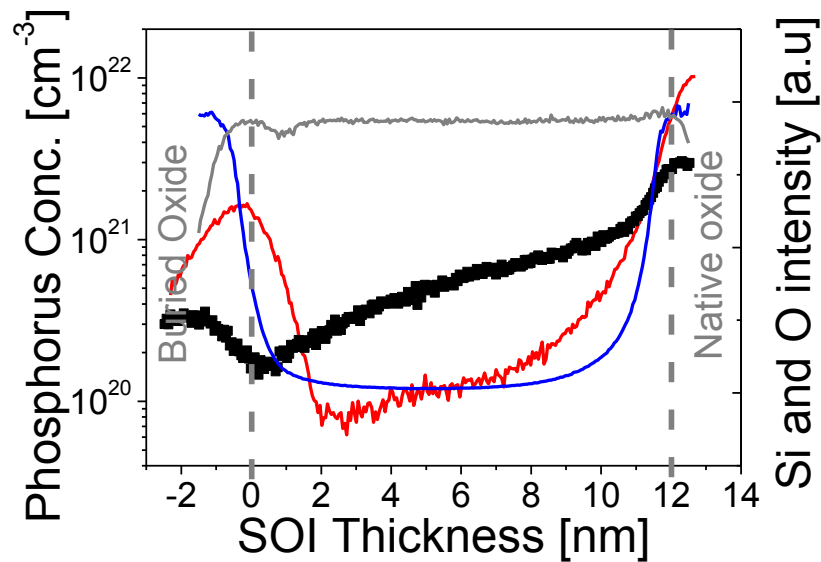


Fig. 4.17: Phosphorus concentration for, as doped un-annealed (black curve) and annealed (red) 12 nm SOI recorded with SIMS depth analysis. Oxygen (blue) and Silicon (grey) profile is also shown for reference.

orders of magnitude difference between the two data below 10 nm. The values are also lower above 35 nm. However, between 15 nm – 35 nm, the resistivity of annealed SOI is higher than for the un-annealed samples. This resistivity profile supports the SIMS DP of phosphorous in annealed SOI (Fig. 4.15), with dopants segregated at the two interfaces. As the device layer is thinned, a large amount of dopants segregated at the SOI/native oxide interface are lost and the resistivity increases in comparison to un-annealed SOI which has a higher concentration at its centre. The carrier concentration in thinner SOI are limited by the depletion caused by the interface traps. Since annealing leads to a pileup of dopants at the SOI-BOX interface, annealed SOI with thicknesses below 15 nm have higher carrier concentrations and lower resistivity than un-annealed samples. These results also suggest that multiple annealing cycles could facilitate detrapping of the segregated dopant and reduce the resistivity of the film.

Low resistivity ultra-thin SOI samples were also obtained by ion implantation of thin SOI wafers. Fig. 4.17 shows the SIMS DP analysis for Si (grey), P (black) and O (blue) in the 12 nm device layer. The red curve in the graph shows the phosphorous DP following annealing at 750 °C for 60 seconds. The SOI wafers were annealed and thinned to various thicknesses down to 5 nm for resistivity and STM analysis. The resistivity of a 10 nm and a 5 nm SOI were $2 \times 10^{-3} \text{ cm}^{-3}$ and $1 \times 10^{-2} \text{ cm}^{-3}$, respectively.

4.12 STM and STS of < 12 nm SOI

Annealed SOI thinned down to 12 nm were studied with STM, STS and field emission spectroscopy to check the effects of spreading resistance. No voltage drop or shift in STS peaks were observed for these samples. Further measurements were also carried out on SOI samples with various thicknesses of 10 nm, 8 nm and 5 nm by thinning the 12 nm ion implanted SOI device layer. Fig. 4.18(a) shows a plane fit STM image recorded on a 5 nm SOI surface with 0.5 V bias and a current set-point of 20 pA. The image and the bias stability conditions are identical to that found on bulk Si(100) [2]. Fig. 4.18(b) and 4.18(c) compare the tunneling spectra and field emission spectra recorded on the 5 nm SOI (black) and a bulk Si surface (grey). The STS spectra for the 5 nm SOI are essentially identical to that of the bulk Si (100). These results demonstrate that with sufficient doping the effect of spreading resistance can be minimised to investigate the electronic structure of 5 nm thick device-layers.

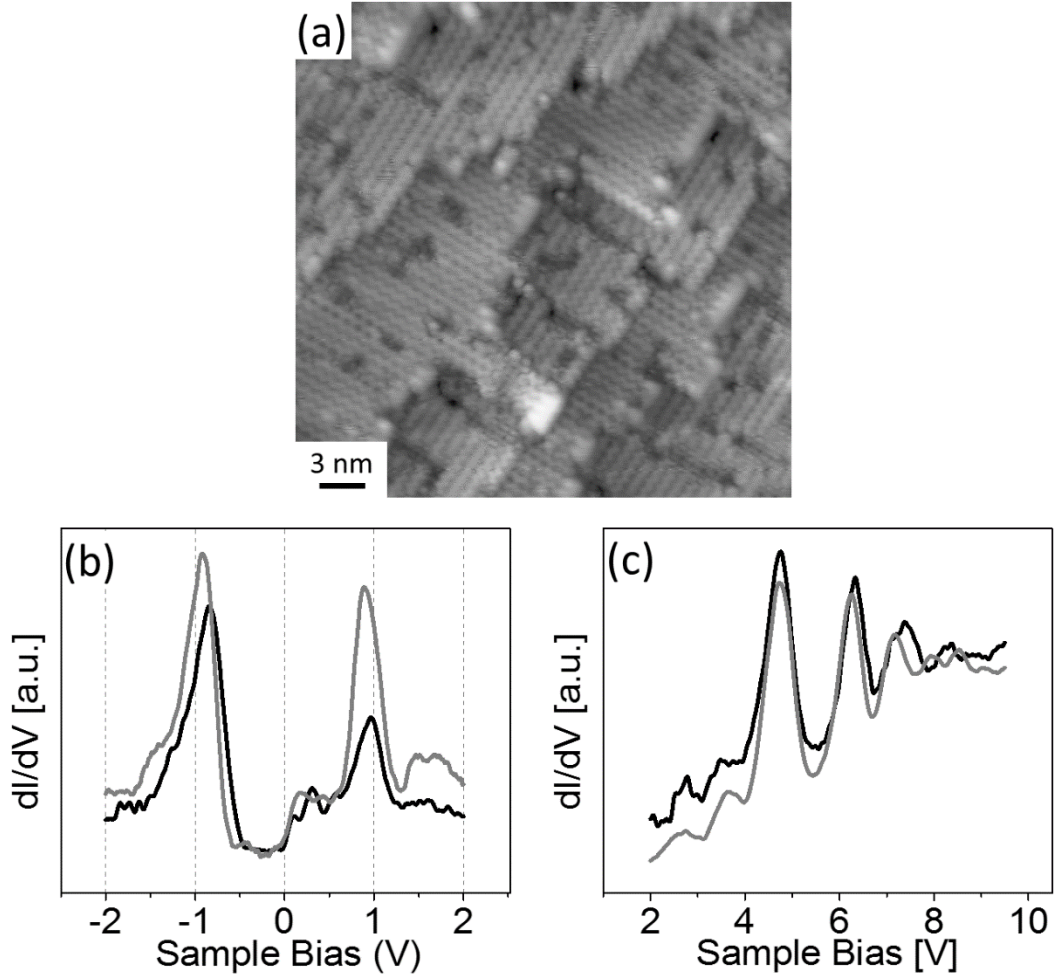


Fig. 4.18: Scanning tunneling microscopy and spectroscopy of 5 nm SOI. (a) STM image of the surface state recorded at 0.5 V and 20 pA current shows the dangling bonds (also shown in Fig. 4). (b) and (c) shows the tunneling and field emission spectra respectively. Spectra plotted in grey are for bulk Si.

4.13 Conclusion

Si(100) device layers with different n-type doping concentration were studied by scanning tunneling microscopy, spectroscopy and field emission spectroscopy. SOI device layers with varying doping-levels were obtained by thinning an ion implanted 45 nm thick SOI. The dopant profile of the SOI was obtained using *ex-situ* SIMS. The effects of thinning annealed and un-annealed SOI on the electrical properties were studied with 4-point probe resistivity measurements. Further, thinned SOI was characterized with STM. A voltage shift in the position of the features in tunneling and

field emission spectra was observed as a function of the doping concentration in the device layer.

A STM technique was established to identify the shifted spectral features of Si(100) surface. A clean Si(100) (2×1) surface has the empty state π^* and σ^* bands at around +0.3 V and +0.8 V above the Fermi level, respectively. STM bias voltage corresponding to π^* and σ^* bands show zig-zag dangling bonds or bean shaped back bonds, respectively. The topographic phase transition observed by switching the STM bias voltage between the two empty state bands was used to identify the shifted spectral features in the thinned SOI. Additionally, the shift observed in the field emission spectra was compared with the work function measured through *ex situ* kelvin probe microscopy. The work function as a function of doping level in the thinned SOI device layer was determined with a Pt coated AFM tip with respect to a gold reference. The KPM data showed a clear variation in the work function along the thickness of the device layer but this variation was almost insignificant in comparison to the voltage shift observed in the field emission spectra. The KPM asserted that shifts observed in field emission spectra were not a result of work function variation in the device layer.

Effects of tip-induced field on band bending in a Si(100) (2×1) surface was discussed in context of the blue shift observed in STM and STS. It was shown that the pinning of the Fermi level and surface states of a Si(100) (2×1) surface limits the tip-induced field effects to less than 0.8 V. Furthermore, the role of spreading resistance due to the extremely small tunneling contact in STM, combined with the high resistivity of the device layer was discussed. A comparison of the spreading resistance value calculated using the electrical resistivity data and the voltage blue shift observed in STM/STS showed a good match corresponding to a contact radius of between 0.4 Å – 1.5 Å. These results asserted the sensitivity of STM, STS and the field emission spectroscopy to spreading resistance in Si(100) ultra-thin SOI. The correlation between the dopant concentration and the voltage shift measured in STM and STS were demonstrated and the blue shift in the spectral and image features were shown to be due to the spreading resistance. Incidentally, application of STM and STS to study the dopant concentration in the range of 10^{13} - 10^{16} cm⁻³ in Si(100) was also demonstrated.

In order to verify these findings and also to study size effects in ultra-thin SOI, the experiments discussed above were repeated on less than 12 nm heavily doped (10^{20} cm^{-3}) SOI. The STM and STS of 5 nm SOI showed no significant role of tip-induced band bending or the spreading resistance. Subsequently, it's observed that an SOI film with device layer thickness down to 5 nm characterized with an LT-STM and STS behaves bulk like showing STS and ER spectra features very similar to bulk silicon.

4.14 References

1. Neddermeyer, H., *STM studies of nucleation and the initial stages of film growth*. Critical Reviews in Solid State and Materials Sciences, 1990. **16**(5): p. 309-335.
2. Kubby, J.A. and J.J. Boland, *Scanning tunneling microscopy of semiconductor surfaces*. Surface Science Reports, 1996. **26**(3): p. 61-204.
3. Jang, H., et al., *Quantum Confinement Effects in Transferrable Silicon Nanomembranes and Their Applications on Unusual Substrates*. Nano Letters, 2013. **13**(11): p. 5600-5607.
4. Zhang, P., et al., *Electronic transport in nanometre-scale silicon-on-insulator membranes*. Nature, 2006. **439**(7077): p. 703-706.
5. Lin, K.C., et al., *Surface characterization of silicon on insulator material*. Applied Physics Letters, 1998. **72**(18): p. 2313-2315.
6. Sutter, P., W. Ernst, and E. Sutter, *Scanning tunneling microscopy on ultrathin silicon on insulator (100)*. Applied Physics Letters, 2004. **85**(15): p. 3148-3150.
7. Johnson, M.B. and J.M. Halbout, *Scanning tunneling microscopy and spectroscopy for studying cross-sectioned Si(100)*. Journal of Vacuum Science & Technology B, 1992. **10**(1): p. 508-514.
8. Mazur, R. and D. Dickey, *A spreading resistance technique for resistivity measurements on silicon*. Journal of the electrochemical society, 1966. **113**(3): p. 255-259.
9. Barimar, P.S.N., et al., *Spreading resistance at the nano-scale studied by scanning tunneling and field emission spectroscopy*. Applied Physics Letters, 2017. **110**(26): p. 263111.
10. Jäger, N.D., et al., *Scanning tunneling microscopy and spectroscopy of semi-insulating GaAs*. Physical Review B, 2002. **65**(19): p. 195318.
11. Maboudian, R., et al., *Tunneling spectroscopy on the GaAs(110) surface: Effect of dopant concentration*. Surface Science, 1992. **275**(1): p. L662-L668.
12. Feenstra, R.M. and J.A. Stroscio, *Tunneling spectroscopy of the GaAs(110) surface*. Journal of Vacuum Science & Technology B, 1987. **5**(4): p. 923-929.

13. McEllistrem, M., et al., *Electrostatic sample-tip interactions in the scanning tunneling microscope*. Physical Review Letters, 1993. **70**(16): p. 2471-2474.
14. Barimar, P.S.N., et al., *Study of the effect of thermal treatment on morphology and chemical composition of silicon-on-insulator*. Journal of Vacuum Science & Technology B, 2016. **34**(4): p. 041806.
15. Naydenov, B. and J.J. Boland, *Variable-height scanning tunneling spectroscopy for local density of states recovery based on the one-dimensional WKB approximation*. Physical Review B, 2010. **82**(24): p. 245411.
16. Becker, R.S., J.A. Golovchenko, and B.S. Swartzentruber, *Electron Interferometry at Crystal Surfaces*. Physical Review Letters, 1985. **55**(9): p. 987-990.
17. Binnig, G., et al., *Tunneling Spectroscopy and Inverse Photoemission: Image and Field States*. Physical Review Letters, 1985. **55**(9): p. 991-994.
18. Hla, S.-W., *Scanning tunneling microscopy single atom/molecule manipulation and its application to nanoscience and technology*. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2005. **23**(4): p. 1351-1360.
19. Hla, S.-W., et al., *Single-Atom Extraction by Scanning Tunneling Microscope Tip Crash and Nanoscale Surface Engineering*. Nano Letters, 2004. **4**(10): p. 1997-2001.
20. Chadi, D.J., *Atomic structure of reconstructed group IV and III-V semiconductor surfaces*. Ultramicroscopy, 1989. **31**(1): p. 1-9.
21. Jung, T., Y.W. Mo, and F.J. Himpsel, *Identification of Metals in Scanning Tunneling Microscopy via Image States*. Physical Review Letters, 1995. **74**(9): p. 1641-1644.
22. Lin, C.L., et al., *Manifestation of work function difference in high order Gundlach oscillation*. Phys Rev Lett, 2007. **99**(21): p. 216103.
23. Ploigt, H.-C., et al., *Local work function changes determined by field emission resonances: NaCl/Ag(100)*. Physical Review B, 2007. **76**(19): p. 195404.
24. Ruffieux, P., et al., *Mapping the electronic surface potential of nanostructured surfaces*. Phys Rev Lett, 2009. **102**(8): p. 086807.

25. Kim, T.-Y., et al., *Quantum confinement effect of silicon nanocrystals in situ grown in silicon nitride films*. Applied Physics Letters, 2004. **85**(22): p. 5355-5357.
26. Sze, S.M. and K.K. Ng, *Physics of semiconductor devices*. 2006: John Wiley & Sons.
27. Ndoye, C., T. Liu, and M. Orlowski, *Comparison of Diffusion Mechanisms in Si Bulk, Nanomembranes, and Nanowires*. ECS Transactions, 2011. **33**(31): p. 3-18.
28. Zhang, P., et al., *Electronic transport in nanometre-scale silicon-on-insulator membranes*. Nature, 2006. **439**(7077): p. 703-706.
29. Kaiser, W.J., et al., *Scanning tunneling microscopy characterization of the geometric and electronic structure of hydrogen-terminated silicon surfaces*. Journal of Vacuum Science & Technology A, 1988. **6**(2): p. 519-523.
30. Weimer, M., J. Kramar, and J.D. Baldeschwieler, *Band bending and the apparent barrier height in scanning tunneling microscopy*. Physical Review B, 1989. **39**(8): p. 5572-5575.
31. Jäger, N.D., et al., *Importance of carrier dynamics and conservation of momentum in atom-selective STM imaging and band gap determination of GaAs(110)*. Physical Review B, 2003. **67**(16): p. 165327.
32. Himpsel, F.J. and T. Fauster, *Probing valence states with photoemission and inverse photoemission*. Journal of Vacuum Science & Technology A, 1984. **2**(2): p. 815-821.
33. Grasserbauer, M., H.W. Werner, and P. Paufler, *Analysis of Microelectronic Materials and Devices*. John Wiley & Sons, Chichester-New York-Brisbane-Toronto-Singapore 1991. ISBN 0-471-91713-3. Crystal Research and Technology, 1993. **28**(1): p. 118-118.
34. Berg, J.A.V.d., et al., *Characterization by medium energy ion scattering of damage and dopant profiles produced by ultrashallow B and As implants into Si at different temperatures*. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2002. **20**(3): p. 974-983.

35. Oshima, M., et al., *Resonant Auger electron spectroscopy for analysis of the chemical state of phosphorus segregated at SiO₂/Si interfaces*. Journal of Electron Spectroscopy and Related Phenomena, 1998. **88**: p. 603-607.
36. Kasnavi, R., et al., *Characterization of arsenic dose loss at the Si/SiO₂ interface*. Journal of Applied Physics, 2000. **87**(5): p. 2255-2260.
37. Sato, Y., K. Imai, and N. Yabumoto, *Phosphorus pileup and sublimation at the silicon surface*. Journal of The Electrochemical Society, 1997. **144**(7): p. 2548-2551.
38. Shibahara, K., et al., *Dopant loss origins of low energy implanted arsenic and antimony for ultra shallow junction formation*. MRS Online Proceedings Library Archive, 1998. **532**.
39. Meishoku, K., et al., *Quantitative Evaluation of Dopant Loss in 5–10 keV As Ion Implantation for Low-Resistive, Ultrashallow Source/Drain Formation*. Japanese Journal of Applied Physics, 1999. **38**(4S): p. 2324.
40. Pei, L., *Dopant Segregation at Silicon-Oxide Interfaces*. 2007.
41. Griffin, P.B., S.W. Crowder, and J.M. Knight, *Dose loss in phosphorus implants due to transient diffusion and interface segregation*. Applied Physics Letters, 1995. **67**(4): p. 482-484.
42. Scott, S.A., et al., *Influence of Surface Chemical Modification on Charge Transport Properties in Ultrathin Silicon Membranes*. ACS Nano, 2009. **3**(7): p. 1683-1692.
43. Zhao, X., et al., *Influence of surface properties on the electrical conductivity of silicon nanomembranes*. Nanoscale Research Letters, 2011. **6**(1): p. 402-402.
44. Pengpeng, Z., et al., *Electrical conductivity in silicon nanomembranes*. New Journal of Physics, 2006. **8**(9): p. 200.

5

THERMAL STABILITY OF ULTRA-THIN SOI

The evolution of the morphology of silicon-on-insulator (SOI) due to annealing in an UHV environment was investigated. Thin SOI film deforms at high temperatures into 3D crystals in a process known as dewetting. The process is driven by surface energy minimization and occurs via surface diffusion. The dewetting process in SOI is known to start with nucleation of voids in the film and grows via capillary edge and Rayleigh instabilities. In this work, preliminary measurements have suggested that SOI with thicknesses below 4 nm dewets spontaneously through a process that involves thermally driven fluctuations of the film thickness. STM measurements have shown that annealing 3 nm SOI films produces low energy facets along with a wave-like modulation of the surface roughness. Supporting evidence has also been obtained from SEM and AFM measurements, which show the presence of thickness fluctuations in the film which is known to be characteristic of films dewetting via the growth of thermal fluctuations. Finally, KPM measurements show clear evidence of the presence of an ultra-thin wetting layer between the dewetting crystals during dewetting of a 3 nm SOI film, consistent with the emergence of a new dewetting mechanism at these thicknesses.

5.1 Introduction

The thermal stability of thin films is of pronounced technological importance [1-3]. Thin films and nanostructures are extensively used in making devices such as CMOS, FET, solar cells, sensors, etc., and fabrication of devices usually involves high temperature processing. Thin films are frequently metastable and their shape usually changes following thermal treatment [2]. A 2D film agglomerates into 3D crystal islands, exposing the underlying substrate layer when heated to sufficiently high temperatures [1, 2, 5]. This phenomenon, when it occurs, is known as dewetting and is driven by surface energy minimization and usually occurs well below the melting point of the film [2]. Dewetting is important for SOI based technologies since the Si device layer has a significantly higher surface energy than the BOX.

Surface studies of SOI film is complicated by the presence of the thermal oxide that caps the device layer. A study of SOI requires removal of this protective oxide layer known as native oxide [6-9]. In UHV, the oxide layer is desorbed through a thermal annealing process [6, 7, 9]. Once the native oxide has been removed from SOI, the Si device layer will undergo dewetting behaviour under certain thermal conditions, peeling back the device layer to uncover the BOX. There are many literature reports of dewetting occurring for SOI device layers [2, 10-18]. Thermal oxide desorption in SOI starts at around 750 °C [9, 19] and the process does not depend on the thickness of SOI. However, the onset temperature of dewetting is known to decrease with the thickness of SOI [13, 19, 20]. In the case of ultra-thin SOI, the dewetting temperature gets closer to the oxide desorption temperature, complicating the thermal processing of these films since desorption and dewetting processes are in competition.

Annealing of ultra-thin SOI also leads to interesting and unexpected behaviours. STM measurements on 3 nm SOI have shown that annealing leads to faceting of the film and an increase in surface roughness. Also, crystals formed due to dewetting of the ultra-thin film have a lower contact angle compared to that found for thicker films. Further, analysis has shown the presence of wave-like surface patterns on the ultra-thin SOI following annealing, similar to that reported

for polymer and metal films [21-28], and the existence of a wetting layer that physically and electrically connects the dewetting crystals – phenomena that is not seen in the case of thicker SOI. We suggest that SOI films with thicknesses less than 4 nm are sensitive to thermal fluctuations, which may allow the top and bottom interfaces to interact. These fluctuations modulate the film thickness, creating matter waves that ultimately lead to the formation of dewetted crystals separated by a Si wetting layer stabilised by the van der Waal interaction between these interfaces. We further suggest that this phenomenon is responsible for the presence of low energy facets and the low contact angles measured at these dewetted crystals.

5.2 Experimental details

SOI samples with device layer thickness ranging from 3 nm to 45 nm were annealed in an UHV environment with base pressure lower than 1×10^{-10} mbar. All samples were prepared from the following 3 wafers: 1) a 45 nm SOI with doping concentration of 10^{19} cm^{-3} , and BOX thickness of 145 nm, 2) a 12 nm SOI with doping concentration of 10^{15} cm^{-3} , and BOX thickness of 25 nm, and 3) a 12 nm SOI with doping concentration of 10^{20} cm^{-3} , and BOX thickness of 25 nm. Since STM measurements were possible only on conducting samples, highly doped SOI were used for all the surface measurements. Details about the initial wafer thickness of every sample are provided as discussed.

All samples were cut into standard size of 11×5 mm. Samples for dewetting studies only, were prepared by thinning the whole region of the SOI film using fluorine and oxygen plasma, as discussed in chapter 3. However, SOI samples with thicknesses less than 12 nm, used for dewetting and surface studies (STM and STS measurements), were patterned to have a reference film (10 nm) alongside a film with required thicknesses (3 – 10 nm). The 10 nm reference film was mainly used to verify the quality of the STM tip. These samples were fabricated similar to that used for the multi-thickness samples prepared for KPM measurements discussed in section 4.2 of chapter 4. However, since etching small thicknesses (2 - 6 nm) with fluorine plasma was a challenge, a KOH recipe was instead used to etch silicon. A 12 nm SOI with native oxide was covered with photoresist and rinsed

in 1% dilute HF to remove the native oxide from the unexposed region. After washing off the resist, the sample was rinsed in 30 % KOH solution for 3 – 10 s at room temperature. KOH etched about 2 – 6 nm of silicon. Samples were then treated with oxygen plasma to make sure that the surface was flat and smooth. Before loading into the UHV chamber, samples were rinsed in HF followed by oxygen passivation using H₂O₂ (technique discussed in chapter 3).

Techniques such as direct resistive heating and indirect heating on a button heater were used for the thermal treatment. Similar results were obtained from both the techniques, however, direct resistive heating technique was advantageous for thermal gradient measurements. Samples were annealed in UHV to temperatures ranging from 700 to 900 °C, for 10 – 300 s. For surface studies (STM) of ultra-thin SOI film, the annealing parameters for every individual sample had to be optimised to preserve the integrity of the film and avoid dewetting. Surface morphology of the film after annealing was investigated using Zeiss SEM, Bruker AFM and Createc STM. All Kelvin Probe Microscopy measurements were carried out in KPM mode in the Bruker Enviroscope AFM.

5.3 Surface studies of annealed ultra-thin SOI

SOI device layers of various thicknesses ranging from 45 nm to 3 nm were characterized with STM and STS. The STM measurements were carried out following *ex-situ* cleaning described in chapter 3 and flash annealing to desorb the native oxide. The effects of annealing on dopant diffusion, dopant segregation and the resulting variation in the electrical properties of the film are discussed in chapter 4. This section discusses the evolution of the surface morphology of SOI films due to annealing, especially the case of ultra-thin SOI films.

STM measurements were carried out on ultra-thin SOI with thicknesses of 12 nm, 10 nm, 8 nm, 5 nm and 3 nm. These samples were thinned from an annealed (750 °C for 60 s) 12 nm SOI doped to 10²⁰ cm⁻³. Annealing before thinning was carried out to activate the dopants and allow diffusion towards the SOI-BOX interface as discussed in section 4.11 of chapter 4. These samples were thinned using the KOH recipe discussed in the experimental section (section 5.2),

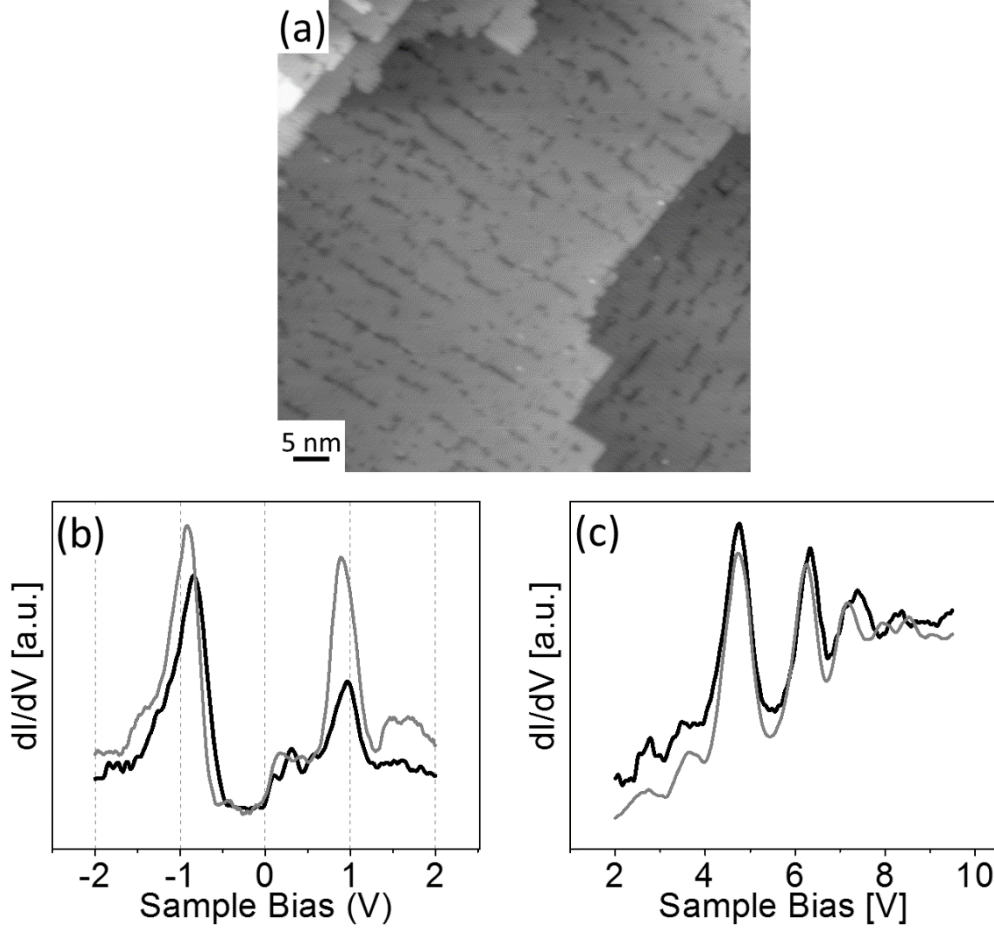


Fig. 5.1: (a) STM height image of a 5 nm SOI recorded at 2 V and 10 pA current setpoint. (b) and (c) shows the tunneling and field emission spectra, respectively, recorded on the 5 nm surface (black) and bulk Si(100) (2×1) (grey).

and flash annealed to desorb the oxide. Since flash annealing for longer times results in dewetting, a single short anneal of 30s at around 750 °C was adopted for all samples except the 3 nm one. Due to the short annealing time, most of the oxide on the surface was still intact except for the OFR (oxide free region) and STM measurements were carried out inside these OFR.

The surface morphology of the thinned samples did not appear to vary much for SOI thicknesses down to 5 nm. Fig. 5.1(a) shows a plane fit STM height image of a flash annealed 5 nm SOI, recorded with 2 V bias and a current set-point of 10 pA. The STM image shows an atomically flat surface with occasional atomic steps. The dark line defects running perpendicular to the dimer rows on the surface are the metal contaminants [29], probably caused by the dissolved metal ions in the HF bath, and which are commonly found on Si(100) surfaces. Fig. 5.1(b) and

5.1(c) shows the tunneling and field emission spectra, respectively, recorded on the 5 nm SOI (black) and the bulk Si(100) (2×1) (grey). Both tunneling and field emission spectra recorded on SOI down to 5 nm SOI were essentially identical to that of the bulk Si (100), as discussed in chapter 4.

Fig. 5.1(a) confirms that SOI with film thickness down to around 5 nm can be annealed to desorb oxide and results in an atomically flat device layer surface. The figure also suggests that the KOH etch recipe followed by oxygen plasma smoothening, used in this work, produces an atomically flat SOI surface. Due to the extremely narrow process temperature window, the STM measurements were successful only after numerous failed attempts to optimise the thermal budget. Manual loading of samples on the sample holder caused every individual sample to require slightly different annealing parameters. Further, despite all the optimization required, *ex-situ* SEM characterization of the annealed 5 nm SOI sample revealed that several regions on the film, especially at the edges had dewetted.

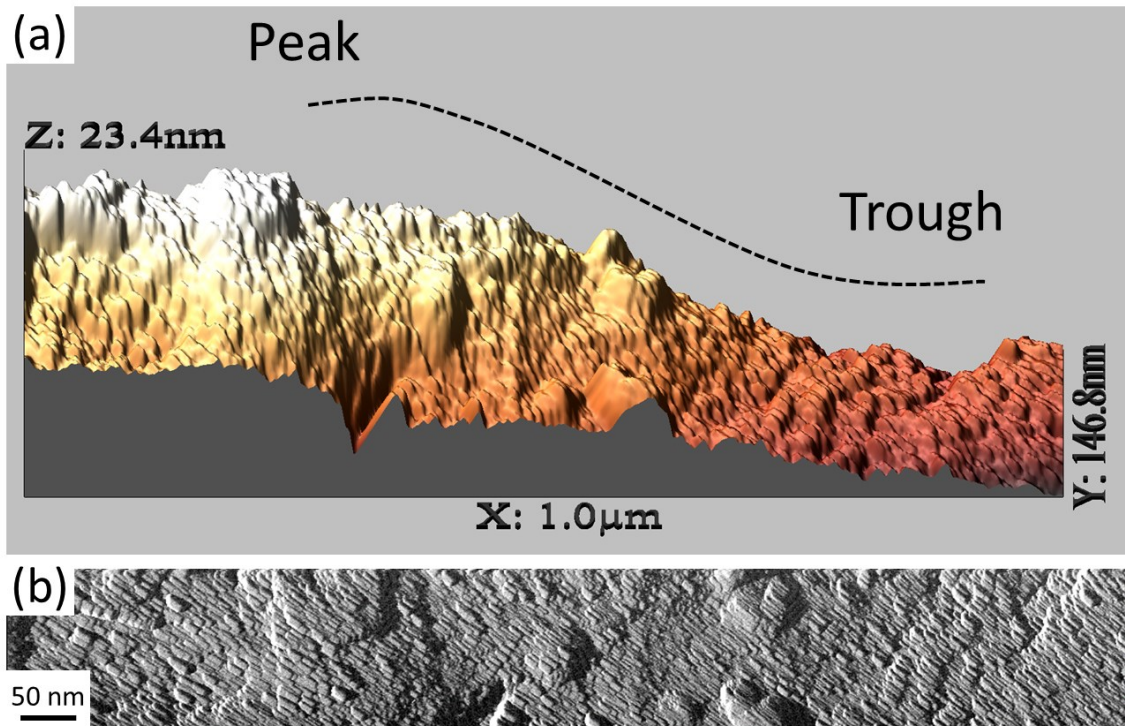


Fig. 5.2: STM image of a flash annealed 3 nm SOI. (a) shows a 3D STM height image and (b) shows the current error image. The image was recorded with 8 V and 5 pA. The STM height image shows a wave like pattern as pointed by the dotted line in (a).

Fig. 5.2(a) and 5.2(b) shows the 3D STM height and current error image, respectively, of a 3 nm SOI following flash annealing at $\sim 730^\circ\text{C}$ for 30 s. The image was recorded with 8 V bias and 5 pA current. The plane fitted STM image in Fig. 5.2(a) shows that, in contrast to the smooth surface found for the 5nm SOI film, annealing the 3nm film results in a rough surface with an average roughness of 1.5 nm (neglecting the slope) and a maximum feature height of about 23.4 nm. The 3d view of this surface reveals the presence of a wave like pattern with a peak and trough indicated by the dotted line in Fig. 5.2(a). The current error image in Fig. 5.2(b) shows the surface to be made of several rectangular terraces. The STM analysis of the 3 nm SOI confirmed that the surface remained conducting and the measurements could be carried out at biases as low as 0.5 V. Crucially, this means that despite the mass transport that is evident in Fig. 5.2(a) the SOI film has remained continuous. Furthermore, the surface profile in Fig. 5.2(a) also suggests that the ultra-thin SOI roughens during annealing forming peaks and troughs but without rupturing the film and exposing the low energy SiO_2 interface.

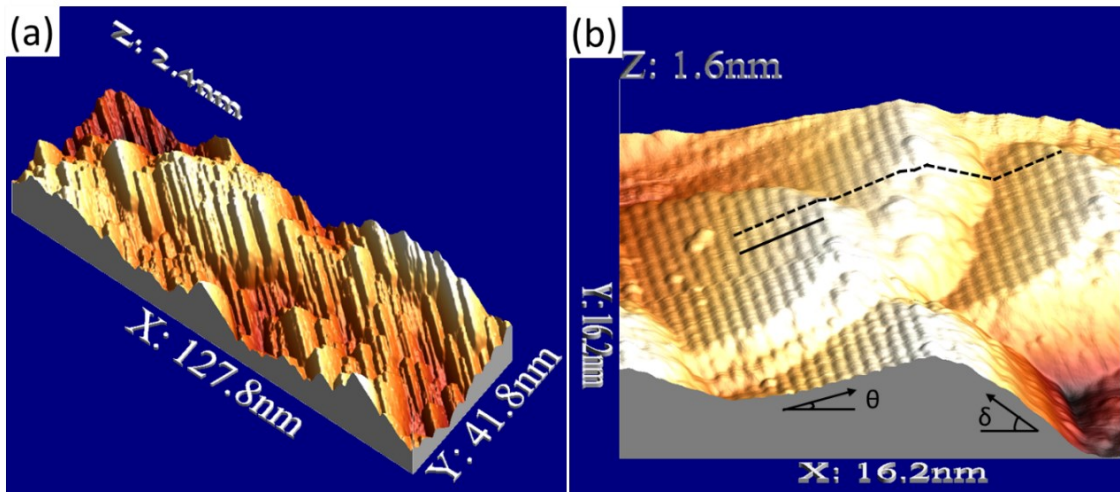


Fig. 5.3: STM 3D height images of the 3 nm SOI surface showing different surface features. (a) is recorded with set-point parameters of 2 V bias, 10 pA current. (b) is recorded with 0.5V bias and 10 pA current. (a) shows sharp rectangular terraces while (b) shows circular terraces.

To further study the surface morphology, detailed high-resolution STM images were recorded at different regions of the 3 nm SOI. Unlike the Si(100) terraces found in thicker SOI samples, the surface of the 3 nm SOI was faceted

with two kinds of terraces: a rectangular terrace and a circular terrace structure. Typical rectangular and circular terrace structures recorded at different locations are shown in Fig. 5.3(a) and Fig. 5.3(b), respectively. The STM images in Fig. 5.3(a) and (b) are recorded with biases of 2 V and 0.5 V, respectively, and a set-point current of 10 pA for both the images. The structure of the atomic rows within both the terraces was apparent when the STM bias voltage was below 2.5 V. However, both the faceted surfaces consisted of only one kind of surface domain, as shown in Fig. 5.3(b). The difference in the terrace structure is assumed to be

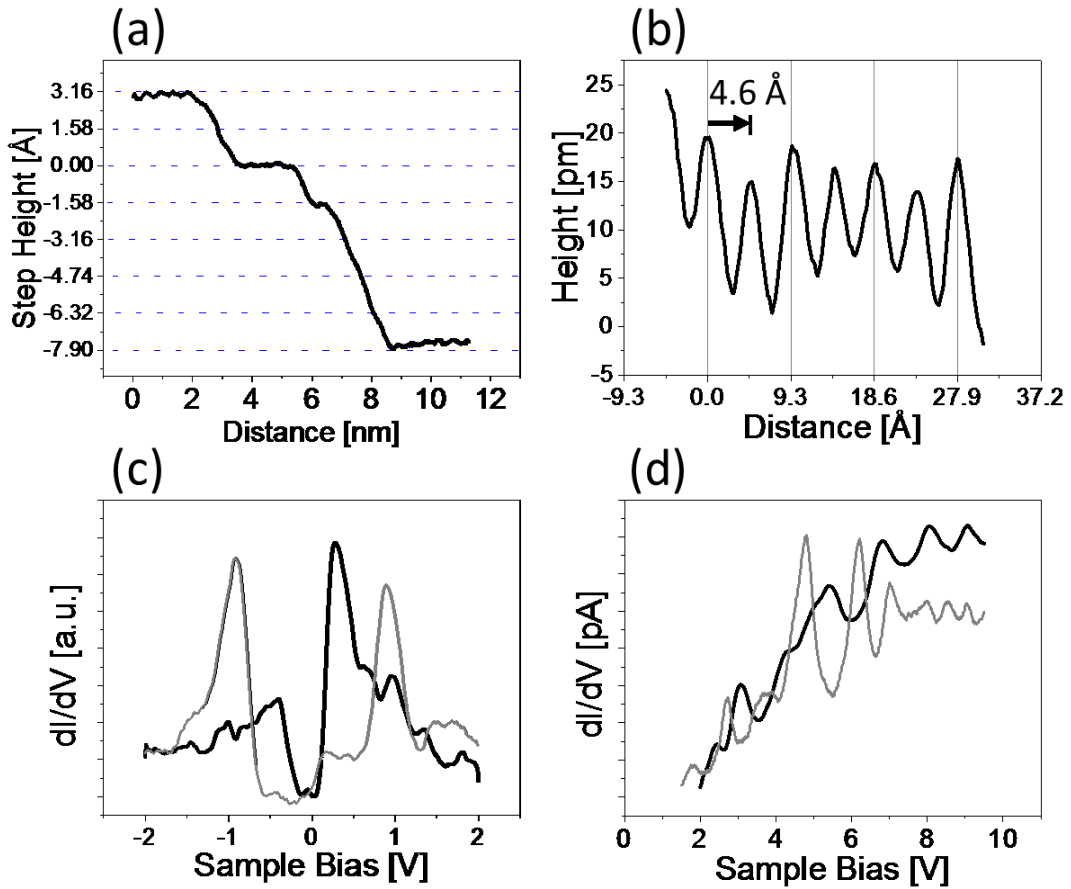


Fig. 5.4: (a) shows the line profile taken from the dotted line in Fig. 11(b). The angle offsets θ and δ are $\sim 7.3^\circ$ and $\sim 19^\circ$, respectively. (b) the line profile taken from the solid line in Fig. 11(b) showing the spacing between the rows. (a) and (b) shows the tunneling and field emission spectra, respectively, of the 3 nm SOI. Both the spectra were recorded with set-point parameters of 2 V and 20 pA current. The grey spectra in (d) is the field emission spectra recorded from a bulk Si(100) (2×1) surface. The grey spectra in (c) and (d) are the spectra recorded from the bulk Si(100) shown here for reference.

due to the annealing temperature gradient in the sample since the measurements were carried out at different locations.

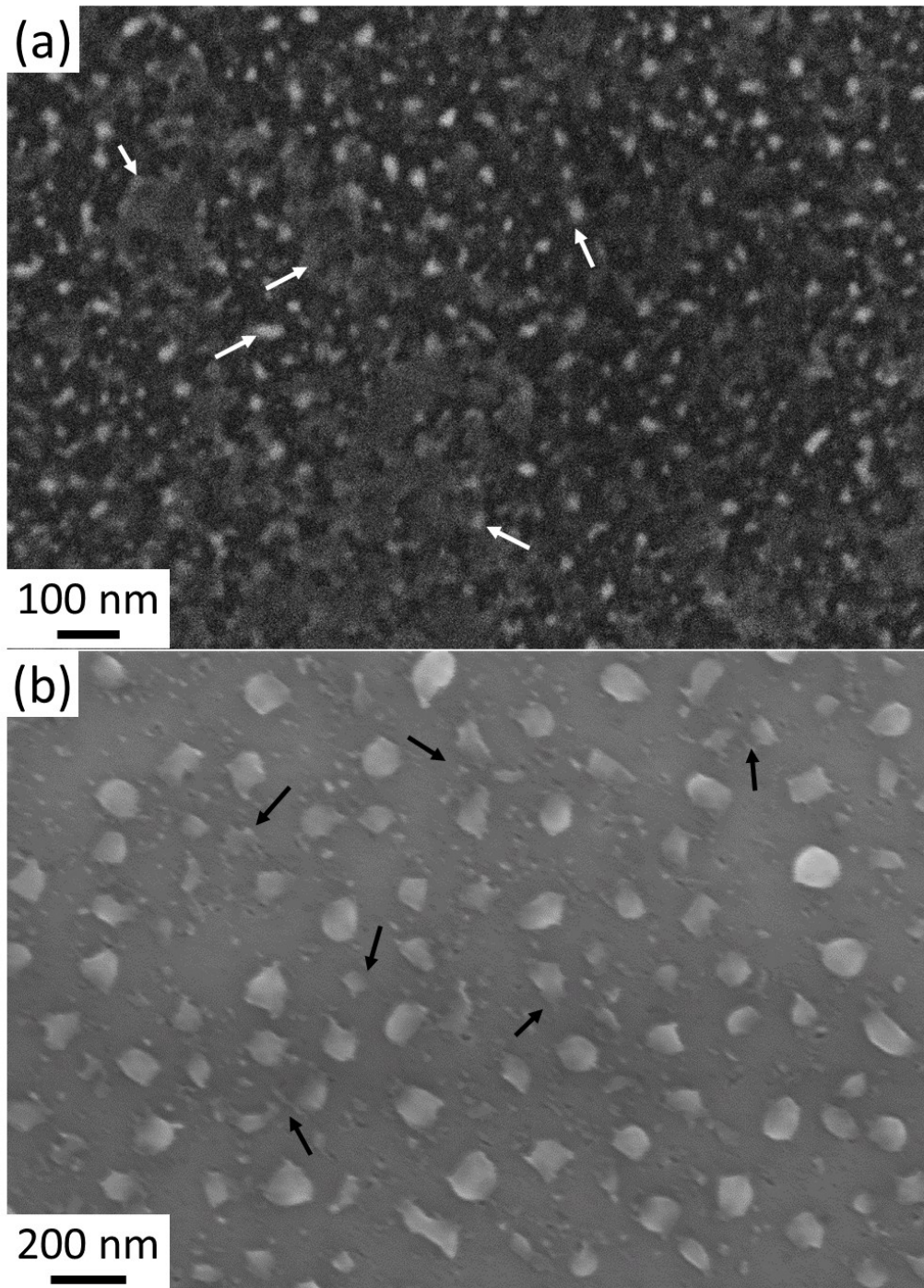


Fig. 5.5: SEM images of thickness fluctuations and dewetting captured in the same 3 nm SOI due to thermal gradient across the sample during annealing. (a) shows the initial stages where fluctuation in the film thickness can be seen (pointed with white arrows). (b) shows the dewetting crystals with tapered edges. The tapered edges are pointed with black arrows.

Fig. 5.4(a) shows the line profile extracted from the dotted line shown in Fig. 5.3(b). The profile shows bunching of steps with the single terrace step height of $\sim 1.6 \text{ \AA}$. The spacing between the atomic rows in the case of (θ) sloped terrace was around $4.6 \text{ \AA}$ (see Fig. 5.4(b)). The step height and the atomic row spacing clearly show that the terraces are not along the Si(100) plane. Fig. 5.4(c) and 5.4(d) shows the tunneling and field emission spectra recorded on the 3 nm SOI surface. The tunneling spectra showed a sharp empty state peak at $+0.25 \text{ eV}$ and a broad filled state peak at around -0.5 eV . The tunneling spectra show that the surface was semiconducting with a surface energy gap of $\sim 0.2 \text{ eV}$. The field emission spectra from the annealed 3 nm SOI film shows several sharp peaks at 3 eV, 5.4 eV, 6.8 eV, 8 eV and 9 eV. In comparison to the field emission spectra of a bulk Si(100) (2×1) surface (grey spectra in Fig. 5.4(d)), all the peaks in the spectra from the 3 nm SOI were blue-shifted by at least 0.4 eV. This blue shift in the field emission spectra could indicate a shift in the work function of the surface due to the difference in the crystal plane of the facet [30, 31].

The STM analysis showed roughening of the 3 nm film following annealing resulting in a peaks and troughs structure, in certain cases these structures are several times the thickness of the film. These observations are consistent with silicon mass transport across the film and may be a result of the thermal fluctuations that is captured during the rapid anneal process [22-28].

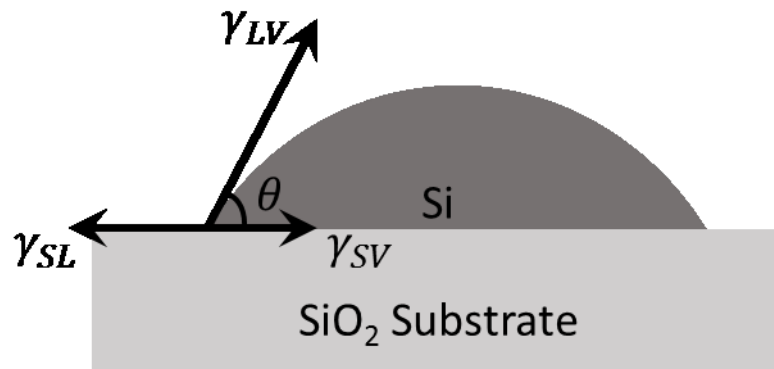


Fig. 5.6: Schematic illustration of the equilibrium contact angle considered in Young's equation[2, 4].

To check for large scale mass transport the annealed 3 nm SOI was further analysed using SEM and AFM. Due to the thermal gradient present during annealing, different stages of the dewetting process are found across the film. Fig. 5.5(a) shows a region from the cooler side of the ~ 3 nm SOI, where the surface appears uneven due to fluctuations in the film thickness. The uneven nature of the film results in a contrast difference in the SEM image. The STM data presented above was recorded from around the region shown in Fig. 5.5(a). The film fluctuations seen in the SEM image can be closely related to the peaks and troughs observed in STM. Fig. 5.5(b) shows the dewetting in the hotter region of the sample where presumably the amplitude of the thermal fluctuation is more pronounced. Here we find that some of the crystals seem to lack the anisotropy in its shape – crystal facets seem to be absent in some crystals. It can also be noted that some of the crystals have tapered edges, and appear to have reduced contact angles. We believe that the tapered edges in the crystals are because the crystals are connected with a wetting silicon layer instead of the BOX. The smaller equilibrium contact angle of the crystals could indicate a reduced surface energy of the film as shown by the Young's equation given by,

$$\cos \theta = \left(\frac{\gamma_{SV} - \gamma_{SL}}{\gamma_{LV}} \right) \quad 5.1$$

Where, γ_{SV} , γ_{SL} and γ_{LV} are the surface energies for the solid-vapor, solid-liquid and liquid-vapor interfaces, and θ is the equilibrium contact angle (see Fig. 5.6) [2, 4]. The reduction in the film's surface energy is possibly due to the restructuring of the ultra-thin film during annealing forming low energy facets, as observed in the STM analysis.

5.4 Kelvin probe microscopy of annealed 3 nm SOI

Annealing studies of patterned metal wires (carried out by other research groups), have shown that development of thermal instabilities can lead to formation of thin filaments between the dewetting crystals [32]. It is also known that rapid re-solidification can freeze-in the transient morphologies such as the fine connecting filaments [32]. In this work, we have shown that it may be possible to capture the transient morphology in the dewetting of ultra-thin SOI films where the dewetting crystals are still connected to each other through an ultra-thin

wetting film. We now show that the presence of wetting films can be detected using Kelvin probe microscopy (KPM).

The *ex-situ* KPM measurements described here were carried out immediately following UHV annealing to avoid oxidation of the wetting layer. Unfortunately, these measurements could not be carried out on the annealed 3nm SOI discussed earlier. Instead, the measurements were carried out on a different patterned sample that exposed regions of the silicon substrate beneath the BOX. This provided an important reference layer that allowed differentiation of the BOX and the Si device layer. Since the contact potential difference (CPD) in KPM can be influenced by the quality of the AFM tip, it is good to have a reference layer in the sample. For this purpose, the 3 nm SOI was patterned into a strip, with BOX etched down to the substrate on either side of the strip (as shown in the Fig. 5.7(a)). The exposed silicon substrate, was used as a reference to compare the contact potential difference. Fig. 5.7(a) and 5.7(b) shows the 3D AFM height and CPD image, respectively, of the 3 nm sample, following flash annealing at ~ 730 °C for 30 s. These *ex-situ* KPM measurements were carried out immediately following the UHV annealing.

The CPD images were acquired in the Kelvin Probe Microscopy (KPM) feature of AFM in the lift mode using a two-pass scan on electrically grounded samples. A Topography image was obtained during the first pass in tapping mode with zero tip bias. During the second pass the tip was lifted to a set distance ($h_{\text{lift}} = 30$ nm) above the sample surface while a bias voltage (V_{tip}) was applied to the tip. An alternating current (ac) voltage combined with a direct current (dc) bias was applied to the tip during the scan in lift mode, i.e., $V_{\text{tip}} = V_{\text{dc}} + V_{\text{ac}} \sin(\omega t)$ and the peak-to-peak amplitude of the V_{ac} was set to 6 V. A lock-in amplifier was used to isolate the signal while the feedback controller of the AFM adjusted the V_{dc} such that the electrostatic interactions between the tip and the sample were nullified.

While the AFM height image in Fig. 5.7(a) shows that the film has dewetted, the stability of the CPD image in Fig. 5.7(b) suggests that the crystals and the region between the crystals (which we shall refer to as the wetting layer) is

electrically conducting. In a thicker SOI, it is well known that the 2D film agglomerates into 3D crystals exposing the underlying insulating BOX [2]. Since the crystals sit over the insulating BOX, they are electrically isolated from each other and thus CPD measurements are not possible. However, in the CPD image shown in Fig. 5.7(b), crystals are not charging, indicating that the crystals are electrically connected to each other and to the grounding electrode. Furthermore, the difference in CPD of the crystals, the wetting layer and the silicon substrate, is less than 400 mV. Fig. 5.7(c) shows the height (black) and CPD (blue) line profile crossing over the Si substrate, crystals and the wetting layer, labelled in Fig. 5.7(a). CPD of the silicon substrate was used as a reference. The line profile clearly shows the CPD difference between the three entities. Interestingly, we find the CPD values were different for crystals of different sizes. To compare the relative CPD values,

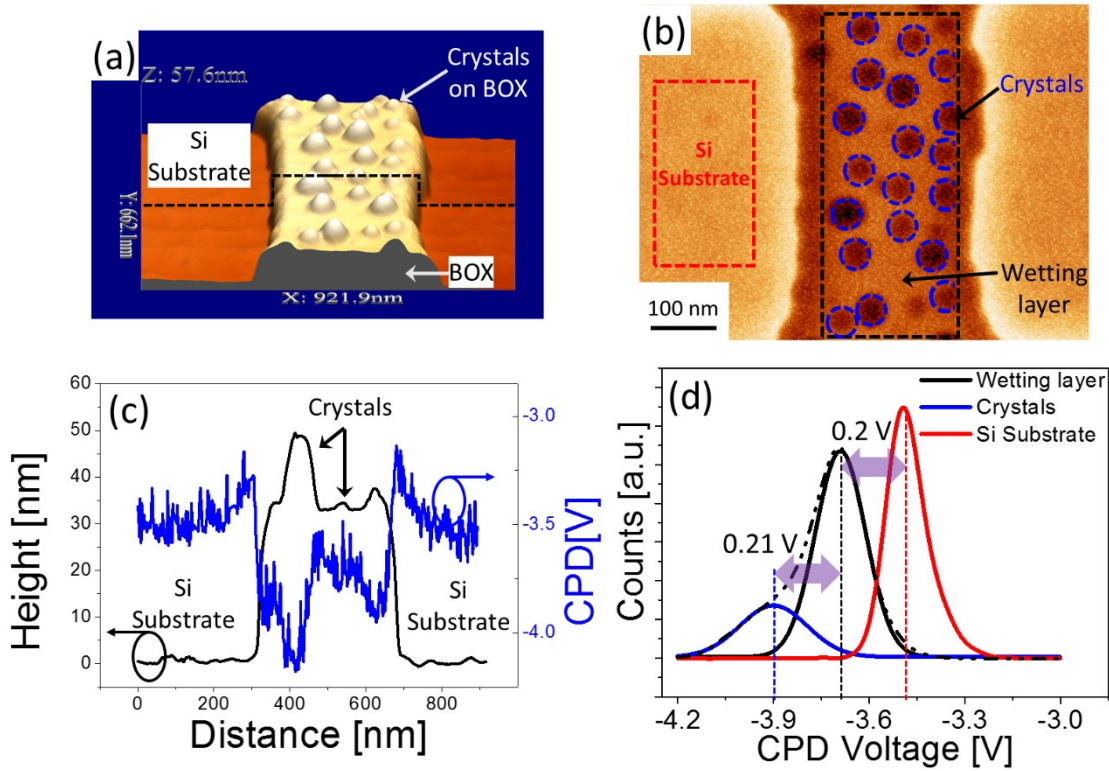


Fig. 5.7: AFM and KPM data suggesting the possibility of freezing a transient morphology in annealed ultra-thin SOI with dewetting crystals inter-connected with an ultra-thin “wetting” film. The sample was patterned into a ~ 250 nm SOI strip with BOX etched on either side to expose the Si substrate. (a) and (b) shows the 3D AFM height and CPD data, respectively. (c) shows the height and CPD line profile obtained across the line shown in (a). (d) shows the CPD histogram of the substrate (red), crystals (blue) and the “wetting” layer (black). Histogram for the crystals and the wetting layer is extracted by fitting the dotted curve shown in (d).

histograms were obtained (Fig. 5.7(d)) from the three regions in the CPD image corresponding to the substrate, crystals and the wetting layer, recorded from the areas within the red, blue and black dotted enclosures in Fig. 5.7(b). The histogram for the crystals and the wetting layer was obtained by fitting the combined data shown as a dotted curve in Fig. 5.7(d). The position of the peaks corresponding to the film and the crystals show a CPD difference of about 200 meV and 410 meV, respectively. The substrate silicon is p-type doped to 10^{15} cm^{-3} while the SOI is n-type doped to $\sim 10^{20} \text{ cm}^{-3}$. The difference in CPD values may be explained as a difference in the doping concentration of the three regions. However, the difference could also be due to the small sizes of the film and the crystals. Regardless of the precise CPD values, the KPM data confirms that the crystals are interconnected by an ultra-thin wetting layer. These results are in-line with the STM and SEM data of the ultra-thin SOI.

5.5 Different dewetting mechanisms in SOI device layer

This section presents an analysis of surface morphology following UHV annealing of SOI with film thicknesses ranging between 3 nm to 25 nm. This section also describes and further compares the two dewetting mechanisms observed in this work.

Generally, for SOI films thinner than 45 nm, annealing above 900°C encourages dewetting, the extent of dewetting however depends on the film thickness and the anneal duration. The initiation of the dewetting process in a flat and stress-free SOI film is known to occur via a substrate-exposing void nucleation process [2]. When the radius of the void reaches a critical radius ($r_{\text{void}} > r_{\text{crit}}$), there is a decrease in free energy of the system and therefore such a void grows. The activation energy required to form such a void is estimated using the equation [2]

$$\Delta G_{\text{void}} = 2\pi r_{\text{crit}} t_{\text{Si}} \gamma_{\text{Si}} = 2\pi t_{\text{Si}}^2 \gamma_{\text{Si}} \quad 5.2$$

Where, ΔG is the activation energy for creating the void with $r_{\text{void}} > r_{\text{crit}}$, (since, $r_{\text{crit}} = \frac{t_{\text{Si}}}{\sin \theta_{\text{Si}}}$; therefore $r_{\text{crit}} = t_{\text{Si}}$) t_{Si} is the thickness of SOI and γ_{Si} is the surface energy of SOI. Taking $r_{\text{crit}} = t_{\text{Si}} = 1 \text{ nm}$ and $\gamma_{\text{Si}} = 1.5 \text{ J/m}^2$ the activation energy required to homogeneously nucleate a critical void $\sim 60 \text{ eV}$ which is prohibitively large and this value further increases with the square of the SOI thickness [2]. For

this reason it is believed that homogeneous nucleation of a critical void does not occur[2, 33]. A critical void in SOI is believed to occur via a heterogeneous void nucleation mechanism at a defect site in the film.

Once a supercritical void is formed, the thermodynamic model explaining the kinetics of dewetting was developed by Danielson et al. [2]. The proposed model is a 5-stage mechanism: (1) A void is formed in the thin film, with a radius greater than a critical radius that depends on film thickness. (2) The void edge

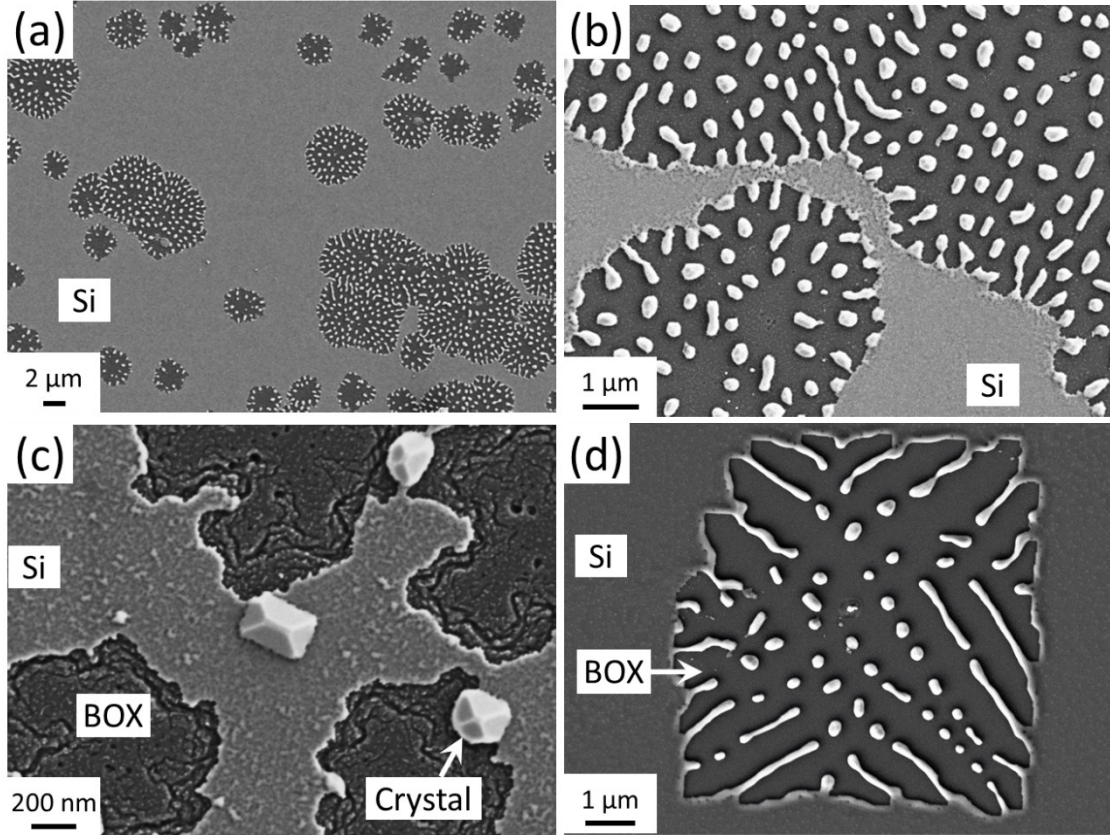


Fig. 5.8: SEM images showing different stages of dewetting of the SOI device layer. (a), (b) and (c) are for 25 nm SOI thinned from doped 45 nm and (d) is a 12 nm pristine undoped SOI.

thickens and retracts by capillary edge instability, exposing the underlying BOX. (3) The thickened void edge breaks down due to a Rayleigh instability. (4) The void edge forms uniformly spaced fingers of Si. (5) Finally, the fingers break up into Si crystals via Rayleigh instability.

Fig. 5.8(a), 5.8(b) and 5.8(c) shows SEM images recorded from doped SOI samples with a device layer thickness of 25 nm following three successive 60 s

anneal cycles at 900°C. These samples were thinned from a 45 nm SOI phosphorous doped to 10^{19} cm^{-3} and were annealed without oxygen plasma cleaning. Fig. 5.8(a) shows a large scale view of a dewetted area on the SOI. The Si film has become broken in places, agglomerating into Si crystals and exposing the BOX layer. A closer view of one dewetted region is shown in Fig. 5.8(b). According to Danielson's five-step model of the dewetting mechanism [2], fingers of Si form at the void edge and then break into nano crystals via Rayleigh instability. Some examples of Si fingers which are close to breaking into crystals are visible in the area shown in Fig. 5.8(a) [18]. A more detailed image of the nano crystals is shown in Fig. 5.8(c). The Si device layer, exposed BOX, and Si crystals are indicated in Fig. 5.8(c). Faceting of the crystal islands can be observed in Fig. 5.8(c). The contact angle of the dewetting crystals is governed by the energy configuration in the film [14]. The Young's equation that relates the interface energies with the contact angle, applies during the dewetting process since the film is a high viscosity liquid. However, after re-crystallisation the surface contact angle of the dewetting solids are uniquely defined for and by the given facet [12, 14]. This is unlike the case of a liquid droplet, which is not limited to discrete values but takes the value that minimizes the free energy [34]. In the case of two facets with degenerate energies, the facets with a steeper surface contact angle will form because that results in a smaller surface area [14]. The crystals are usually situated on or beside a region of exposed BOX. Fig. 5.8(d) shows dewetting on a 12 nm SOI following a 30 s anneal cycle at 850 °C. This sample was boron doped to 10^{15} cm^{-3} and used as obtained, without thinning. As the dewetting theory suggests, the thinner a film gets, the lower the dewetting temperature [2]. The onset temperature of dewetting in 12 nm SOI is at least 50 °C lower than that of 25 nm SOI. Dewetting in 12 nm SOI (Fig. 5.8(d)) shows a square pattern with the edges parallel to the $\langle 110 \rangle$ direction and the dewetting crystals aligned along the $\langle 130 \rangle$ direction. This long range order in the position of the crystals is due to the surface energy anisotropy in the SOI film.

As the SOI thickness reduces further, the dewetting temperature also lowers, thus dropping the temperature difference between the oxide desorption and

dewetting. As a result, dewetting of thinner films gives rise to more complex structures [19]. Also, thinner SOI becomes increasingly sensitive to mechanical, chemical and thermodynamic factors, which may have minimal impact on dewetting in thicker films and responsible for new behaviours in thinner SOI.

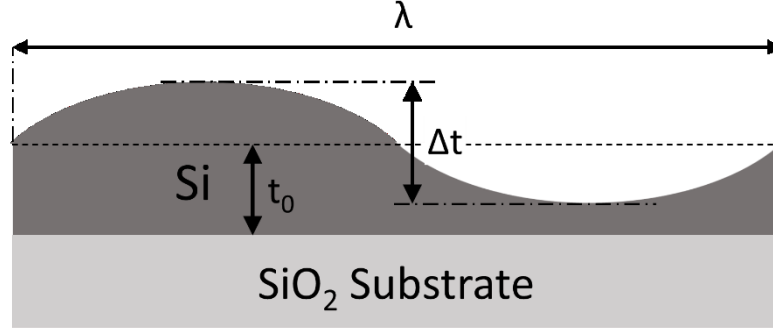


Fig. 5.9: Schematic illustration of an interfacial wave in SOI oscillating at a wavelength λ showing the change in film thickness Δt resulting from the perturbation, where t_0 is the initial film thickness. For a set thickness of ultrathin film there is a range of wavelengths whose amplitudes will continue to grow until $\Delta t > t_0$ causing film rupture.

At the time of writing this thesis, and on the basis of available STM, SEM and AFM results, we believe that the dewetting in ultra-thin SOI with thickness lower than 3 nm proceeds through thermal fluctuation in contrast to the void growth mechanism observed in the case of thicker SOI, as discussed in the previous section. The thermal energy produces surface interfacial waves with a characteristic wavelength λ that brings about thickness variation in the film (see Fig. 5.9) [35]. The fluctuations in the film thickness increases the van der Waals attraction interaction between the film surface and the interface. Also, the thickness variation increases the film-vacuum surface area thus increasing the component of the free energy that will drive the opening of voids to expose the low energy BOX. The critical wavelength λ_{crit} , that is defined as the shortest wavelength of an interfacial perturbation that may result in the rupture of the film is given by

$$\lambda_{crit} = t^2 \sqrt{\frac{c\gamma_{Si}}{A}}$$

Where c is a constant, t is the thickness of the film, γ_{Si} is the surface energy of Si film and A is the Hamaker constant [22, 35, 36]. Perturbation with wavelength

$\lambda \geq \lambda_{crit}$ are amplified and results in spontaneous rupture of the film [35, 37]. However, the fastest growing perturbation wavelength is close to the critical wavelength, since a shorter wavelength has less driving force and the longer wavelength require the displacement of a larger volume of the film.

An important aspect of the thermally driven spontaneous dewetting, is the formation of undulations, which appears as bicontinuous surface patterns, at the early stages of film breakup and formation of uniform sized holes in the film [25-28]. Analysis of annealed ultra-thin SOI have shown the existence of bicontinuous surface patterns and uniform sized holes. Fig. 5.10(a) shows an SEM image of a 6 nm SOI annealed for 30 s at 750 °C. The sample surface shows the presence of several holes and protrusions as shown in the inset in Fig. 5.10(a). These protrusions are believed to be the SiC structures created during the oxide desorption process (more details in section 3.4). Fig. 5.10(b) shows a contrast adjusted SEM image of Fig. 5.10(a). In Fig. 5.10(b), the pixel intensity of the SEM image in Fig. 5.10(a) above and below a threshold value was neglected to display a thin slice of grey scale data. The contrast corrected SEM image clearly highlights the dark grey bicontinuous surface patterns on the film. The pattern appears similar to the thermal fluctuation driven dewetting patterns in polymer and metal films [22, 23, 25-28]. This SEM data further supports the argument put forth earlier, based on the results of surface analysis of 3 nm SOI, suggesting that the 3 nm SOI dewets spontaneously through a process that involves thermally driven fluctuation of the film thickness.

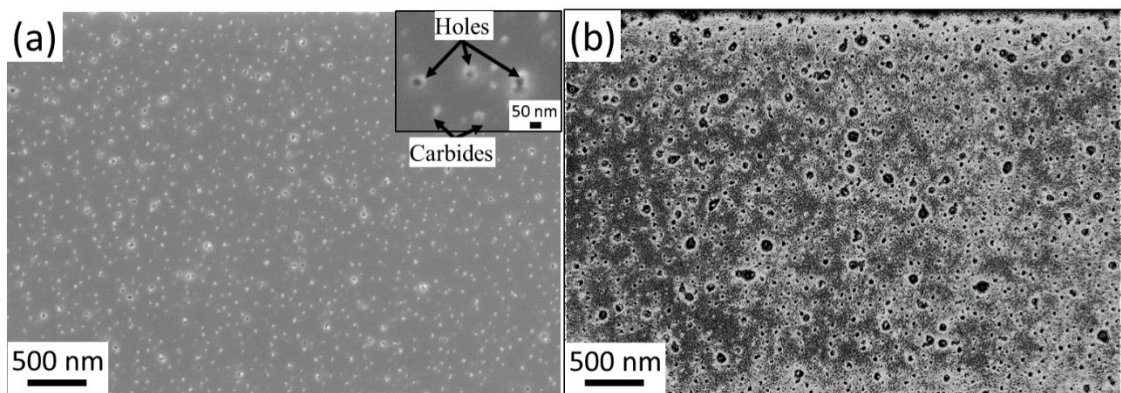


Fig. 5.10: (a) SEM image of a 6 nm annealed SOI. (b) shows the SEM image in (a) after adjusting the contrast. (b) shows undulation like patterns on the surface. The inset in (a) shows an expanded region in (a) showing holes and carbides.

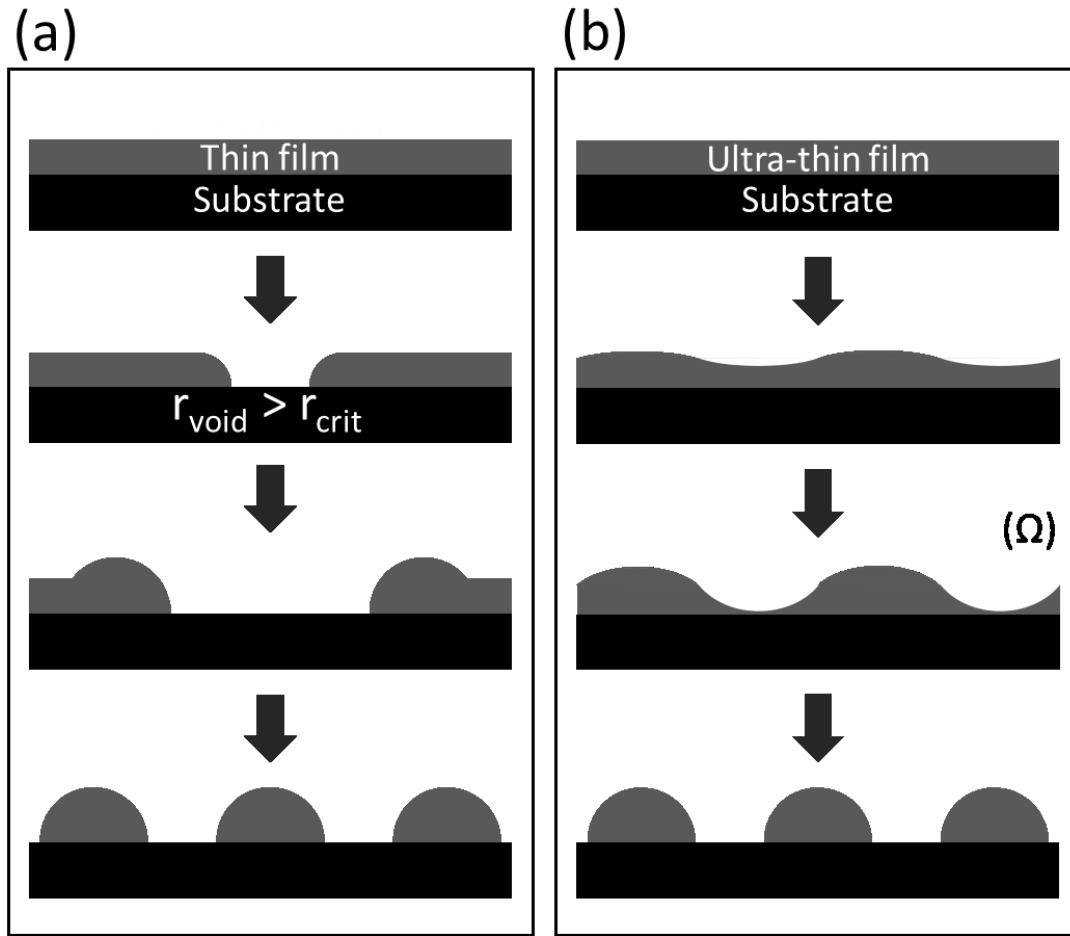


Fig. 5.11: The two dewetting modes: through hole nucleation and growth in thick SOI; through growth of thermal fluctuation in ultra-thin SOI. (Ω) shows the possible intermediate stage in dewetting of ultra-thin SOI due to thermal fluctuation.

Fig. 5.11 shows a schematic representation of the two dewetting mechanisms discussed in this section. The arrow on the left shows the dewetting mechanism in a thicker film where the void formed at the defect site grows via a diffusion driven capillary edge instability as proposed by Danielson et al.,. The mechanism shown on the right is a fluctuation driven spontaneous dewetting which is important only in the case of ultra-thin SOI. As shown in section 5.5, dewetting in the absence of voids is thermodynamically impossible for thick SOI. This thermal fluctuation model is only important for ultra-thin SOI films. Also, in the thermal fluctuation mechanism transient morphology with ultra-thin wetting layer interconnecting the crystals (as pointed by (Ω) in Fig. 5.11) may be obtained by a rapid annealing process.

5.6 Conclusions

The evolution of the morphology of SOI device layers after UHV annealing was studied for varying film thicknesses. SOI device layers were thinned to thicknesses ranging from 25 nm to 3 nm and annealed in an UHV environment to temperatures ranging from 600 °C to 1000 °C. Further, annealed SOI was characterized with SEM, AFM and STM.

All samples were found to dewet at around 900 °C, but the extent of dewetting depended on their thickness and the duration of annealing. For device layer thicknesses above ~4 nm, the film was found to dewet via a diffusion driven mechanism. The dewetting process in this case starts as nucleation of square voids and voids grow via capillary edge instability and crystals were formed via Rayleigh instability. The dewetting process follows along the crystallographic axis: square shaped voids grow with edges parallel to the $\langle 110 \rangle$ direction and the final crystals align along the $\langle 130 \rangle$ direction. The dependence on crystallographic axis is due to the anisotropic nature of the surface energy.

STM measurements on 3 nm SOI have shown that annealing leads to faceting of the film and increase in surface roughness. The roughness on the film resembles peaks and troughs of waves. SEM analysis has shown the presence of wave-like surface patterns in the ultra-thin SOI before dewetting. Based on these observations we have suggested that ultra-thin SOI becomes increasingly sensitive to thermal fluctuations. Using KPM measurements we have detected a transient structure during dewetting where the dewetting crystals are physically and electrically interconnected. These observations indicate that dewetting in ultra-thin SOI with thicknesses less than ~3 nm is driven by the growth of thermal fluctuations. The thermal fluctuation in the ultra-thin film allows the surface and the interface to interact via van der waals forces and results in homogeneous spontaneous nucleation of voids in SOI device layers. The thermal perturbation with wavelength equal to or greater than a critical wavelength gets amplified and results in spontaneous rupture of the film exposing the underlying BOX. However, by abruptly stopping the annealing process, transient structures as mentioned above may be obtained. Further, crystals formed due to dewetting of the ultra-thin

film having a lower contact angle compared to thicker films. Based on these observations, we have proposed that the ultra-thin SOI restructures during annealing and forms low surface energy facets. Since the faceting lowers the surface energy of the system, dewetting of the faceted film results in a lower contact angle of the dewet crystals.

5.7 References

1. Yukinori, O., et al., *Thermal Agglomeration of Thin Single Crystal Si on SiO₂ in Vacuum*. Japanese Journal of Applied Physics, 1995. **34**(4R): p. 1728.
2. Danielson, D.T., et al., *Surface-energy-driven dewetting theory of silicon-on-insulator agglomeration*. Journal of Applied Physics, 2006. **100**(8): p. 083507.
3. Danielson, D.T., *Anisotropic dewetting in ultra-thin single-crystal silicon-on-insulator films*. 2008, Massachusetts Institute of Technology.
4. Young, T., *An essay on the cohesion of fluids*. Philosophical Transactions of the Royal Society of London, 1805. **95**: p. 65-87.
5. Cheynis, F., et al., *Dewetting dynamics of silicon-on-insulator thin films*. Physical Review B, 2011. **84**(24): p. 245439.
6. Sutter, P., W. Ernst, and E. Sutter, *Scanning tunneling microscopy on ultrathin silicon on insulator (100)*. Applied Physics Letters, 2004. **85**(15): p. 3148.
7. Zhang, P., et al., *Electronic transport in nanometre-scale silicon-on-insulator membranes*. Nature, 2006. **439**(7077): p. 703-706.
8. Xue, K., J.B. Xu, and H.P. Ho, *Nanoscale in situ investigation of ultrathin silicon oxide thermal decomposition by high temperature scanning tunneling microscopy*. Nanotechnology, 2007. **18**(48): p. 485709.
9. Barimar, P.S.N., et al., *Study of the effect of thermal treatment on morphology and chemical composition of silicon-on-insulator*. Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena, 2016. **34**(4): p. 041806.
10. Tabe, M., et al., *Formation of high-density silicon dots on a silicon-on-insulator substrate*. Applied Surface Science, 1999. **142**(1–4): p. 553-557.
11. Legrand, B., et al., *Formation of silicon islands on a silicon on insulator substrate upon thermal annealing*. Applied Physics Letters, 2000. **76**(22): p. 3271.
12. Nuryadi, R., Y. Ishikawa, and M. Tabe, *Formation and ordering of self-assembled Si islands by ultrahigh vacuum annealing of ultrathin bonded silicon-on-insulator structure*. Applied Surface Science, 2000. **159–160**: p. 121-126.
13. Legrand, B., et al., *Thermally assisted formation of silicon islands on a silicon-on-insulator substrate*. Journal of Applied Physics, 2002. **91**(1): p. 106.

14. Yang, B., et al., *Self-organization of semiconductor nanocrystals by selective surface faceting*. Physical Review B, 2005. **72**(23).
15. Bussmann, E., et al., *Thermal instability of silicon-on-insulator thin films measured by low-energy electron microscopy*. IOP Conference Series: Materials Science and Engineering, 2010. **12**: p. 012016.
16. Bussmann, E., et al., *Dynamics of solid thin-film dewetting in the silicon-on-insulator system*. New Journal of Physics, 2011. **13**(4): p. 043017.
17. Aouassa, M., et al., *The kinetics of dewetting ultra-thin Si layers from silicon dioxide*. New Journal of Physics, 2012. **14**(6): p. 063038.
18. Leroy, F., et al., *Dynamics, anisotropy, and stability of silicon-on-insulator dewetting fronts*. Physical Review B, 2012. **85**(19).
19. Trautmann, M., et al., *Interplay between deoxidation and dewetting for ultrathin SOI films*. Applied Physics Letters, 2017. **110**(16): p. 161601.
20. Nuryadi, R., et al., *Thermal agglomeration of single-crystalline Si layer on buried SiO₂ in ultrahigh vacuum*. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2002. **20**(1): p. 167-172.
21. Bischof, J., et al., *Dewetting Modes of Thin Metallic Films: Nucleation of Holes and Spinodal Dewetting*. Physical Review Letters, 1996. **77**(8): p. 1536-1539.
22. Vrij, A., *Possible mechanism for the spontaneous rupture of thin, free liquid films*. Discussions of the Faraday Society, 1966. **42**: p. 23-33.
23. Ruckenstein, E. and R.K. Jain, *Spontaneous rupture of thin liquid films*. Journal of the Chemical Society, Faraday Transactions 2: Molecular and Chemical Physics, 1974. **70**: p. 132-147.
24. Wyart, F.B. and J. Daillant, *Drying of solids wetted by thin liquid films*. Canadian Journal of Physics, 1990. **68**(9): p. 1084-1088.
25. Herminghaus, S., et al., *Spinodal Dewetting in Liquid Crystal and Liquid Metal Films*. Science, 1998. **282**(5390): p. 916-919.
26. Xie, R., et al., *Spinodal Dewetting of Thin Polymer Films*. Physical Review Letters, 1998. **81**(6): p. 1251-1254.

27. Seemann, R., S. Herminghaus, and K. Jacobs, *Gaining control of pattern formation of dewetting liquid films*. Journal of Physics: Condensed Matter, 2001. **13**(21): p. 4925.
28. Krishna, H., et al., *Thickness-dependent spontaneous dewetting morphology of ultrathin Ag films*. Nanotechnology, 2010. **21**(15): p. 155601.
29. Niehus, H., et al., *A real space investigation of the dimer defect structure of Si (001)-(2times8)*. Journal of Microscopy, 1988. **152**(3): p. 735-742.
30. Jr., J.A.D. and H.E. Farnsworth, *Work Function and Sorption Properties of Silicon Crystals*. Journal of Applied Physics, 1958. **29**(8): p. 1195-1202.
31. Sayed, S.Y., et al., *Preferential face deposition of gold nanoparticles on silicon nanowires by galvanic displacement*. CrystEngComm, 2012. **14**(16): p. 5230-5234.
32. Fowlkes, J., et al., *Hierarchical nanoparticle ensembles synthesized by liquid phase directed self-assembly*. Nano letters, 2014. **14**(2): p. 774-782.
33. Srolovitz, D.J. and M.G. Goldiner, *The Thermodynamics and Kinetics of film agglomeration*. JOM, 1995. **47**(3): p. 31-36.
34. Liu, F., *Self-Assembly of Three-Dimensional Metal Islands: Nonstrained versus Strained Islands*. Physical Review Letters, 2002. **89**(24): p. 246105.
35. O'Kelly, C.J., S.J. Jung, and J.J. Boland, *Metal Nanostructure Synthesis via Surface Energy Driven Growth*. Crystal Growth & Design, 2016. **16**(12): p. 7318-7324.
36. Sheludko, A., *Thin liquid films*. Advances in Colloid and Interface Science, 1967. **1**(4): p. 391-464.
37. Saramago, B., *Thin liquid wetting films*. Current Opinion in Colloid & Interface Science, 2010. **15**(5): p. 330-340.

6

THERMAL PROCESSING OF PATTERNED SOI NANOWIRES

Due to the capillary edge and Rayleigh instabilities, the edges of SOI and nanowires fabricated from SOI tend to dewet at a reduced temperature compared to un-patterned SOI, and therefore makes the surface analysis of nanowires challenging. In this work silicon nanowires of different widths were fabricated from silicon-on-insulator (SOI) wafers using electron beam lithography. We show that nanowires can be processed in UHV using low thermal budget flashing and then analysed with STM. The reduction in thermal budget is believed to be due to the edge effect along the length of the nanowires. An increase in surface diffusion of silicon atoms away from the edges due to capillary forces expedites the oxide desorption process in the nanowires. By carefully controlling the thermal process, nanowires can be prepared without affecting their structural integrity. However, if annealed further, the capillary forces deforms the edges of the nanowires and causes them to finally break into a row of crystals due to Rayleigh instability. The findings in this work shows that surface analysis of ultra-small silicon nanowires on insulator structures is possible. In order to carry out the surface analysis on smaller nanostructures in the future, a simple nanowire and nanodisc fabrication technique has been developed. Commercially available TiO_2 nanowires and nanoparticles spray deposited over SOI have been used as etch mask to fabricate silicon nanowires and nanodisc from SOI and form the basis for this approach.

6.1 Introduction

Nanomaterials are interesting as they exhibit fascinating mechanical [1], optical [2, 3] and electronic properties [4, 5] that are significantly different from their bulk counterparts. The properties of nanomaterials can also be tuned by modifying their size [6, 7], shape [5] and surface [8]. Also, the enormous surface-area-to-volume ratio of nanomaterials leads to interesting size-dependent thermodynamic properties such as lowering of melting point temperatures with reducing nanoparticle Size [9-11].

Silicon nanostructures have generated particular interest lately owing to their compatibility with the existing Si-based micro and nano-electronics technology [12-15]. Silicon processing and integration techniques have advanced far beyond any other material, and also silicon is considered a model system for an indirect-band gap semiconductor [16]. Silicon nanostructures fabricated from Silicon-on-Insulator (SOI) have enormous technological relevance since they are a basis for some of the current day CMOS technology [17]. Furthermore, the SOI structure enables fabrication of crystalline nanostructures of virtually any desired crystal orientation over an oxide layer.

Silicon nanowires are also an attractive one-dimensional nanomaterial that could play an important role as a model system to demonstrate quantum size effects [18]. STM and STS are powerful tools to study the electronic structure and size effects of nanowires. However, presence of oxide on the nanowires complicates the surface analysis. The thermal annealing process used to desorb the oxide in UHV, can lead to instabilities in nanowires and result in dewetting.

Silicon nanowires fabricated over SOI also undergoes self-diffusion at the edges due to the capillary forces [19]. The high local surface curvature of the edges leads to diffusion of silicon away from the edges into the flat film. This diffusion of silicon can accelerate the oxide desorption near the edges and therefore facilitate oxide desorption from the nanowires without affecting their structural integrity. However, on further annealing, the capillary forces develops into capillary edge instability [19]. This instability, which is driven by surface-energy-driven surface-

diffusion [19, 20], along with Rayleigh instability, later leads to dewetting of the edges.

Under high temperature processing conditions nanowires are prone to breakup into fragments. It was first predicted by Plateau that a liquid cylinder of radius r is unstable to radius perturbations whose wavelength λ exceeds the circumference of the cylinder. The cylinder thus decreases its total energy by breaking-up into a row of spherical drops under volume conservation [21]. Plateau's work was later followed by the theoretical studies on the instability of liquid jets by Lord Rayleigh [22]. More recently, calculations have been performed for solid cylinders by taking mass transport by surface diffusion into account [23]. They have shown that for a cylinder with initial radius r and a sinusoidal perturbation $R = r + \Delta r_o \sin(2\pi x/\lambda)$, perturbations with wavelength $\lambda > 2\pi r$ are expected to increase spontaneously in amplitude and grow with time. This is consistent with recent results that have shown at high temperatures Si nanowires on oxide have also been found to break-up into nanocrystals [19, 24, 25].

6.2 Experimental details

6.2.1 Nanowire design considerations

Si nanowires on SOI were fabricated using electron beam lithography (EBL). In order to analyse the SOI nanowires in an UHV STM, samples were designed to fulfil the following requirements:

1. High density of nanowires makes them easier to locate them with STM.
2. Avoid presence of thick oxide on the sample surface to avoid crashing of STM tip.
3. High doping of nanowires for better conductivity.
4. Nanowires of multiple widths fabricated for comparative studies.

These requirements were satisfied by the following design:

1. High density of Si nanowires in a $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ area were fabricated and consisted of 400 unit cells shown in Fig. 6.1(a). This $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ pattern was repeated in the three regions of the sample.
2. The regions beside the nanowire areas were etched down to substrate silicon.

3. Si nanowires were fabricated on highly doped (10^{20} cm^{-3}) SOI device layer.
4. Nanowires with increasing widths from 50 nm to 225 nm in increments of 25 nm were fabricated (see Fig. 6.1(a))

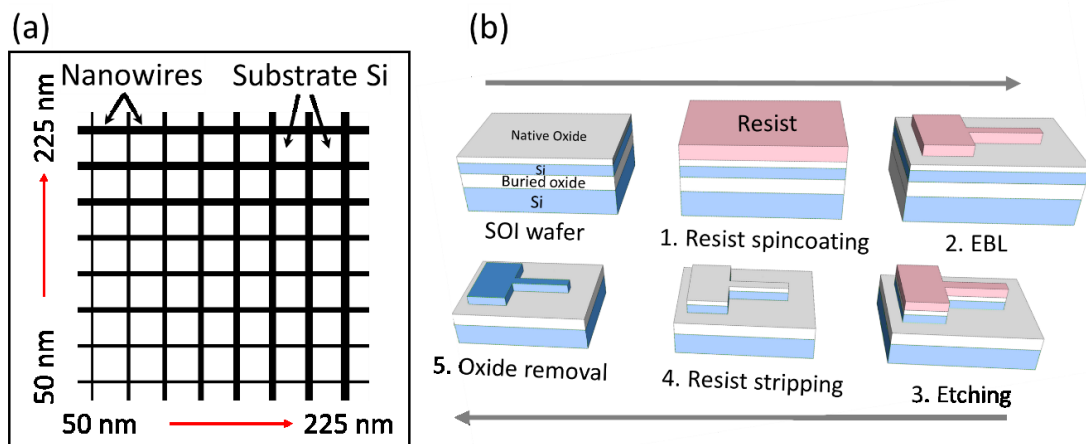


Fig. 6.1: (a) Schematic showing the design of the EBL Si nanowires. (b) Schematic showing the EBL process. This was the smallest set of nanowire network consisting of nanowires of width ranging from 50 nm to 225 nm. This set was repeated in a $200 \mu\text{m} \times 200 \mu\text{m}$ area.

6.2.2 Electron beam lithography (EBL) and nanowire edge smoothening

Fig. 6.1(b) shows a schematic of the EBL process. The technique involves irradiating the spin coated resist over the sample in a specific user defined pattern. An e-beam resist is first spin-coated over the SOI and exposed to the e-beam in a specific pattern using a Raith EBL system. The e-beam exposure pattern is controlled by the EBL software. A pattern is loaded into the software and a beam

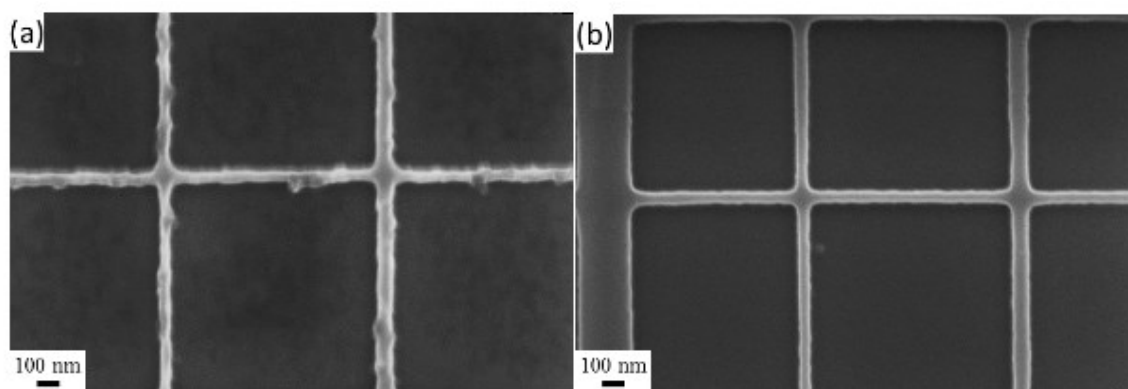


Fig. 6.2: SEM images of as fabricated Si nanowires on a 10 nm SOI (a), and the same sample following a 60 s O_2 plasma treatment followed by dil. HF rinse (b).

blanker system in the SEM is used as a dynamic mask to write the pattern. EBL resists such as ma-N 2403, Poly(methyl methacrylate) (PMMA) and Hydrogen SilsesQuioxane (HSQ) were used for patterning. HSQ resist gave the best results, i.e., thinnest (50 nm) nanowires with comparatively low edge roughness were obtained using the HSQ resist.

Even the nanowires fabricated using HSQ resist had significant edge roughness as shown in Fig. 6.2(a). A higher edge roughness is a trade-off while fabricating large area patterns. Lower edge roughness may be obtained by increasing the EBL resolution but that would increase the lithography time by a great extent. In order to circumvent this issue a simple edge smoothening technique was utilized. Oxygen plasma treatment was found to be effective in reducing the edge roughness. Fig. 6.2 shows an SEM image of Si nanowires before (a) and after (b) a 60 s O₂ plasma treatment. The O₂ plasma treatment was followed by a quick rinse in hydrofluoric acid. An isotropic O₂ plasma oxidises the rough features on the nanowire since these rough regions have higher surface area. The plasma grown oxide layer is later etched off in HF solution.

6.3 Edge effect: oxide desorption and dewetting

As discussed earlier in section 6.2, surface diffusion due to capillary forces at the edges is inversely proportional to the edge thickness. The edges of patterned SOI are often tapered and thinner than the device layer (see Fig. 6.3(a)) [20], therefore the tapered edges have higher curvature gradient. The capillary driven diffusion at the edges leads to edge effects in oxide desorption processes. This edge effect can clearly be seen in Fig. 6.3(b) showing a 45 nm SOI after flash annealing for 60 s at 750 °C. The oxide desorption was observed to be prevalent near the edges of the sample. The silicon atoms diffusing away from the edge and towards the flat region of the film readily provides silicon adatoms for the oxide desorption process near the edges. This results in increased rate of oxide desorption at lower temperatures.

The edges of SOI are also known to undergo dewetting at lower temperatures [19, 20, 26]. The edge effect in dewetting is strongly believed to be due to the capillary film edge instability [19]. The film edge is modelled as an infinitely long

discontinuity or a line defect on the film which initiates the dewetting process [19]. Once the oxide is desorbed, the film edges starts to retract due to self-diffusion and finally dewet. This can be seen in the SEM images in Fig. 6.3(b) and 6.3(c), showing edges of a 45 nm and a 20 nm SOI film both annealed for three 60 s cycles at 900°C. The 45 nm film in Fig. 6.3(c) shows the early stage of dewetting where the SOI film has started to peel back from the edge and the rim of the edge is bulged. This initial stage of dewetting is similar to that predicted by Danielson's model based on capillary film edge instability [19]. The 20 nm SOI, shown in Fig.

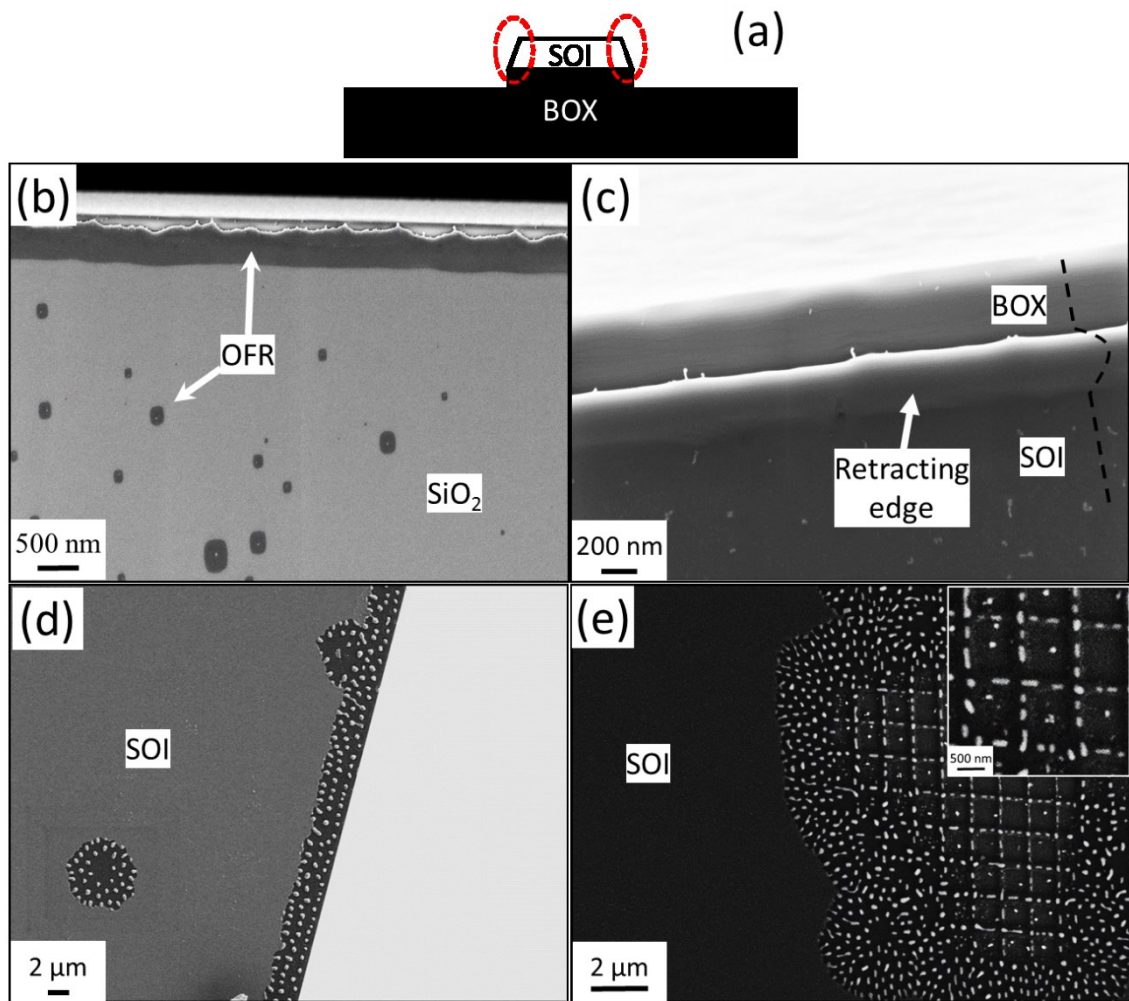


Fig. 6.3: (a) Schematic showing thinner edges of patterned SOI which is believed to initiate dewetting [2, 3]. (b) and (c) shows edge effects in dewetting observed for a (b) 45 nm and (c) 20 nm SOI following three 60 s anneal cycles at 900°C. (d) Shows dewetting of an 8 nm SOI at the edge of the wafer even before the complete desorption of oxide, following a ten 30 s anneal cycles at 750°C (e) SEM image of nanowire on a 10 nm SOI after ten 30 s anneal cycles at 800°C. Inset in (e) shows a close-up of the Rayleigh instability driven breaking of nanowires.

6.3(d), although annealed with parameters similar to the 45 nm SOI, shows an advanced stage of dewetting with several rows of crystals. This difference in the stage of dewetting in the two samples is because the edge of the thinner SOI has a higher curvature gradient and therefore leads to more diffusion. As a result edges of thinner SOI dewets more rapidly than in the case of thicker SOI.

Fig. 6.3(e) shows dewetting of a patterned 10 nm SOI after ten 30 s anneal cycles at 750°C. Fig. 6.3(e) clearly shows the reduced thermal stability of the patterned region: while the un-patterned region of the sample was intact, the patterned region had completely agglomerated under this annealing condition. The dewetted region consisted of patterns shown in Fig. 6.1(a). The inset in Fig. 6.3(e) shows a close-up of dewetted nanowires where the nanowires have broken into crystals.

This section clearly shows that the edges of ultra-thin SOI and nanostructures fabricated on the ultra-thin SOI dewets at lower temperature. The edge effect also ensures oxide desorption from the silicon edges at lower temperatures. STM measurements of nanowire structures fabricated on ultra-thin SOI also showed an enhanced oxide desorption on the nanowires in comparison to the flat film region. The following section details an STM analysis of flash annealed SOI nanowires, fabricated from an 8 nm SOI film.

6.4 STM analysis of SOI nanowires

The STM measurements were carried out on nanowires with widths as small as 50 nm fabricated on an 8 nm thick device layer of SOI. Fig. 6.4(a) shows an STM topographic image of a 50 nm wide SOI nanowire following 3 flash annealing cycles of 30 s at ~ 730 °C. The BOX around the nanowire structure was etched down to substrate allowing the STM probe to approach the nanowire safely without risking crashing into the BOX. Although the flash annealing condition was not sufficiently high to desorb oxide from a flat silicon region, the substrate silicon was covered with a thin layer oxide that did not prevent STM imaging. In order to avoid the tip crash into this oxide, high scan bias voltages were used for large area scans. The STM image in Fig. 6.4(a) was recorded at 7 V bias and 5 pA current setpoint. The figure shows an STM image of a ~ 50 nm nanowire. Fig. 6.4(b) shows a close-

up region from the middle of the nanowire. This image was recorded with 4 V bias and 5 pA current setpoint. The image reveals atomic steps of Si(100), although there is some ghosting in the image due to a double-tip effect that is common whenever STM is used to image a surface with large topographic features. The image also show SiC protrusions, which is consistent with the surface oxide layer being completely desorbed as discussed in section 3.5 (chapter 3).

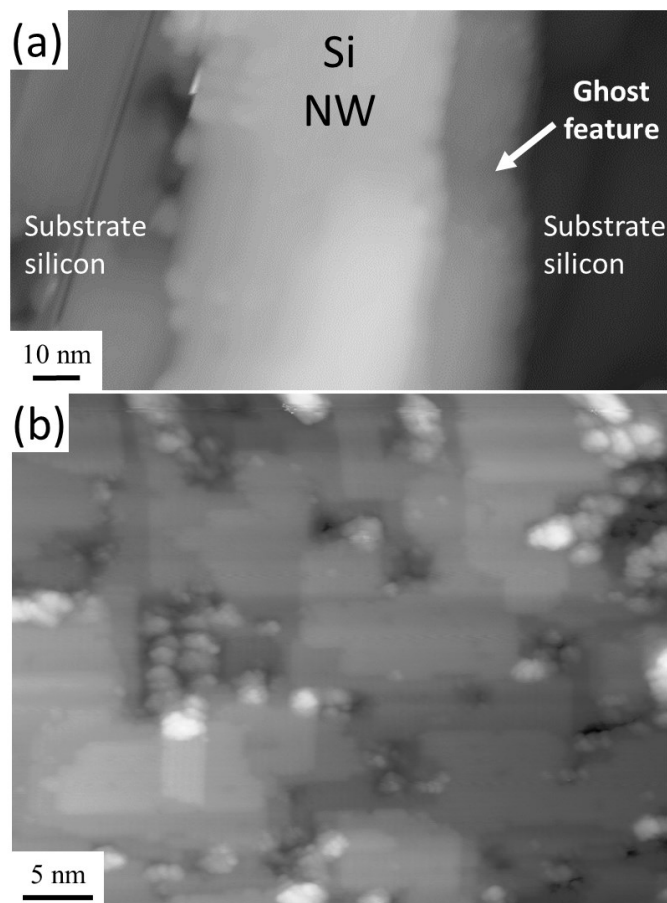


Fig. 6.4: (a) STM height image of a 50 nm wide SOI nanowires fabricated on an 8 nm SOI. (b) shows a close-up region from (a). (a) was recorded at 7 V sample bias and 5 pA setpoint current. (b) was recorded at 4 V bias and 5 pA setpoint current.

Fig. 6.5(a) shows an STM topographic image recorded from a close-up region of the nanowire surface. The image was recorded with 2 V bias and 20 pA setpoint current. The figure clearly shows two domains of the dimer rows with row spacing equal to approximately $7.3 \text{ \AA}$, consistent with the surface being Si(100) (2×1).

This suggests that a silicon nanowire of width up to 50 nm and thickness down to 8 nm can be flash annealed at a lower temperature of around 730 °C to desorb oxide and to obtain a clean silicon surface. These STM images are a testament that silicon nanowires of these dimensions are stable under reduced thermal budget flash annealing and do not undergo faceting or dewetting. Fig. 6.5(b) shows the tunneling spectra recorded from the 50 nm wide nanowire surface (black) along with a reference spectra from bulk Si(100). The spectra was recorded with 2 V bias and 20 pA setpoint current. The spectra of the nanowire shows a ~ 0.4 eV blue shift in the spectral features in comparison to the bulk Si(100). The same ~ 0.4 eV shift was also observed in the spectra recorded on other nanowires as wide as 200 nm and 225 nm (same thickness of 8 nm). In principle there could be different reasons

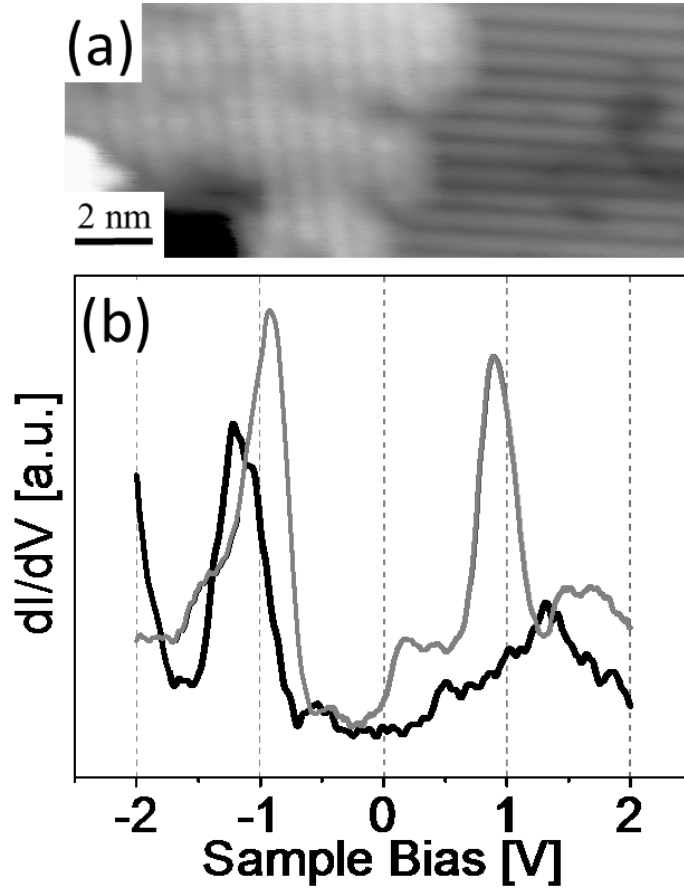


Fig. 6.5: (a) A close-up of a 50 nm wide nanowire on SOI showing a clean Si(100) (2×1) surface. (b) shows the STS spectra recorded from the nanowire surface (black) along with a reference spectra from a bulk Si(100) (grey). Both image and the spectra were recorded at 2 V bias and 20 pA current. The shift in the spectra recorded from the nanowire is probably due to contamination in the tip.

for blue shift in STS: such as high sample resistance, tip-induced field effect and high spreading resistance have been discussed in chapter 4. However, the blue shift observed in this case was only be due to a contaminated tip since there was no correlation with the nanowire thickness and the shift was constant for all thicknesses. Furthermore, analysis of the quality of the STM tip over the Pt crystal also suggested that the tip was contaminated.

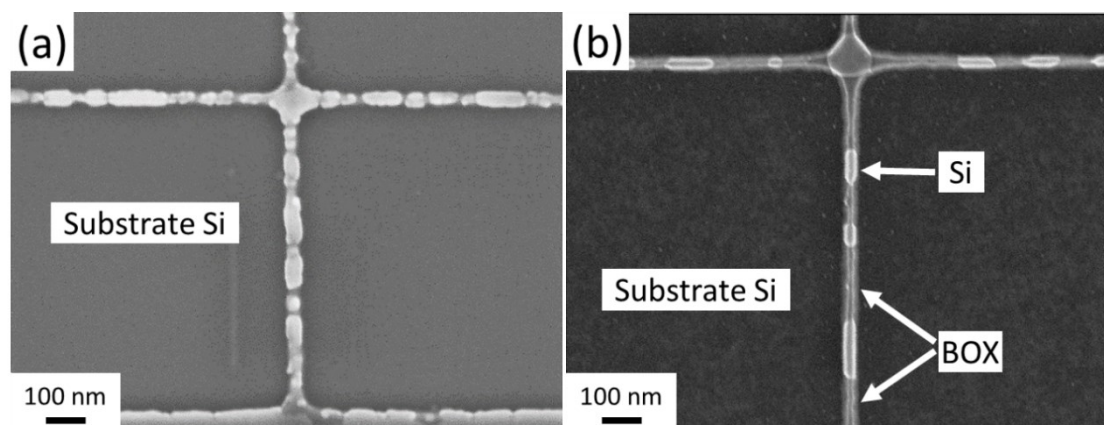


Fig. 6.6: Different stages of thermal instability in Si nanowires on SOI. (a) Rayleigh instability driven fluctuations in nanowires. (b) complete breaking of nanowires into discontinuous elongated Si crystals.

Annealing of nanowires at temperatures above ~ 730 °C resulted in instability in the nanowires, initially forming a modulation in the structure consistent with breaking into droplets and later breaking into elongated crystals on the BOX. The thermal gradient across the sample allowed for the study of different stages of the formation of these instabilities. Fig. 6.6(a) shows the initial stage of thermal instability in the nanowires forming oscillating structures due to Rayleigh instability. The sample was annealed for 30 s at ~ 750 °C. Advanced stage of dewetting of nanowires into crystals is shown in Fig. 6.6(b) which was recorded from the hotter end of the sample.

6.5 TiO₂ nanowire masked Si nanowires

The previous section demonstrated that silicon nanowires fabricated on SOI can be flash annealed and prepared in UHV for surface analysis without damaging the integrity of the structures. However, a thorough spectroscopic analysis of the structures proved challenging due to issues in the sample design and STM

measurements. Even with the help of one of the most sophisticated EBL systems available on the market, it was a challenge to fabricate nanowire structures smaller than 50 nm for STM analysis. STM analysis requires a high density of nanowires spread across the sample so that fabricating such a high density nanowires leads to a reduction in resolution. Our Createc UHV STM has a maximum sampling range of under 4 μm so that a low nanowire density makes it problematic to find target nanowires to study.

Although an oxygen plasma thinning technique can be used to thin EBL fabricated nanowires, plasma oxidation is an isotropic process and therefore a nanowire over BOX with a rectangular cross-section, would be oxidised equally from all three directions. Since the dimensions of the EBL fabricated nanowires in our case had an aspect ratio of 10:50 (thickness: width), O_2 plasma thinning will reduce the nanowire thickness significantly more than the nanowire width. Also, repetitive etching in dil. HF solution etches the BOX underneath the nanowires and makes the nanowires structurally unstable. Due to these challenges, oxygen plasma thinning could not be used. Further, to overcome the fabrication challenges a simple nanowire fabrication technique was developed.

Fig. 6.7 shows a schematic of the TiO_2 nanowire masked Si nanowires fabrication technique. This process makes use of chemically synthesised oxide nanowires as an etch mask to fabricate Si nanowires on SOI. TiO_2 nanowires with mean diameters of 50 nm, 20 nm and 10 nm were procured from Emfutur technologies and Novarials Corporation. The nanowires were dispersed in water or an IPA/ethanol mixture through mild sonication. The TiO_2 nanowires were spray deposited over SOI (Fig. 6.7 step 1). SOI samples were then etched in ICP (Fig. 6.7 step 2). The ICP etching removes all the silicon from the device layer except the region of silicon beneath the nanowires. The anisotropic nature of the ICP process along with the small size of the mask results in sharp edge features on the Si nanowires. After the ICP process, a thin film of metal is deposited through e-beam metal evaporation.

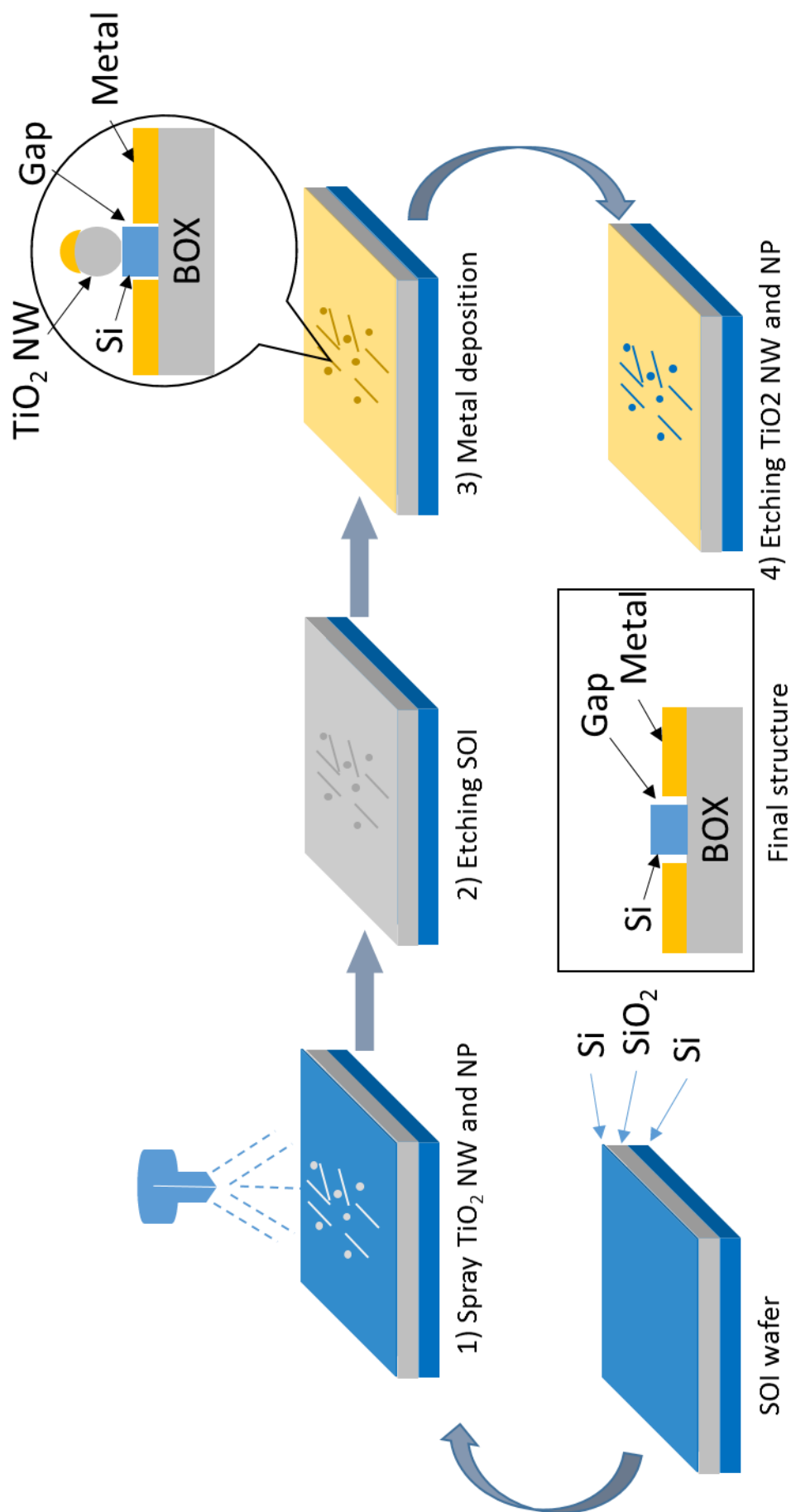


Fig. 6.7: Schematic of the TiO₂ masked Si nanowires fabrication process. 1) Spraying TiO₂ nanowires and nanoparticles on SOI, 2) ICP etching of SOI, 3) Metal deposition, 4) lift-off process to obtain Si nanowires and nanodiscs on BOX with metal contacts on the sides.

The e-beam evaporator provides directional metal deposition, this means that the metal is deposited only on the top of TiO_2 but not on the sides, as shown in the circle indicated in step 3 of Fig. 6.7. A short rinse in dil. HF solution etches the TiO_2 from the sides and lift-off the metal over it. This process provides a continuous metal film over the BOX, barely contacting the Si nanowires. Similar to TiO_2 nanowires, even TiO_2 nanoparticles could be used in this process. Etching SOI with TiO_2 nanoparticles over it will produce silicon nanodiscs on SOI.

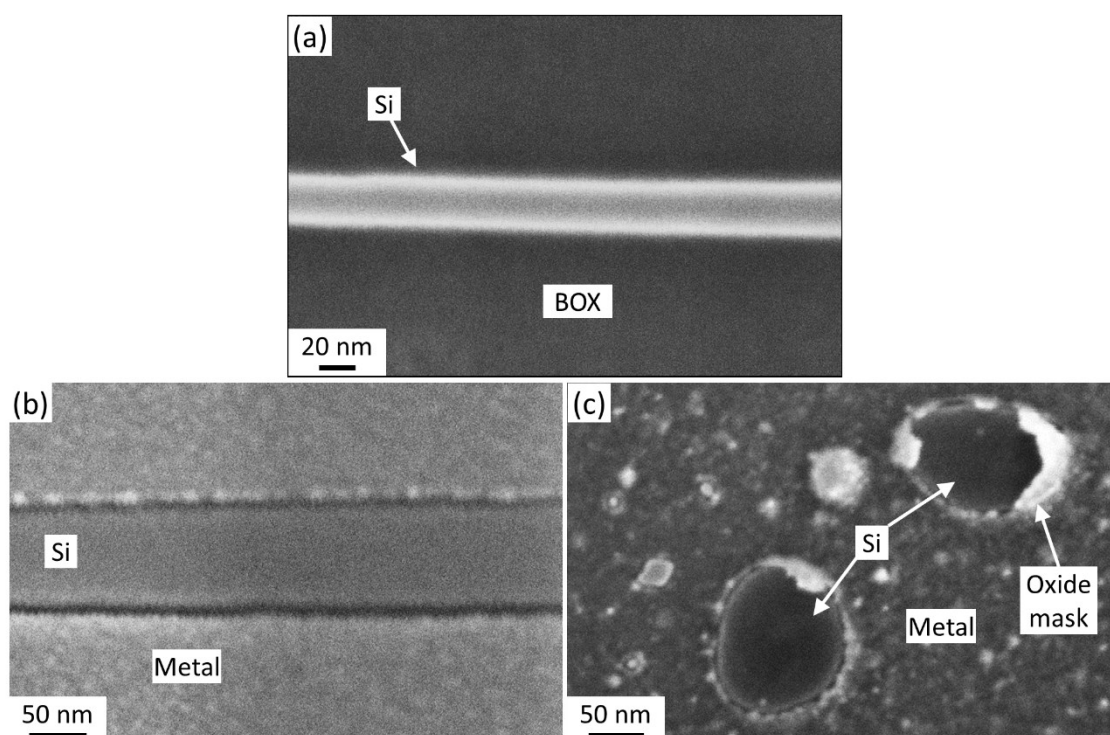


Fig. 6.8: SEM images showing nanostructures fabricated on SOI. (a) shows ~ 20 nm low edge roughness Si nanowires on BOX fabricated using the TiO_2 mask technique. (b) shows the fabricated nanowires with contact metal film. (c) Si nanodiscs with un-etched resist and metal contact film.

One of the important advantage of this technique is the ability to fabricate ultra-small Si nanowires and nanodiscs with low edge roughness. Fig. 6.8 shows an example of the Si nanowires and nanodiscs fabricated using this technique from 10 nm SOI. The Si nanowire shown in Fig. 6.8(a) is 20 nm wide. The length of these nanowires were around $3 \mu\text{m}$. These Si nanowires have a sharp edge features in comparison to the nanowires fabricated through EBL (Fig. 6.2(a)). Fig. 6.8(b) and (c) shows an SEM image of Si nanowires and Si nanodiscs surrounded by a

metal film. This metal film acts as an electrical contact for all the nanowires fabricated on the wafer. Since these samples were prepared for demonstration purposes, a Ti/Au (4 nm/ 4nm) metal film was used. However, for STM measurements a Pt metal film could be used so that in the event of STM tip contamination, the Pt metal could also be used to form the tip. Another advantage of this technique in comparison to EBL is the ease of fabricating colossal amount of crystalline nanowires or nanowire network on wafers. The nanowire and nanodiscs fabricated over SOI with metal contact film will be used in the future to study their electronic structure using STM and STS.

6.6 Conclusion

STM measurements of flash annealed SOI nanowires have shown that the surface oxide on the nanowires desorbs at lower temperatures in comparison to a flat silicon surface. Diffusion of silicon away from the edges of the nanowires due to the capillary edge instability is believed to supply silicon adatoms that expedites the oxide desorption process in the nanowires. Analysis has also shown that nanowires as small as 50 nm wide and 8 nm thick can sustain the low budget thermal processing without undergoing faceting or dewetting. However, annealing at temperatures over ~ 750 °C breaks the nanowires through Rayleigh instability into Si crystals.

Furthermore, this chapter also presents preliminary data of a new and simple silicon nanowire and nanodisc fabrication technique. This fabrication technique uses solution dispersed TiO_2 (or any stable nanowires) nanowires and nanoparticles, sprayed over SOI, as an etch mask to fabricate ultra-small and high edge definition silicon nanowires and nanodiscs on SOI. This technique can also be used to fabricate large density of nanowires and nanowire networks over BOX. Furthermore, using metal lift-off process, the nanowires and nanodiscs on BOX have been contacted with metal film through the sides. The metal film encircled nanostructure samples would be useful for future STM analysis of quasi 1D and 2D SOI nanostructures.

6.7 References

1. Herring, C. and J.K. Galt, *Elastic and Plastic Properties of Very Small Metal Specimens*. Physical Review, 1952. **85**(6): p. 1060-1061.
2. Priolo, F., et al., *Silicon nanostructures for photonics and photovoltaics*. Nat Nano, 2014. **9**(1): p. 19-32.
3. Duan, X., J. Wang, and C.M. Lieber, *Synthesis and optical properties of gallium arsenide nanowires*. Applied Physics Letters, 2000. **76**(9): p. 1116-1118.
4. Boukai, A.I., et al., *Silicon nanowires as efficient thermoelectric materials*. Nature, 2008. **451**(7175): p. 168-171.
5. Wu, Z., J.B. Neaton, and J.C. Grossman, *Quantum Confinement and Electronic Properties of Tapered Silicon Nanowires*. Physical Review Letters, 2008. **100**(24): p. 246804.
6. Hodes, G., *When Small Is Different: Some Recent Advances in Concepts and Applications of Nanoscale Phenomena*. Advanced Materials, 2007. **19**(5): p. 639-655.
7. Canham, L.T., *Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers*. Applied Physics Letters, 1990. **57**(10): p. 1046-1048.
8. Leão, C.R., A. Fazzio, and A.J.R. da Silva, *Si Nanowires as Sensors: Choosing the Right Surface*. Nano Letters, 2007. **7**(5): p. 1172-1177.
9. Guisbiers, G., et al., *Mechanical and thermal properties of metallic and semiconductive nanostructures*. The Journal of Physical Chemistry C, 2008. **112**(11): p. 4097-4103.
10. Lopeandía, A.F. and J. Rodríguez-Viejo, *Size-dependent melting and supercooling of Ge nanoparticles embedded in a SiO₂ thin film*. Thermochemica Acta, 2007. **461**(1): p. 82-87.
11. Sun, J. and S.L. Simon, *The melting behavior of aluminum nanoparticles*. Thermochemica Acta, 2007. **463**(1): p. 32-40.
12. Teo, B.K. and X.H. Sun, *Silicon-Based Low-Dimensional Nanomaterials and Nanodevices*. Chemical Reviews, 2007. **107**(5): p. 1454-1532.

- 13.Cui, Y. and C.M. Lieber, *Functional Nanoscale Electronic Devices Assembled Using Silicon Nanowire Building Blocks*. Science, 2001. **291**(5505): p. 851-853.
- 14.Huang, Y., et al., *Logic Gates and Computation from Assembled Nanowire Building Blocks*. Science, 2001. **294**(5545): p. 1313-1317.
- 15.Lauhon, L.J., et al., *Epitaxial core-shell and core-multishell nanowire heterostructures*. Nature, 2002. **420**(6911): p. 57-61.
- 16.Chen, F., et al., *Quantum Confinement, Surface Roughness, and the Conduction Band Structure of Ultrathin Silicon Membranes*. ACS Nano, 2010. **4**(4): p. 2466-2474.
- 17.Shahidi, G.G. *SOI technology for the GHz era*. in *2001 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers (Cat. No.01TH8517)*. 2001.
- 18.Ma, D.D.D., et al., *Small-Diameter Silicon Nanowire Surfaces*. Science, 2003. **299**(5614): p. 1874-1877.
- 19.Danielson, D.T., et al., *Surface-energy-driven dewetting theory of silicon-on-insulator agglomeration*. Journal of Applied Physics, 2006. **100**(8): p. 083507.
- 20.Ishikawa, Y., et al., *Effect of patterning on thermal agglomeration of ultrathin silicon-on-insulator layer*. Applied Surface Science, 2002. **190**(1): p. 11-15.
- 21.Plateau, J., Transl. Annual Reports of the Smithsonian Institution, 1873: p. 1863.
- 22.Rayleigh, L., *On The Instability Of Jets*. Proceedings of the London Mathematical Society, 1878. **s1-10**(1): p. 4-13.
- 23.Nichols, F. and W. Mullins, *SURFACE- AND VOLUME-DIFFUSION CONTRIBUTIONS TO MORPHOLOGICAL CHANGES DRIVEN BY CAPILLARITY*. AIME MET SOC TRANS, 1965. **233**: p. 1840-1848.
- 24.Kolb, F.M., et al., *On the morphological instability of silicon/silicon dioxide nanowires*. Applied Physics A, 2005. **80**(7): p. 1405-1408.
- 25.Misra, N., et al., *Pulsed laser annealing of semiconductor structures for functional devices*. physica status solidi (c), 2008. **5**(10): p. 3264-3270.

26. Ishikawa, Y., et al., *Pattern-induced alignment of silicon islands on buried oxide layer of silicon-on-insulator structure*. Applied Physics Letters, 2003. **83**(15): p. 3162-3164.

7

CONCLUSIONS AND FUTURE WORK

A simple oxygen plasma treatment has been found to effectively clean and thin device layers of SOI. The cleaning technique produces an atomically smooth and flat device layer. Using a thermal gradient flash annealing strategy, various stages of oxide desorption and evolution of the surface morphology of SOI were investigated simultaneously. Furthermore, an effective low thermal budget SOI cleaning process was developed and used throughout this work.

Through STM analysis of SOI, the role of the spreading resistance due to the extremely small tunneling contact in STM and high sample resistivity was investigated. It was demonstrated that, with appropriate doping levels, SOI with a varying device layer thicknesses down to 5 nm can be analysed using STM. STM analysis has shown that SOI films with device layer thicknesses down to 5 nm show STS and ER spectra features very similar to bulk silicon.

Analysis of SOI with thicknesses below 4 nm have shown that annealing leads to faceting of the film and an increase in surface roughness. The roughness of the film was shown to exhibit peaks and troughs associated with matter waves. Based on these observations we propose that the roughness results from thickness fluctuations in the ultra-thin SOI due to thermal excitation. KPM measurements revealed the presence of an ultra-thin wetting layer that physically and electrically connects the dewetted crystals, and which we suggest is due to a Van der Waal mediated pinning interaction between the film-vacuum and film-substrate interfaces that prevent complete dewetting.

Although these analysis have shown a transition in the qualitative nature of the thermomechanical stability in ultra-thin SOI, further analysis needs to be

carried out to quantitatively evaluate the SOI system. Investigation of morphological evolution of the annealed Si film as a function of film thickness would help determine the pathways of dewetting in ultra-thin SOI. These analysis will also provide an insight into the thickness dependent transition and the evolution of the thermomechanical behaviour from the classical to the non-classical regime. These analysis would also enable the calculation of effective interfacial potential for ultra-thin SOI.

STM measurements of flash annealed SOI nanowires showed that the surface oxide on the nanowires can be desorbed at lower temperatures in comparison to a flat silicon surface. Diffusion of silicon due to capillary forces is believed to supply silicon adatoms necessary for oxide desorption and expedite the cleaning process. The low temperature processing protects the integrity of nanowires and makes the STM analysis possible.

Finally, a simple ultra-small nanowire and nanodisc fabrication technique was demonstrated which enables the fabrication of structures that are below present EBL resolution capabilities ($< 10\text{nm}$). There are significant advantages of the fabrication technique. Apart from the ability to fabricate ultra-small structures, the technique can produce an extremely high density of nanowires with a low edge roughness. Additionally, the metal film in encircling the SOI nanostructures can electronically couple with the nanostructures and allow STM measurements. In terms of future work, a logical next step would be to investigate the properties of the metal encircled quasi 1D and 2D Silicon-on-Oxide structures to understand the effective coupling of charges in and out of the ultra-small Si structures and subsequently to measure their electronic properties. Metal encircled crystalline Si nanostructures may form ideal structures to study quantum confinement in silicon.