



Characterization of Rapid Melt Growth (RMG) Process for High Quality Thin Film Germanium on Insulator

Nurfarina Zainal, S.J.Neil Mitchell, David W. McNeill, Micheal F. Bain, B.M. Armstrong, Paul T. Baine, David Adley and Tatania S. Perova

ECS Trans. 2012, Volume 45, Issue 4, Pages 169-180. doi: 10.1149/1.3700467

Email alerting service Receive free email alerts when new articles cite this article - sign up in the box at the top right corner of the article or click here

To subscribe to ECS Transactions go to: http://ecst.ecsdl.org/subscriptions

ECS Transactions, 45 (4) 169-180 (2012) 10.1149/1.3700467 ©The Electrochemical Society

Characterization of Rapid Melt Growth (RMG) Process for High Quality Thin Film Germanium on Insulator

N. Zainal^{a,c}, S. J. N. Mitchell^a, D. W. McNeill^a, M. F. Bain^a, B. M. Armstrong ^a, P. T. Baine ^a, D. Adley ^b, T. S. Perova ^b

Germanium is one of the most promising materials for high performance infra-red photovoltaic devices. High quality singlecrystal germanium on insulator structures can be produced by a Rapid Melt Growth process. Experiments show that thin-film germanium deposited by physical vapor deposition provides better quality in comparison with chemical vapor deposition. The longitudinal optical Ge-Ge peak in Raman spectrum is shifted from the expected 300.2 cm⁻¹ position due to tensile stress resulting from the thermal expansion differences of the materials. The importance of silicon in the rapid melt process is confirmed by the fact that germanium films on sapphire substrates yielded polycrystalline structure. Films produced at high temperature (980 °C) show Ge-Ge Raman peak with linewidth of 3.3 cm⁻¹ indicating good crystalline quality, comparable to bulk germanium (3.2 cm⁻¹), and thus demonstrating the potential to produce low cost high quality germanium films.

Introduction

Semiconductor based photovoltaic technology has been developed for more than 20 years using a range of techniques and materials with first invention being silicon based. Research has aimed to improve the energy conversion efficiency and reduce the manufacturing cost [1, 2]. At present, multi-junction solar cells show the highest performance, but have complex and expensive manufacturing processes [3, 4]. By developing a deposition and growth technique with good material electrical properties, a low cost and high quality solar cell can be produced. Germanium has been chosen because it has excellent electrical properties. With a band gap of Eg=0.66 eV [5] energy from the infra red region of the solar or thermal spectrum can be absorbed and converted into electrical energy. The issues of availability and cost can be overcome by using thin-films instead of thick wafers of germanium. Solid-state structures can be produced using low cost thin-film deposition techniques combined the rapid melt growth (RMG) process. High-quality single crystal thin-films of germanium produced by RMG can provide a germanium on insulator (GeOI) structure. Initial experiments on integration of GeOI with

Northern Ireland Semiconductor Research Centre, School of Electronics, Electrical Engineering & Computer Science, Queen's University, Belfast, BT9 5AH, UK
Department of Electronic and Electrical Engineering, University of Dublin, Dublin 2, Ireland

^c Department of Electrical and Electronics Engineering, Universiti Tun Hussein Onn Malaysia, 86400 Parit Raja, Batu Pahat, Johor, Malaysia

silicon and sapphire substrates have demonstrated that good quality germanium crystalline structure can be obtained as shown by micro-Raman spectroscopy.

Materials and Methods

In this work, two techniques have been used for deposition of germanium, namely physical vapor deposition (PVD) and chemical vapor deposition (CVD). The process parameters are also varied, aiming for an optimal germanium crystalline structure and to verify the lateral growth of germanium on insulator. The parameters include germanium thickness, crucible materials (silicon dioxide, hafnium dioxide), anneal temperature and substrate.

The rapid melt growth (RMG) process uses a micro-crucible to hold the molten germanium [6, 7]. The crucible is formed on the surface of an oxidized silicon wafer with the germanium contacting the silicon in a seed window. In the fabrication process for PVD samples, the germanium is deposited directly on top of the oxide. The germanium chemical vapor deposition process, however, is selective to silicon surfaces and thus requires a thin silicon layer to be deposited on the oxide prior to the germanium deposition. The deposited germanium is then patterned into narrow stripe features with 3 to 4µm width and 60 to 400µm lengths. These stripes are then covered with a capping layer of low temperature oxide to form the micro-crucible as shown in figure 1(a). Rapid thermal annealing (RTA) is applied to heat the germanium above its melting point (938 °C) for a few seconds. After annealing, the germanium cools and crystallizes starting from the silicon seed and continuing laterally along the crucible. The seed region is expected to be defective because of the lattice mismatch between silicon and germanium. The dislocations will extend out from the seed region but terminate at the micro-crucible walls, and thus good crystalline quality can be obtained beyond this region. A surface view of the structure with seed region of 60µm length and 3 to 4µm width germanium stripes is shown in the Scanning Electron Microscopy image, figure 1(b). Straight, smooth stripes with no delamination are observed before heat treatment (anneal) of the sample. During the RTA, the crucible can become strained due to the germanium balling phenomenon [8]. In our work the capping layer was reinforced using a polycrystalline silicon layer which was found to be essential in minimizing germanium balling and delamination [9]. The quality of germanium crystalline structure is examined by micro-Raman spectroscopy with Scanning Electron Microscopy (SEM), used for imaging.

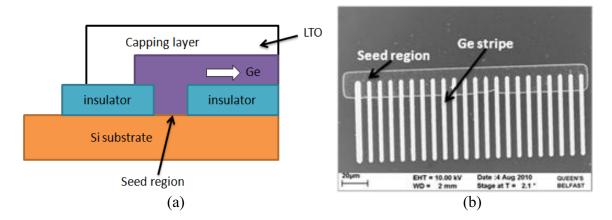


Figure 1. (a) Schematic diagram (not to scale) of rapid melt growth process with low temperature oxide (LTO) as a capping layer. (b) Micrograph of germanium stripes before annealing process.

Results and Discussions. In the case of a capping layer comprising only low temperature oxide (PECVD oxide), significant cracks and delamination of the stripes are observed and crucible integrity is compromised as shown in figure 2. This is because when heat treatment is applied above germanium melting point (938 °C), it tends to form into ball shapes (balling phenomenon) [8] causing the crucible to become strained. The issue is more severe with wide stripe since micro-crucible cap is wider and hence less rigid.

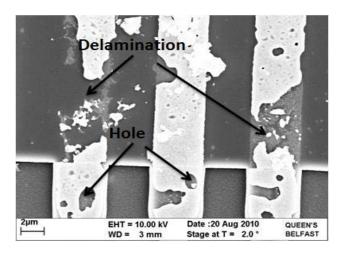


Figure 2. Micrograph showing cracks and delamination of germanium stripe with only PECVD oxide cap after annealed at 942 °C for 1 second.

During the heat treatment to melt the germanium, the oxide capping layer may also undergo structural changes. This was investigated by performing various heat treatments on oxide test samples. The etch rate is used as an indication of material density since high density corresponds to low etch rates. Figure 3 shows that the etch rate falls sharply with anneal temperature until approximately 800 °C where the rate of change reduces. The oxide thickness is linearly dependent to the temperature with 5% reduction observed at

1000 °C as shown in figure 4. This shrinkage in the oxide provides addition space for the molten germanium to flow and may contribute to the crack formation.

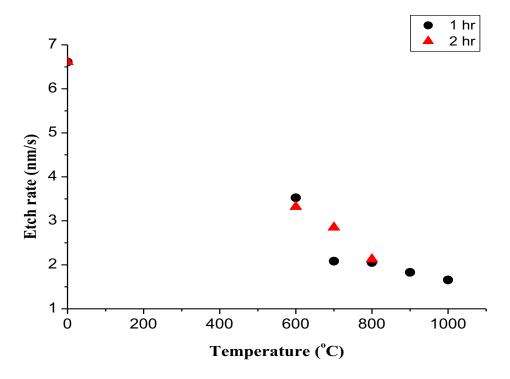


Figure 3. Graph of oxide etch rate (nm/s) versus annealing temperature (°C).

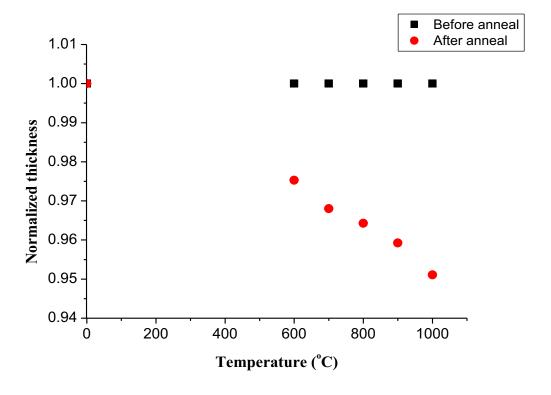


Figure 4. Normalized graph of oxide thickness versus temperature (°C) before and after the annealing process.

The micro-crucible was reinforced by adding a 1 μ m thick poly-crystalline silicon (polysilicon) layer on top of the PECVD oxide capping layer. The polysilicon was deposited by low pressure chemical vapor deposition (LPCVD) at 620 °C. Addition of this layer was found to minimize germanium balling and prevent delamination, with a smooth layer of germanium stripes observed in figure 5(a) and (b). These defect free structures are observed for 60 to 400 μ m length with 170nm thick PVD germanium stripes. A 1 second RTA at 942 °C was used.

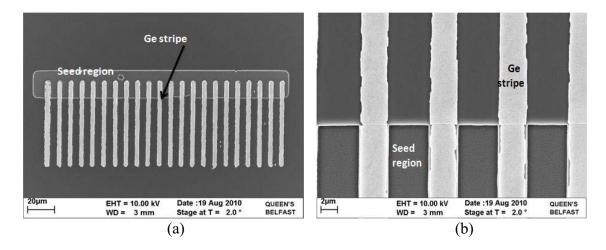


Figure 5. (a) and (b) Micrographs showing germanium stripes produced using microcrucible comprising polysilicon on top of PECVD oxide.

The crystalline structure of 170nm thick PVD germanium stripe was analyzed by micro-Raman Spectroscopy with bulk (single crystal) germanium used as a reference. The Raman spectrum of bulk crystalline Ge demonstrates an intense longitudinal-optical phonon (LO) Ge-Ge mode with peak position at 300.2 cm⁻¹ and the linewidth (or full width at half maximum (FWHM)) of ~ 3 cm⁻¹. The presence of tensile or compressive strain in the structure will result in shift of this LO peak to the low- or high-frequency side, respectively. Prior to rapid melt growth (RMG) the Raman spectrum in figure 6 demonstrates a relatively wide Ge-Ge peak with a FWHM of ~8 cm⁻¹ compared to the bulk germanium reference sample with FWHM = 3.2 cm⁻¹. Along with the asymmetry, observed from the low frequency side of the peak, this suggests the presence of some amorphous content as well as polycrystalline nature of the structure. This partial crystal growth occurs in the germanium during the deposition of the capping layer at up to 620 °C. After RMG the Raman spectra (figure 6) shows a sharp and symmetric peak (with FWHM of <4 cm⁻¹) indicating an improved crystalline quality of Ge stripe compared to the unannealed sample.

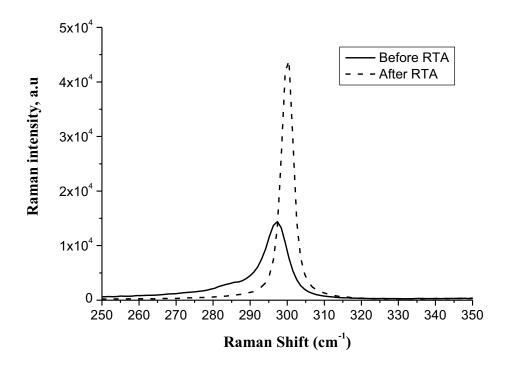


Figure 6. Raman spectra before and after rapid thermal anneal.

The comparison of Raman spectra, registered from the Ge stripe annealed at 942 °C after RMG and from n-type bulk Ge (reference sample) is shown in figure 7. One can see that the spectra are practically identical, indicating good crystalline quality germanium in the stripe.

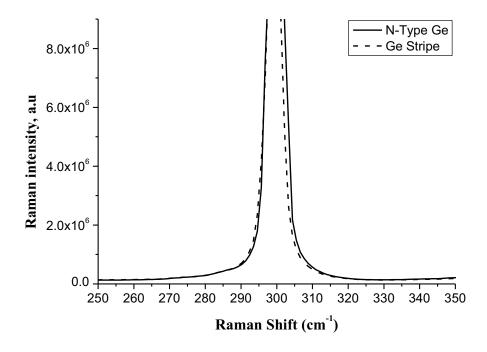


Figure 7. Spectral comparisons of germanium stripe after RMG process with single crystal germanium.

Micro-Raman line-mapping measurements were also carried out along the length of PVD germanium stripe for samples annealed at higher temperature (980 °C) with thickness of 170 nm and 210 nm. A uniform stress distribution along the stripe is obtained for both thicknesses with Ge-Ge peak position at 299.5 cm⁻¹ as shown in figure 8, slightly lower than that for the bulk germanium at 300.2 cm⁻¹. This shift in peak position indicates a small tensile stress which is due to the difference of thermal expansion coefficients between the germanium and micro-crucible materials. A discontinuity in the Raman line-mapping profiles is observed at the edge of the seed window. This is thought to be due to a change in surface gradient and in some cases the presence of micro cracks after removal of the capping layer.

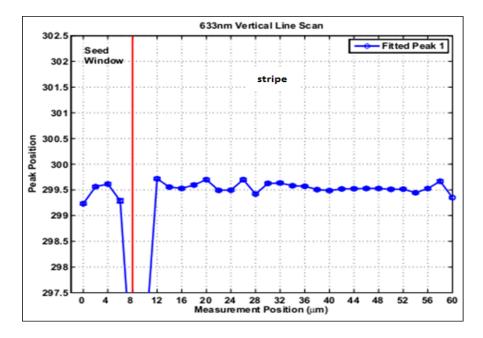


Figure 8. Peak position of germanium finger stripe annealed at 980 °C showing a uniform stress distribution along the stripe outside the seed window.

The crystalline quality of the sample annealed at 980 °C is also improved compared to the sample treated at 942 °C with the FWHM for the 170nm germanium stripe of ~3.3 cm⁻¹ [9] being almost identical to that for the bulk Ge (~3.2 cm⁻¹). A slightly increased linewidth (FWHM ~3.6 cm⁻¹) is observed for the 210nm thick germanium stripe due to the rougher surface. Figure 9 shows that the spectrum from the seed area has a wider peak compared to the stripe region due to dislocations caused by silicon and germanium lattice mismatch. The dislocations do not extend along on the germanium stripe.

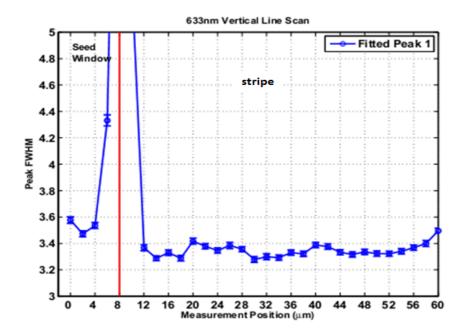


Figure 9. FWHM peak of germanium stripe annealed at 980 °C showing dislocation does not extend along the stripe.

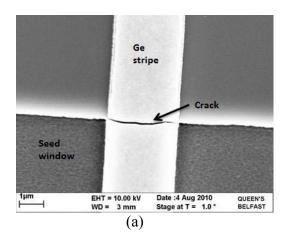
In case of the CVD samples, no cracks and delamination is observed after annealing at higher temperature (≥1000 °C) and removal of capping layer. However, a rougher surface is produced with less uniform stress distribution revealed by the Ge-Ge peak position and a degraded germanium crystalline quality as confirmed by larger linewidth (with FWHM varied within ~5−8 cm⁻¹) obtained during line mapping Raman measurements. In contrast, PVD films show a longer distance of uniform stress distribution and FWHM as annealing temperature increases.

<u>Insulator Layer and Substrates</u>. During the rapid melt process, the molten germanium is in contact with the inner walls of the micro-crucible. Interaction between the germanium and these surfaces can influence the structure of the resultant germanium stripes. Typical dielectric materials used for the crucible are silicon dioxide or silicon nitride. Hafnium dioxide is an alternative material which has a high dielectric constant and is employed in the gate stack of advanced MOS devices. Early work has shown that the use of silicon nitride does not allow good quality crystallized germanium films to be obtained due to a significant tendency for the molten germanium to balling.

Hafnium dioxide (HfO₂) is investigated as insulator and crucible layer and compared to the silicon dioxide. A 20nm HfO₂ layer is deposited on top of oxidized silicon using atomic layer deposition (ALD) and patterned to form a seed window. A 170nm thick PVD germanium layer is then deposited and patterned into narrow stripes which run from seed window along the hafnium dioxide surfaces. These stripes are then covered with a 20nm thick hafnium dioxide, $1\mu m$ of PECVD oxide and $1\mu m$ of polysilicon that act as capping layers. A higher annealing temperature (≥ 1000 °C) has been applied. The polysilicon and PECVD oxide capping has been removed using polysilicon etch and

buffered HF after the annealing process. However, HfO₂ cap is difficult to etch after high temperature treatment, therefore the HfO₂ cap layer is not removed.

In case of SiO_2 as insulator layer, cracks in the stripe occur at the edge of the seed window after removal of the polysilicon and oxide cap for the 170nm germanium thickness after the RMG process. However, the stripe has a smooth surface as shown in figure 10 (a). No cracks are observed at the step between seed HfO_2 window and stripes for 60μ m to 400μ m. On the other hand, the germanium surface is rougher as observed on the SEM images shown in figure 10(b).



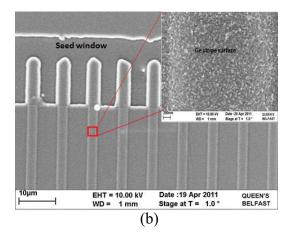


Figure 10. Micrograph of (a) germanium stripe on silicon dioxide after annealing at 980 °C and (b) HfO₂ samples after ≥ 1000 °C annealing temperature for 60μ m distance.

Compared to germanium on silicon dioxide the FWHM of LO Raman peak registered from Ge stripe on hafnium dioxide is slightly wider (~3.9 cm⁻¹), this is believed to be due to the increased surface roughness. The peak position observed at 299.3 cm⁻¹ is slightly lower than that for the bulk Ge at 300.2 cm⁻¹ as expected, indicating a small tensile stress due the differences thermal expansion coefficient of materials. In terms of semiconductor devices, tensile strain in germanium is useful as it provides a significant impact on the band structure that will results in increase of the electron mobility and thus, enhance the optoelectronics properties [10, 11].

Silicon Germanium (SiGe) Content. In case of CVD germanium, it is necessary to grow first a thin silicon layer on the oxide to enable the selective germanium deposition. This is because it is impossible to deposit germanium by CVD on the oxide but only selective onto silicon. Therefore, thin silicon layer is required to be deposited on oxide prior to the CVD germanium deposition. After the RMG process, the Raman spectrum shows a sharp Ge-Ge peak at 300 cm⁻¹ with FWHM of < 4 cm⁻¹ for both CVD and PVD samples. This indicates a good crystalline quality of germanium stripes comparable to the bulk Ge (FWHM = 3.2 cm⁻¹) as shown in figure 11. The peak position for both samples is slightly shifted to the low-frequency side due to the tensile strain. A peak corresponding to SiGe bonding is observed in the Raman spectrum around 380-390 cm⁻¹ in case of CVD sample annealed at $T \ge 940$ °C.

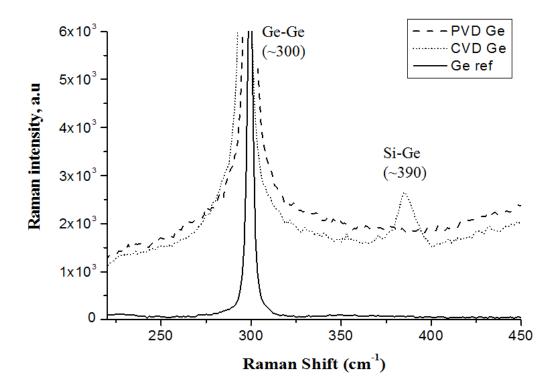


Figure 11. Raman spectra for bulk germanium reference, PVD and CVD samples after RMG at a distance of 36µm from the seed window.

The presence of SiGe is believed to result from the thin silicon layer. Miyao et al. [7] observed a similar SiGe peak in the RMG germanium grown by molecular beam epitaxy and attributed this to silicon diffusion from the seed window. In our PVD samples SiGe was not found even for high temperature (≥1000 °C) annealing where diffusion of silicon from the seed window might be expected.

It has been suggested that the lateral crystallization is driven by either silicon concentration gradient [7] or thermal gradient from the seed window [12] or a combination of both [12, 13]. In the case of the thermal gradient, the seed window provides a heat sink during temperature ramp down at the end of the RTA. This causes the germanium close to the seed to solidify first and crystallization progresses along the stripe. In the silicon gradient case, the higher silicon content at the seed results in a higher melting point and again on cooling this region solidifies first. To explore the driving mechanism the micro-crucible was fabricated on a sapphire substrate, producing a structure with no source of silicon.

A 50nm silicon dioxide layer was deposited on the sapphire using PECVD and patterned to make a seed window. A 170nm thick PVD germanium layer is deposited covering the seed area and silicon dioxide and then patterned into narrow stripes. A 1µm PECVD oxide and 1µm polysilicon layers were deposited on germanium to act as the capping layer. After RTA at 985 °C, the capping layer was removed and Raman spectroscopy was used to investigate the crystalline quality. As expected no SiGe or silicon peaks were present. The Ge-Ge peak shown in figure 12 has a FWHM value of

~6.4 cm⁻¹ as well as asymmetry from low-frequency side of spectra, indicating that the Ge stripe has polycrystalline structure with some amorphous content. This suggests that the presence of silicon is necessary for optimum crystalline quality. No delamination is observed on the SEM image with 170 nm thick PVD germanium. It was also found that the sapphire substrate provides less tensile stress (as negligible shift in peak position is observed). This is due to the thermal expansion coefficient of sapphire being more closely matched to that germanium compared to silicon.

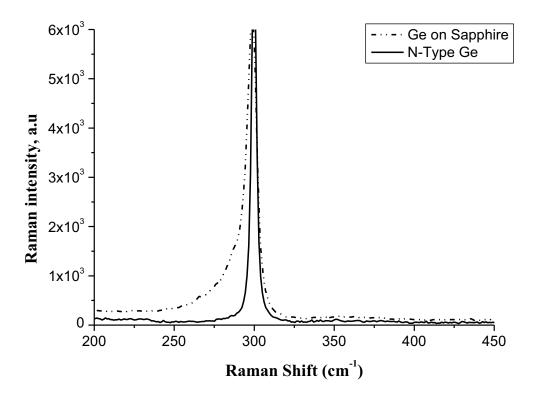


Figure 12. Raman spectra of germanium on sapphire substrate.

Conclusions. PECVD oxide capping alone is not rigid enough to hold the molten germanium resulting in cracks and delamination. Reinforcing the crucible with a polysilicon cap on top of the PECVD oxide provides robust capping layers thus prevents balling and delamination. In contrast to thermal treatment at 942 °C, a higher annealing temperature provides a better crystalline quality of PVD deposited Ge films. This is confirmed by uniformity of Raman spectra characteristics (the peak position and FWHM) extended further away from the seed window. The rougher surface of PVD Ge films on hafnium dioxide results in a slight widening of the Ge spectra. In contrast to samples with CVD germanium, no SiGe spectrum was traced for PVD samples even annealing at high temperature (≥1000 °C). This proves that the intermixing of Si and Ge is due to the thin silicon layer deposited prior to the germanium in the CVD process and not because of the diffusion of silicon from the seed window. CVD samples demonstrate less uniform Raman spectra with degradation of germanium crystal quality as annealing at high temperature (≥1000 °C) in contrast to PVD films. In the absence of a silicon seed, which was the case for samples on sapphire substrate, a lower quality germanium crystal structure (polycrystalline with some amorphous content) was observed. This indicates that silicon diffusion is an important mechanism in the rapid melt process. It is believed that the thermal flow from seed window is causing the germanium lateral growth. Results from micro-Raman Spectroscopy shows that good quality of germanium stripes can be obtained from rapid melt growth (RMG) process. This technology thus has potential to produce a low cost, high-quality future semiconductor solar cell.

Acknowledgments

The authors wish to thank the financial support from Ministry of Higher Education Malaysia and the Royal Society/Royal Irish Academy. D.A. acknowledges the financial support from IRCSET (Ireland) Postgraduate Award.

References

- 1. S. S. Sun, N. S. Sariciftci, *Organic Photovoltaics Mechanism, Materials and Devices*, Editors, p. 19, Taylor & Francis Group (2005).
- 2. A. Ennaoui, S. Fiechter, Ch. Pattenkofer, N. Alonso-Vante, K. Buker, M. Bronold, Ch. Hopfner and H. Tributsch, *Sol. Energy Mater. Sol. Cells* **29**, (1993).
- 3. G. W. Crabtree and N. S. Lewis, *Physic today*, **60**, (2007)
- 4. C. Wadia, A. P. Alivisatos and D. M. Kammen, Environ. Sci. Technol. 43, (2009).
- 5. B. Bitnar, Semicond. Sci. Technol., 18, (2003).
- 6. Y. Liu, M. D. Deal, J. D. Plummer, J. Electrochem. Soc., 152, 8 (2005).
- 7. M. Miyao, K. Toko, T. Tanaka and T. Sadoh, *App. Phys. Lett.* **95**, 022115 (2009).
- 8. S. Balakumar, M. M. Roy, B. Ramamurthy, C. H. Tung, G. Fei, S. Tripathy, C. Dongzhi, R. Kumar, N. Balasubramanian and D. L. Kwong, *Electrochem. Solid-State Lett.*, **9**, 5 (2006).
- 9. N. Zainal, S. J. N. Mitchell, D. W. McNeill, M. F. Bain, B. M. Armstrong, P. T. Baine, D. Adley and T. S. Perova, *UK Semicond. Conf.*, (2011).
- 10. J. Michel, J. Liu and L. C. Kimerling, *NPhoton* **4**, 157 (2010).
- 11. E. E. Haller, Mat. Sci in Semicond. Pros. 9, (2006).
- 12. K. Toko, T. Sakane, T. Tanaka, T. Sadoh and M. Miyao, *App. Phys. Lett.* **95**, 112107 (2009).
- 13. T. Sadoh and M. Miyao, ECS Trans., 33, 6 (2010).