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Investigation of Transport Through Interfacial Barriers Between Metals and Semiconductors

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Thesis presented for the degree of
Doctor of Philosophy
to the
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Declaration

This thesis is submitted by the undersigned for examination for the degree of Doctor of Philosophy at the University of Dublin. It has not been submitted as an exercise for a degree at any other university.

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For Adam and Paul

Abstract

Electrical spin injection from a ferromagnetic metal source into a semiconductor can only take place through an interfacial barrier (Rashba, Phys. Rev. B **62**, R16267 and Phys. Rev. B **68**, 241310). This thesis presents a study of electrical transport through what can be roughly described as two different junction systems, ferromagnetic metal / semiconductor junctions and ferromagnetic metal / insulator / semiconductor junctions to assess their potential for incorporation into spintronic devices. Transport was studied as a function of semiconductor material, silicon and gallium arsenide, spin injector source, Fe_3O_4 and $\text{Co}_{90}\text{Fe}_{10}$, temperature, insulator material, AlO_x and MgO , and thickness and finally as a function of junction size. The systems can be broken down as follows; GaAs / Fe_3O_4 , Si / Fe_3O_4 , GaAs / AlO_x / $\text{Co}_{90}\text{Fe}_{10}$, GaAs / MgO / $\text{Co}_{90}\text{Fe}_{10}$, Si / AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ and Si / MgO / $\text{Co}_{90}\text{Fe}_{10}$. The tunnel barrier (insulator) thickness was increased from 0 nm in 1 nm steps. Most junctions were fabricated on mid n-type substrates but initially mid p-type and high n and p-type were also used.

Transport through the metal / high doped semiconductor substrates was determined to be dominated by thermionic field emission. All metal / medium doped semiconductor junctions displayed rectifying behaviour, which is characteristic of a Schottky barrier at the metal / semiconductor interface. The introduction of a tunnel barrier, regardless of the material, also displayed rectifying behaviour. A distortion in the forward bias part of the curves due to tunneling was observed and the magnitude of this distortion varied from system to system. In all systems, however, it increased as a function of barrier thickness. In two cases the incorporation of a barrier led to an increase in the reverse bias current, which in this case is the current where spin is injected into the semiconductor, potentially increasing spin injection efficiency. Where possible all junctions were fitted to the thermionic emission / diffusion model to extract the Schottky barrier height, ϕ_B .

As the junctions went from being micro to nano-junctions the barrier height reduced dramatically, which should increase spin injection efficiency. Overall the results presented here have positive implications for the incorporation of some of the studied systems into future spintronic devices, especially for nano scaled devices.

Brief Summary

The focus of this thesis was to investigate and characterise electrical transport through different interfacial barriers formed on Si and GaAs semiconductors when a ferromagnetic metal is grown on top of these substrates. This characterisation is very important in the aid of realising usable and commercial Si and GaAs based spintronic devices. Two different ferromagnetic metals were used, Fe_3O_4 and $\text{Co}_{90}\text{Fe}_{10}$. Fe_3O_4 is a half metal and so theoretically has full spin polarization and $\text{Co}_{90}\text{Fe}_{10}$ has the highest spin polarization of all Co-Fe alloys. The metallic films were grown by DC sputtering and the electrical transport is measured as a function of temperature using a cryostat in a resistivity rig. The substrates used were predominantly mid n-type but initially mid p-type and high p and n-type GaAs substrates were also used. A thin insulating layer was introduced as a tunnel barrier between the $\text{Co}_{90}\text{Fe}_{10}$ films grown on Si and GaAs substrates. Two different insulating materials were used, AlO_x and MgO , which were grown by RF sputtering. In this case the junctions were patterned into two sizes, $50 \times 50 \mu\text{m}$ squares by UV lithography and 100 nm circular junctions by e-beam lithography. The barrier thickness was increased from 0 nm in 1 nm steps and the junctions were characterized as a function of barrier thickness as well as temperature. Film quality and crystal structure was characterised using X-ray diffraction and a superconducting quantum interface device magnetometer.

In all cases transport through the medium doped semiconductors displayed rectifying behaviour, asymmetric $I - V$ curves, which is characteristic of transport through a Schottky barrier. A distortion in the forward bias part of the curves due to tunneling was observed in the junctions where a tunnel barrier was present. The magnitude of this distortion varied from system to system but in all tunnel barrier systems it increased as a function of decreasing temperature and increasing barrier thickness. In two cases the incorporation of a barrier led to an increase in the reverse bias current, which in this case is the current where spin is injected into the semiconductor, potentially increasing spin injection efficiency. Unfortunately in some cases the distortion was so great that it

was impossible to fit the data to the thermionic emission / diffusion model. Transport through a Schottky barrier is via thermionic emission / diffusion through the barrier and this model is used to extract the barrier height, ϕ_B , along with the associated ideality factor, n . and where possible all junctions were fitted to it.

By comparing barrier heights it was observed that the increase in current was mirrored by a decrease in barrier height. By far the most effective way to reduce the barrier height is by reducing the size of the junctions down to the nm range. For example the barrier height at $\text{Co}_{90}\text{Fe}_{10}$ / Si interface is 0.51 eV when the junction size is $50 \times 50 \mu\text{m}$ but is reduced to only 0.11 eV for the circular 100 nm junction. Similar barrier height reductions were seen where they could be compared.

As for highly doped substrates, transport through the ferromagnetic metal / semiconductor junction is dominated by thermionic field emission. In this case, electrons and holes tunnel through the Schottky barrier, resulting in nonlinear but nearly symmetric $I - V$ curves.

Overall these results have identified some obstacles and some interesting possibilities for spin injection from Fe_3O_4 and $\text{Co}_{90}\text{Fe}_{10}$ sources into Si and GaAs semiconductors with and without a tunnel barrier.

Contents

1	Introduction	1
1.1	Spintronics	1
1.1.1	History of Spintronics	2
1.2	Brief Introduction to Silicon and Gallium Arsenide	7
1.2.1	Crystal Structure	7
1.2.2	Band Gap	10
1.2.3	Resistivity, Mobility and Hall Effect	13
1.3	Schottky Barriers	17
1.3.1	Forward and reverse bias	21
1.3.2	Current Transport Mechanisms	22
1.4	Tunnel Barriers	33
2	Experimental Techniques	46
2.1	Sample Deposition	46
2.1.1	Magnetron Sputtering	46
2.1.2	Leybold Sputtering System	46
2.1.3	Shamrock Sputtering System	47
2.1.4	Thermal Evaporation	52
2.2	Structure Characterization	53
2.2.1	X-ray analysis	53
2.2.2	Transmission Electron Microscopy (TEM)	56
2.2.3	Superconducting Quantum Interface Device (SQUID)	57
2.3	Junction Fabrication Process	58
2.3.1	Ultra Violet (UV) Lithography	58
2.3.2	E-beam Lithography	59
2.3.3	Ion Milling Process with an End Point Detector	61
2.3.4	Junction Isolation	63
2.3.5	Ohmic Back Contacts	63

2.4	Transport Measurements	64
2.4.1	The RT Rig	64
2.4.2	Van der Pauw Technique	65
3	Magnetite / Semiconductor Junctions	71
3.1	Introduction	71
3.1.1	Half Metals	71
3.2	Magnetite on differently doped Gallium Arsenide substrates	75
3.2.1	Introduction to the Experiment	75
3.2.2	Fe ₃ O ₄ Film Structure on GaAs (001) Substrates	76
3.2.3	Verwey Transition	77
3.2.4	Electrical Transport	78
3.3	Magnetite on mid n-type Silicon substrates of different orientations	85
3.3.1	Introduction to the Experiment	85
3.3.2	Fe ₃ O ₄ film structure on Si substrates	86
3.3.3	Magnetic Properties of the films	87
3.3.4	Electrical Transport	89
3.3.5	Interface properties	92
3.4	Conclusions and Summary	97
4	Metal / Insulator / Semiconductor Systems	104
4.1	Introduction	104
4.1.1	Insulators	105
4.2	Co ₉₀ Fe ₁₀ on n-type Silicon substrates	107
4.2.1	Introduction	107
4.2.2	Film structures on Si substrates	109
4.2.3	Magnetic properties of the Co ₉₀ Fe ₁₀ films	115
4.2.4	Electrical Transport, 50 × 50 μm sized Junctions	116
4.2.5	Electronic Transport, 100 nm Junctions	131
4.2.6	Interface Properties	143
4.3	Co ₉₀ Fe ₁₀ on n-type Gallium Arsenide substrates	143
4.3.1	Introduction	143
4.3.2	Film Structure	145
4.3.3	Electrical Transport, 50 × 50 μm sized Junctions	146
4.3.4	Electronic Transport, 100 nm Junctions	159
4.4	Resistance	171
4.4.1	Semiconductor Resistance	172

4.4.2	Contact Resistance	175
4.4.3	Tunnel Barrier Resistance	176
4.5	Conclusions and Summary	178
5	Summary and Future Work	187
5.1	Summary	187
5.2	Future Work	192
5.3	Publications	193
A	Depletion Region Approximation	196
A.1	The Depletion Region Approximation	196
B	LabVIEW Programs	201
B.1	Introduction	201
B.2	Transport as a Function of Temperature	201
B.2.1	Barrier Height and Ideality Factor Calculation	205
B.3	Activation Energy Plot	206
B.4	Van der Pauw Technique	210
B.4.1	Resistivity Calculation	210
B.4.2	Semiconductor type and Carrier Concentration	215

List of Figures

1.1	Schematic of Schmidt <i>et. al.</i> model	3
1.2	Conductivity mismatch problem	4
1.3	Schematic of Rashba <i>et. al.</i> model	5
1.4	Basic cubic crystal structures	8
1.5	Miller indices's	9
1.6	Crustal structure of Si and GaAs	10
1.7	Atomic positions of the cubic diamond cell	11
1.8	Simplified semiconductor band diagram	12
1.9	Energy band structures of Si and GaAs	14
1.10	N-type semiconductor sample	16
1.11	Graph of resistivity vs carrier concentration	18
1.12	Energy band diagram, not in equilibrium	19
1.13	In thermal equilibrium	21
1.14	Forward and reverse bias	22
1.15	Current transport mechanisms	23
1.16	Diffusion and emission difference	25
1.17	Wave nature	34
1.18	Barrier shapes	35
1.19	Tunnelling in an FM/I/SC junction	38
2.1	Schematic of Shamrock in 2008	48
2.2	Chamber A target	49
2.3	Chamber A turntable	49
2.4	Chamber B	51
2.5	Chamber B components	52
2.6	Experimental setup for x-ray analysis.	54
2.7	X-ray relectivity example	55
2.8	Crystal plane orientations	56

2.9	UV lithography steps	60
2.10	The Millatron	62
2.11	Hidden end point detector	62
2.12	RT rig sample holder	64
2.13	Van der Pauw resistivity sample	66
2.14	Van der Pauw Hall effect sample	68
3.1	Schematic of DOS of different metals	72
3.2	Schematic of DOS of different half metal	74
3.3	Crystal structure of Fe_3O_4	75
3.4	XRD scans of Fe_3O_4 / GaAs	76
3.5	SQUID data for Fe_3O_4 / GaAs	78
3.6	$R - T$ of Fe_3O_4 on various substrates	79
3.7	Transport measurements on Fe_3O_4 / GaAs	80
3.8	$\ln(dI/dV)$ vs V of Fe_3O_4 / GaAs	81
3.9	AEP of Fe_3O_4 / mid p-type GaAs	83
3.10	Temperature dependence of R_S , F_0 , and I_S	85
3.11	XRD of Fe_3O_4 / Si	87
3.12	SQUID magnetization curves for Fe_3O_4 / Si	88
3.13	Temp dependence of magnetization of Fe_3O_4 / Si	89
3.14	$I - V$ of Fe_3O_4 / Si(111)	90
3.15	AEP of Fe_3O_4 / Si(111)	91
3.16	$I - V$ of Fe_3O_4 / Si(001)	93
3.17	AEP of Fe_3O_4 / Si(001)	94
3.18	TEM and HRTEM of Fe_3O_4 on Si(111)	95
3.19	HAADF of Fe_3O_4 on Si(111)	96
3.20	TEM and HRTEM of Fe_3O_4 on Si(001)	97
3.21	Moment as a function of thickness	98
4.1	Insulator and metal band diagram comparison	105
4.2	TMR improvement for MTJs	107
4.3	Images of $50 \times 50 \mu\text{m}$ and 100 nm sized junctions	110
4.4	Array and schematic of nano junctions	111
4.5	XRD of MgO on Si(001) and Si(111)	113
4.6	Rocking curve of MgO on Si(001)	114
4.7	Magnetization curve of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$	115
4.8	$I - V$ of Si / 0 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	117

4.9	$I - V$ of Si / 1 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	118
4.10	$I - V$ of Si / 2 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	119
4.11	$I - V$ of Si / 3 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	120
4.12	$I - V$ of Si / 0 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	121
4.13	$I - V$ of Si / 1 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	122
4.14	$I - V$ of Si / 2 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	123
4.15	$I - V$ of Si / 3 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	124
4.16	Low bias of $\ln(I)$ vs. V	125
4.17	$\ln(I)$ vs. V for all thicknesses of $\text{Co}_{90}\text{Fe}_{10}$ / AlO_x / Si	126
4.18	$\ln(I)$ vs. barrier thickness for $\text{Co}_{90}\text{Fe}_{10}$ / AlO_x / Si systems	129
4.19	$\ln(I)$ vs. barrier thickness for $\text{Co}_{90}\text{Fe}_{10}$ / MgO / Si systems	130
4.20	$I - V$ of Si / 0 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	132
4.21	$I - V$ of Si / 1 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	133
4.22	$I - V$ of Si / 2 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	134
4.23	$I - V$ of Si / 3 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	135
4.24	$I - V$ of Si / 0 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	136
4.25	$I - V$ of Si / 1 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	137
4.26	$I - V$ of Si / 2 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	138
4.27	$I - V$ of Si / 3 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	139
4.28	$\ln(I)$ vs. barrier thickness for $\text{Co}_{90}\text{Fe}_{10}$ / AlO_x / Si systems	141
4.29	$\ln(I)$ vs. barrier thickness for $\text{Co}_{90}\text{Fe}_{10}$ / MgO / Si systems	142
4.30	TEM and HRTEM of Fe / MgO / Si	144
4.31	XRD graph of $\text{Co}_{90}\text{Fe}_{10}$ / 3 nm MgO / GaAs	146
4.32	$I - V$ of GaAs / 0 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	148
4.33	$I - V$ of GaAs / 1 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	149
4.34	$I - V$ of GaAs / 2 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	150
4.35	$I - V$ of GaAs / 3 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	151
4.36	$I - V$ of GaAs / 0 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	152
4.37	$I - V$ of GaAs / 1 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	153
4.38	$I - V$ of GaAs / 2 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	154
4.39	$I - V$ of GaAs / 3 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the micro sized junction	155
4.40	$\ln(I)$ vs. barrier thickness for $\text{Co}_{90}\text{Fe}_{10}$ / AlO_x / GaAs systems	158
4.41	$\ln(I)$ vs. barrier thickness for $\text{Co}_{90}\text{Fe}_{10}$ / MgO / GaAs systems	159
4.42	$I - V$ of GaAs / 0 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	161
4.43	$I - V$ of GaAs / 1 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	162
4.44	$I - V$ of GaAs / 2 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	163

4.45	$I - V$ of GaAs / 3 nm AlO_x / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	164
4.46	$I - V$ of GaAs / 0 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	165
4.47	$I - V$ of GaAs / 1 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	166
4.48	$I - V$ of GaAs / 2 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	167
4.49	$I - V$ of GaAs / 3 nm MgO / $\text{Co}_{90}\text{Fe}_{10}$ for the nano size junction	168
4.50	$\ln(I)$ vs. barrier thickness for $\text{Co}_{90}\text{Fe}_{10}$ / AlO_x / GaAs systems	170
4.51	$\ln(I)$ vs. barrier thickness for $\text{Co}_{90}\text{Fe}_{10}$ / MgO / GaAs systems	171
4.52	$\ln(\sigma)$ vs. $1000/T$ of mid n-type GaAs	173
4.53	$\ln(\sigma)$ vs. $1000/T$ of the mid n-type Si(001)	174
4.54	Contact resistance	175
4.55	RA product vs. thickness for MgO	176
4.56	RA product vs. thickness for AlO_x	177
4.57	l_c versus carrier concentration	183
A.1	Schematic of depletion region	197
B.1	Front panel of $I - V$ program	202
B.2	Block diagram of $I - V$ program	204
B.3	Front panel of ϕ_B and n program	205
B.4	Back panel of ϕ_B and n program	206
B.5	Front panel of AEP program	207
B.6	Block diagram of AEP program	209
B.7	Front panel of the van der Pauw resistivity program	211
B.6	Block diagram of van der Pauw resistivity program	214
B.7	Front panel of Hall voltage program	215
B.8	Block diagram of Hall voltage program	216

List of Tables

1.1	Table of bandgap constants	13
1.2	Workfunctions and barrier heights	20
2.1	Deposition parameters for Chamber A	50
2.2	Deposition parameters for Chamber B	53
3.1	Summary of carrier concentrations and barrier heights	99
4.1	Table of barrier heights for μm Si Schottky junctions	128
4.2	Table of barrier heights for μm GaAs Schottky junctions	160
4.3	Table of barrier heights for nano scale GaAs Schottky junctions	172
4.4	Table of all barrier heights for all junction sizes	179
5.1	Summary of carrier concentrations and ϕ_B from Chapter 3	189
5.2	Table of all barrier heights for all junction sizes from Chapter 4	191

Chapter 1

Introduction

1.1 Spintronics

Conventional electronics is based on electrical charge carriers, electrons, and the manipulation of electron currents, but it has ignored the electron spin despite being aware of it throughout most of the twentieth century [1]. Spin is a basic and intrinsic property of the electron. The electron behaves as if it were spinning on its own axis thereby creating a magnetic moment, which is the basis of solid-state magnetism. The spin angular momentum, s , can only take one of two values when projected along a given axis, $m_s\hbar$, where m_s is the spin magnetic quantum number and is equal to $\pm\frac{1}{2}$. \hbar is Plank's constant divided by 2π . The magnetic moment m is $-\frac{e}{m_e}s$, where e is the electron charge and m_e is the electron mass. So the magnetic moment can be written as $\pm\frac{e\hbar}{m_e}$ indicating that there only two possible angular momentum states, known as spin up (\uparrow) and spin down (\downarrow).

A new branch of electronics based on the ability to exploit and manipulate the spin of an electron instead of, or along with, charge degrees of freedom could theoretically revolutionize the electronics industry and is of increasing interest to the industry as current silicon technology is beginning to approach fundamental limits. This research field has been named *spin electronics* or *spintronics*. Spintronics is a very broad field but

already at least one area, giant magnetoresistance, has well-established commercial applications. The discovery of giant magnetoresistance [2, 3] was a milestone which started a new research area combining traditional magnetism and electronics. In recognition of its importance the 2007 Nobel prize was awarded to Albert Fert and Peter Grünberg for their contribution to the development of spintronics [4].

1.1.1 History of Spintronics

An essential part in the development of spin based electronics is electrical spin injection and detection. This was first demonstrated about twenty years ago by driving a spin polarized current from a ferromagnetic electrode into a single crystal aluminium bar at temperatures below 77 K [5]. More recently, spin transport was achieved between magnetic and non-magnetic semiconductors with efficiencies of up to 90% [6, 7] but again at low temperatures, and between ferromagnetic and normal metals at room temperature [8]- [10]. However, efficient spin injection from a ferromagnetic metal (FM) into a semiconductor (SC), which is one of the main goals of spin electronics, has proved rather more difficult.

It was originally thought that the most straightforward approach to spin injection from a ferromagnetic metal into a semiconductor would be the formation of an ohmic contact between the two. However, in spite of a lot of effort from a number of groups, spin injection from ferromagnetic metal-semiconductor ohmic contacts has been extremely poor and any polarization effects can be explained by Hall voltages induced by stray magnetic fields from the contacts [11]. Schmidt *et. al.* investigated the reasons as to why ohmic contacts have repeatedly given such poor and unconvincing results and have shown that there is a fundamental obstacle to efficient spin injection between a ferromagnetic metal and a semiconductor [12]. Spin injection efficiency depends on the ratio of the conductivities of the spin polarized source and the semiconductor material that is to be injected. The tiny conductivity of the semiconductor compared to that of the metal results in very

poor spin injection efficiencies, and this is what is known as the conductivity mismatch problem, which was demonstrated using a system comprised of a two dimensional electron gas (2DEG) semiconductor sandwiched between two ferromagnets, shown in figure 1.1. The first interface is located at $x = 0$ and the second at $x = x_0$. The theory of Schmidt

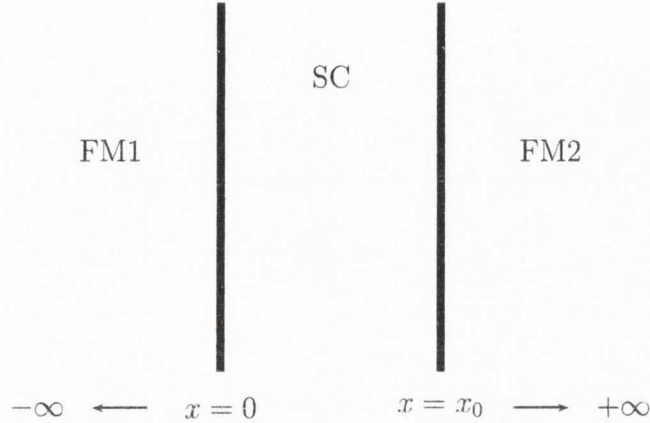


Figure 1.1: Schematic of the system used by Schmidt to develop and demonstrate the conductivity mismatch problem.

et. al. is based on the assumption that spin flip scattering occurs on a much slower time scale than other electron scattering, ($\tau_{sf} \gg \tau_e$) [13]. This assumption is used to define two electrochemical potentials, μ_{\uparrow} and μ_{\downarrow} , which are not necessarily equal [14]. The conductivity mismatch theory developed by Schmidt *et. al.* is shown best in figure 1.2, which was taken from their paper [12]. Part (a) is a simple model of the system as resistor network where the up and down spin resistances are,

$$R_{1\uparrow} + R_{SC\uparrow} + R_{3\uparrow} = R_{\uparrow}$$

$$R_{1\downarrow} + R_{SC\downarrow} + R_{3\downarrow} = R_{\downarrow}$$

where $R_{1\uparrow,\downarrow}$ is the resistance of the first ferromagnetic contact, $R_{SC\uparrow,\downarrow}$ is the resistance of the semiconductor and $R_{3\uparrow,\downarrow}$ is the resistance of the second ferromagnetic contact for the two independent spin channels. Part (b) and (c) of figure 1.2 shows the chemical potential for the parallel and anti-parallel magnetizations in the three different regions. Rashba *et.*

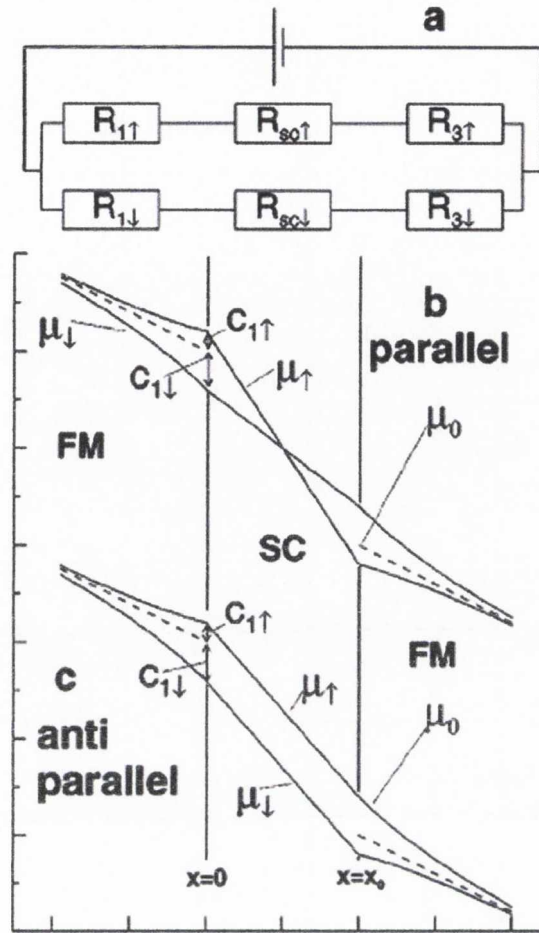


Figure 1.2: (a) A model of the system as a simple resistor network. The electrochemical potentials in the three different regions is shown for (b) the parallel and (c) the anti-parallel magnetization of the ferromagnetic. The solid lines show the potential for the up and down spin electrons and the dotted lines show, μ_0 , the potential without spin effects [12].

al. proposed that replacing the direct metal / semiconductor contact with an interfacial resistance, i.e. an interfacial barrier, would provide a solution to this mismatch problem. They specifically investigated using a tunnel barrier (TB) since it controls the boundary conditions and would change the physics of the problem, supporting considerable differences in electrochemical potentials under the conditions of slow spin relaxation that allow efficient spin injection [15]. This FM / TB / SC system is shown schematically in figure 1.3. Rashba *et. al.* have also examined using a magnetic tunnel transistor emitter for spin

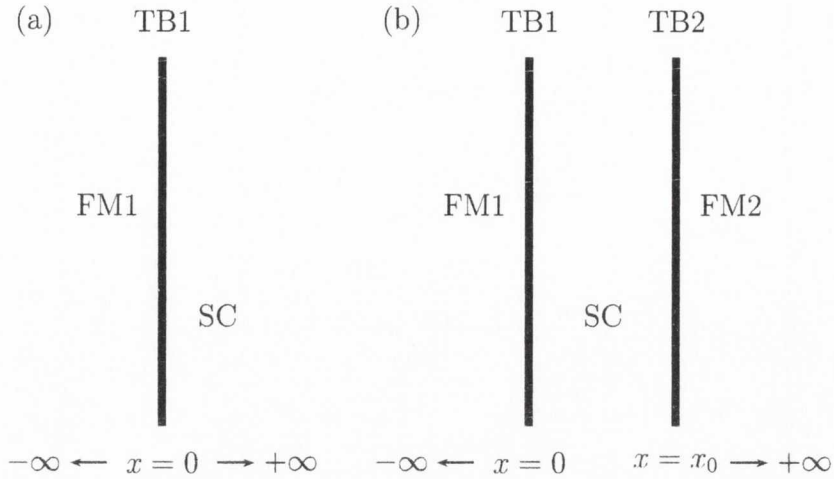


Figure 1.3: Schematic of the system used in Rashba's theory where (a) is a single interface and (b) is the sandwich structure of Schmidt's system, figure 1.1.

injection [16] and quite recently the use of these type of structures has led to high spin injection efficiencies [17]- [19] as well as spin injection at room temperature [20].

Most of these experiments have been carried out using GaAs as the semiconductor. This is because a vital part of spin injection experiments is the detection of any injected current. GaAs is a direct band gap semiconductor and the presence of polarized carriers in a direct gap can be detected by measuring the circular polarization of light emitted from GaAs. Usual detection experiments use spin light emitting diodes (LEDs) where the polarization of the light emitted is due to injected spin polarized currents and can be used to measure the success and efficiency of spin injection.

Si has long been the main semiconductor of interest when it comes to spin injection. It is the most commercially successful semiconductor. Successful efficient spin injection and manipulation could revolutionise the electronics industry. It has long spin relaxation and decoherence times that make it an ideal candidate for successful spin transport. Silicon's indirect band gap, weak spin-orbit coupling and small paramagnetic impurities are what gives it such long spin relaxation and decoherence times. Unfortunately these properties are also what make traditional methods of optical detection impossible in Si-

based structures [21]. The lack of any similar “easy” method of detection such as that which exists for GaAs structures has hindered the progress of Si spin injection experiments. Recently, however two independent groups have successfully demonstrated spin injection and detection through two different methods. The first used a spin valve structure to inject hot electrons into Si [22] & [23]. The energy of the electrons was determined by the Schottky barrier and 1 nA of spin polarized current was generated using an input current of 1 mA. The second experiment [24] & [25] injected spin polarized electrons near the conduction band edge through an Al_2O_3 tunnel barrier so the electron energy in this case is determined by the bias applied across the tunnel barrier. These structures were grown by molecular beam epitaxy (MBE) on GaAs quantum well structures and so the spin polarization was detected using the usual optical means. These first detection experiments seemed to open the door to spin experiments in Si and were soon followed by a non-local geometry spin detection experiment [26]. Most recently Jonker *et. al.* have shown that it is not only possible to inject and detect spin polarized currents using this non-local setup but also that these currents can be extracted and manipulated [27] bringing the future of silicon based spintronic devices ever closer.

The purpose of this thesis has been to investigate transport through ferromagnetic metal / semiconductor junctions in order to see if a barrier is formed, which could potentially enable efficient spin injection from the metal into the semiconductor. The semiconductor materials that were studied are GaAs and Si because these are the most widely used semiconductor materials and therefore generate the most interest.

The first system studied was Fe_3O_4 on Si and GaAs. Fe_3O_4 was picked because it is a half metallic ferromagnet. Half metals have a completely spin polarized conduction band, which should yield a considerable injection efficiency even for ohmic contacts [12]. In the case of tunnelling they should give a much larger spin accumulation in the semiconductor compared to $3d$ transition metal injectors. Fe_3O_4 is a well known example of a class II_B half metal in which conduction occurs via polaronic hopping in a minority spin band [28].

It has a high Curie temperature of 858 K and calculations indicate that Fe_3O_4 exhibits full negative spin at the Fermi level. Although experiments have not confirmed the complete half metallicity of Fe_3O_4 they do show that the number of minority electrons is larger than the number of majority electrons at the Fermi level [29]- [32]. An Fe_3O_4 film on a semiconductor substrate should provide a high negative spin accumulation in the substrate after the formation of a Schottky tunnelling barrier. Another advantage of using the half metal is that the resistivity of Fe_3O_4 increases with decreasing temperature and hence temperature could be used to reduce the conductivity mismatch between the film and the semiconductor substrate. Further details on half metals can be found in Chapter 3, which covers the details of the results of the Fe_3O_4 systems.

The second type of system studied included a thin tunnel barrier inserted between the ferromagnetic metal spin injection source and the semiconductor. These systems used $\text{Co}_{90}\text{Fe}_{10}$ as the spin injection source and were studied as a function of barrier material and thickness. Details of the results of these experiments can be found in Chapter 4.

1.2 Brief Introduction to Silicon and Gallium Arsenide

The semiconductor substrates Si and GaAs are used throughout this thesis. The properties of semiconductors is been well documented in a vast number of textbooks and papers. Semiconductor science is a field in itself but here is a brief introduction to some of the most important properties of semiconductors.

1.2.1 Crystal Structure

An ideal crystalline solid can be described by three primitive basis vectors, \mathbf{a} , \mathbf{b} and \mathbf{c} , so that it remains invariant under translation through any vector that is the sum of integral

multiples of these basis vectors. Basically direct lattice sites can be defined by,

$$\mathbf{R} = m\mathbf{a} + n\mathbf{b} + p\mathbf{c} \quad (1.1)$$

where m , n and p are integers [33]. The smallest volume that can serve as a building block for the crystal structure is $\mathbf{a} \times \mathbf{b} \times \mathbf{c}$. Figure 1.4 shows the conventional cubic cells. The three lattices in the cubic system are the simple cubic (sc), the body centered cubic (bcc) and face centered cubic (fcc). Of these only the sc is a primitive cell, with one lattice point per unit cell.

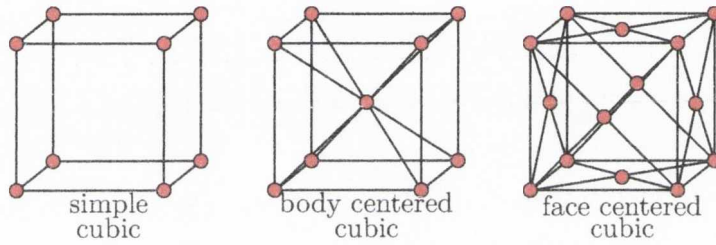


Figure 1.4: The cubic space lattices, cells shown are the conventional cells

For the given set of direct basis vectors a set of reciprocal lattice basis vectors \mathbf{a}^* , \mathbf{b}^* and \mathbf{c}^* can be defined by the basis vectors,

$$\begin{aligned} \mathbf{a}^* &\equiv 2\pi \frac{\mathbf{b} \times \mathbf{c}}{\mathbf{a} \cdot \mathbf{b} \times \mathbf{c}} \\ \mathbf{b}^* &\equiv 2\pi \frac{\mathbf{c} \times \mathbf{a}}{\mathbf{a} \cdot \mathbf{b} \times \mathbf{c}} \\ \mathbf{c}^* &\equiv 2\pi \frac{\mathbf{a} \times \mathbf{b}}{\mathbf{a} \cdot \mathbf{b} \times \mathbf{c}} \end{aligned} \quad (1.2)$$

so that $\mathbf{a} \cdot \mathbf{a}^* = 2\pi$, $\mathbf{a} \cdot \mathbf{b}^* = 0$ and so on by cyclical relationship. The general reciprocal lattice vector is given by,

$$\mathbf{G} = h\mathbf{a}^* + k\mathbf{b}^* + l\mathbf{c}^* \quad (1.3)$$

where h , k and l are integers. $\mathbf{G} \cdot \mathbf{R} = 2\pi \times \text{integer}$ and therefore each vector of a reciprocal

lattice is normal to a set of planes in the direct lattice. The volume of a unit cell of the reciprocal lattice, V_C^* , is inversely proportional to the volume of a unit cell of the direct lattice. $V_C^* = (2\pi)^3/V_C$, where $V_C \equiv \mathbf{a} \cdot \mathbf{b} \times \mathbf{c}$.

The most convenient and commonly used method of defining the various planes in a crystal is to find the intercepts of the plane with the three basic axes in terms of lattice constants and reduce them to the smallest three integers having the same ratio. These are called Miller indices's and, the result is enclosed in brackets, (hkl) , are the Miller indices's for a single plane or set of parallel planes. The most important are shown in figure 1.5.

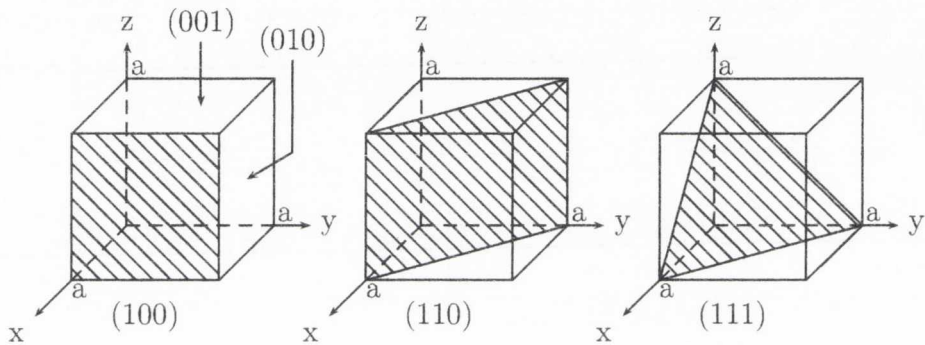


Figure 1.5: Miller indices's of some important planes in a cubic crystal

The diamond structure is the structure of semiconductors like silicon and germanium. This is shown in part (a) of figure 1.6. The space lattice of diamond is fcc with two identical atoms at the co-ordinates 000 and $\frac{1}{4}\frac{1}{4}\frac{1}{4}$ associated with each fcc lattice point. These form the primitive basis, a top down illustration is shown in figure 1.7. The conventional fcc lattice contains four lattice points and it follows that the conventional diamond structure contains $2 \times 4 = 8$ atoms. It has a tetrahedral bonding characteristic, each atom has four nearest neighbours and then 12 next nearest neighbours, shown in figure 1.6, part (a). It is a relatively empty structure, the maximum volume that can be filled with hard spheres being only 34 %. The diamond structure is an example of directional covalent

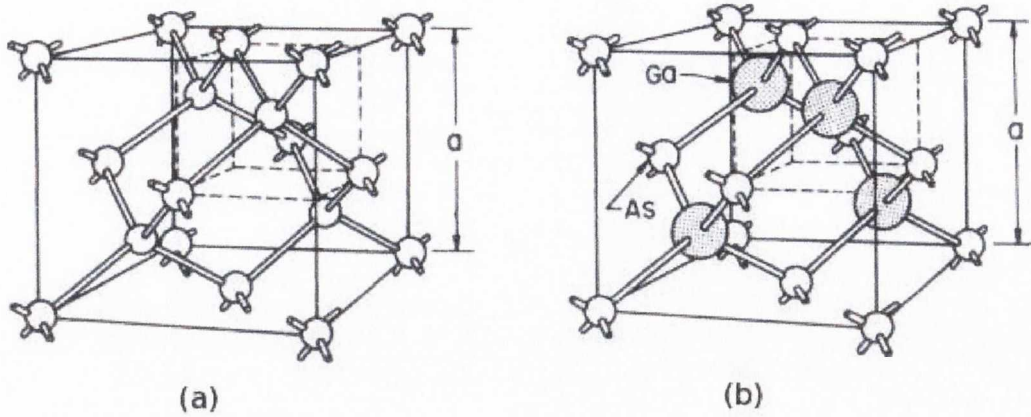


Figure 1.6: Schematic of the crystal structure of (a) diamond structure, typical of Si as well as Ge and C and (b) is the zincblende crystal structure, typical of GaAs

bonding that can be found in some of the crystallization structures of some of the column IV elements in the periodic table. The lattice constant a for Si diamond structure is 5.430 \AA , where a is the edge of the conventional cubic cell.

The diamond structure can also be viewed as two fcc structures displaced from each other by a quarter of the body diagonal. The zincblende structure results when, for example, Ga atoms are placed on one fcc lattice and As atoms are on the other, figure 1.6 part (b). The conventional cell is a cube with Ga co-ordinates of 000 ; $0\frac{1}{2}\frac{1}{2}$; $\frac{1}{2}0\frac{1}{2}$; $\frac{1}{2}\frac{1}{2}0$ and As co-ordinates of $\frac{1}{4}\frac{1}{4}\frac{1}{4}$; $\frac{1}{4}\frac{3}{4}\frac{3}{4}$; $\frac{3}{4}\frac{1}{4}\frac{3}{4}$; $\frac{3}{4}\frac{3}{4}\frac{1}{4}$. The overall lattice is fcc, there are four molecules of GaAs per conventional cell, around each atom are four equally distant atoms of the opposite kind arranged at the corners of the regular tetrahedron. The lattice constant a for GaAs is 5.650 \AA [33].

1.2.2 Band Gap

Every solid contains electrons but the important consideration governing electrical conductivity is how the solid's electrons respond to an applied electric field. Electrons in crystals are arranged in energy bands, which have an energy-momentum, $(E-k)$, relationship that is usually obtained by solving the Schrödinger equation of an approximate

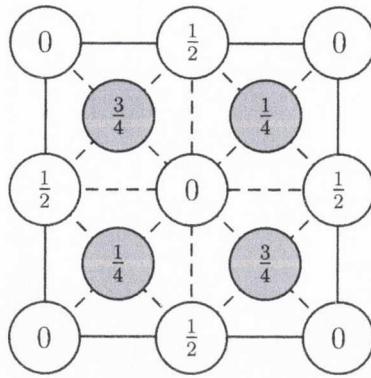


Figure 1.7: Atomic positions of the cubic diamond cell structure projected on a cube face. The fractions denote the height above the base in units of a cube edge. The points at 0 and $\frac{1}{2}$ are on the fcc lattice but the points at $\frac{1}{4}$ and $\frac{3}{4}$ are on a similar lattice, which is displaced along the body diagonal by a quarter of its length. The basis of the fcc space lattice consists of two identical atoms at 000 and $\frac{1}{4}\frac{1}{4}\frac{1}{4}$.

one electron problem. The Bloch theorem, which is one of the most important theorems in solid-state physics, states that if a potential energy $V(\mathbf{r})$ is periodic with the lattice periodicity then the solutions of the Schrödinger equation,

$$\left[-\frac{\hbar^2}{2m} \nabla^2 + V(\mathbf{r}) \right] \psi_{\mathbf{k}}(\mathbf{r}) = E_{\mathbf{k}} \psi_{\mathbf{k}}(\mathbf{r}) \quad (1.4)$$

are of the form,

$$\psi_{\mathbf{k}}(\mathbf{r}) = u_n(\mathbf{k}, \mathbf{r}) \exp(i\mathbf{k} \cdot \mathbf{r}) \quad (1.5)$$

and is called a Bloch function¹. $u_n(\mathbf{k}, \mathbf{r})$ is periodic in \mathbf{r} with the periodicity of the direct lattice and n is the band index. The Bloch theorem can show that the energy $E_{\mathbf{k}}$ is periodic in the reciprocal lattice, $E_{\mathbf{k}} = E_{\mathbf{k}+G}$, where G is a general reciprocal lattice vector given by equation 1.3. It is enough to use only \mathbf{k} s in the primitive cell to label the energy uniquely for a given band index. A Brillouin zone is defined as a Wigner-Seitz

¹Bloch's theorem is expressed as:

The eigenfunctions of the wave equation for a periodic potential are the product of a plane wave $\exp(i\mathbf{k} \cdot \mathbf{r})$ times a function $u_n(\mathbf{k}, \mathbf{r})$ with the periodicity of the crystal lattice.

primitive cell in the reciprocal lattice and gives a description of elementary excitations and electron energy band theory. Momentum \mathbf{k} in a reciprocal lattice can be reduced to a point in the Brillouin zone and energy states can be given a label in the reduced zone schemes.

A crystal behaves as an insulator if the allowed energy bands are either full or empty, as then no electrons will move in an applied electric field. It will only behave as a metal if a band is partly filled and as a semiconductor or semi-metal if one or two of the bands are only slightly full or slightly empty. Semiconductors have a forbidden energy region in which allowed energy states cannot exist, they can exist above or below this gap. The bands above this region are called conduction bands and the bands below this region are called valence bands. The separation between the energy of the lowest conduction band and highest valence band is one of the most important parameters in semiconductor physics and is called the bandgap, E_g . A very simplified representation of this is shown in figure 1.8. It should be noted that convention defines electron energy to be positive when

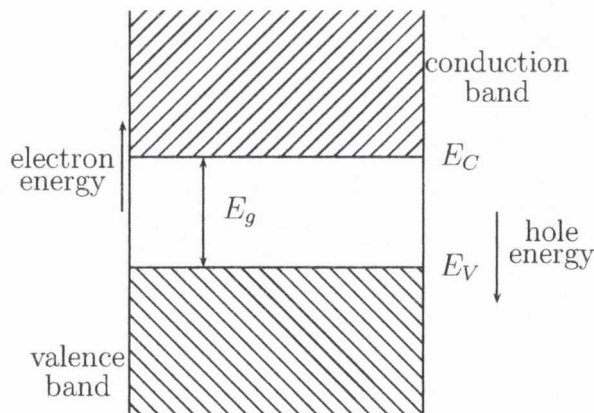


Figure 1.8: Simplified band diagram of a semiconductor

measured upwards and hole energy positive when measured downwards, figure 1.8.

The valence bands consist of a number of sub-bands and in the zincblende GaAs structure there are four sub-bands, as can be seen in part (b) of figure 1.9; the top of the valence band is at $E = 0$. Three of the four bands are degenerate at $k = 0$, Γ point and these form the top edge of the band. The conduction bands are also of a similar nature. At room temperature, under normal atmosphere and for very pure Si and GaAs the bandgap is 1.12 eV and 1.42 eV respectively. Results from literature show that the bandgaps for most semiconductors tend to decrease with increasing temperature. This variation in temperature can be expressed approximately as a universal function,

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \quad (1.6)$$

where $E_g(0)$, α and β are constants specific to the semiconductor material. These values are given for Si and GaAs in table 1.1, [35].

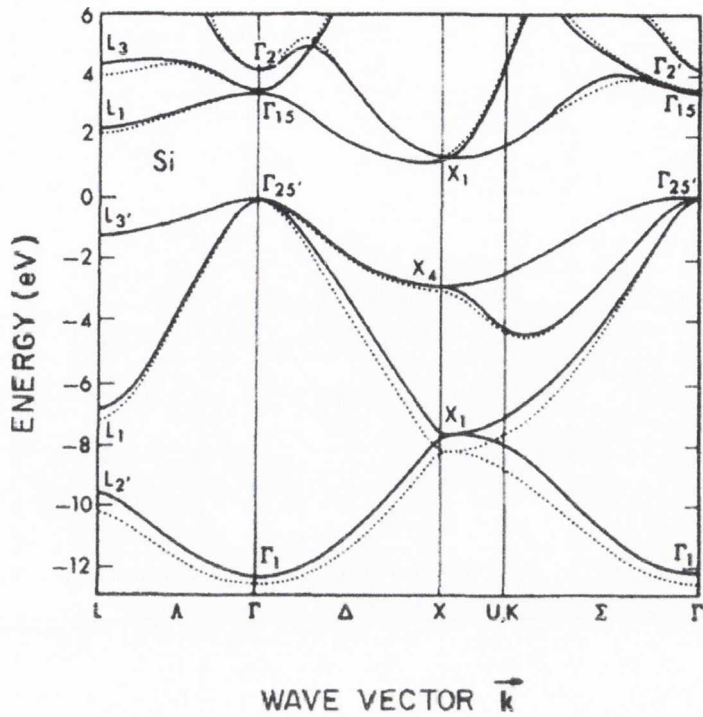
Material	$E_g(0)$	$\alpha \times 10^{-4}$	β
Si	1.170	4.73	636
GaAs	1.519	5.405	204

Table 1.1: Table of the constants $E_g(0)$, α and β for Si and GaAs

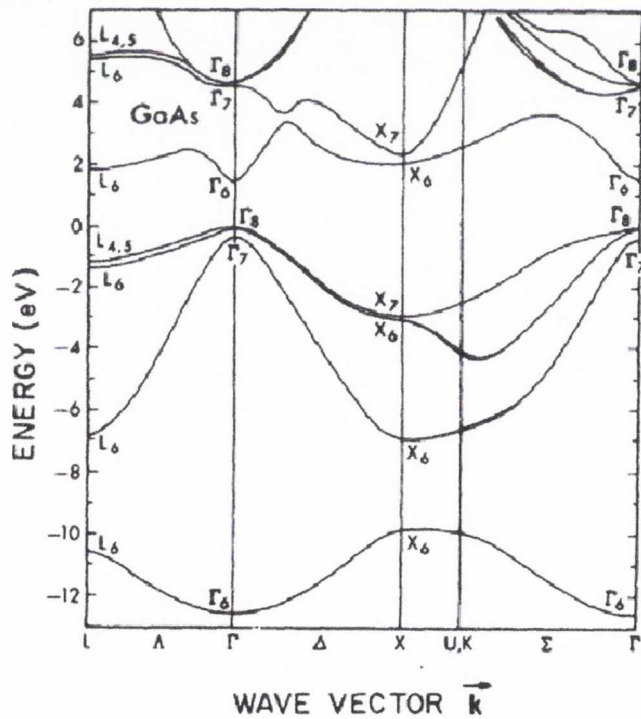
1.2.3 Resistivity, Mobility and Hall Effect

The resistivity, ρ , is defined as the constant of proportionality between the electric field, \mathcal{E} , and the current density, J ,

$$\mathcal{E} = \rho J \quad (1.7)$$



(a)



(b)

Figure 1.9: Energy band structures for (a) Si and (b) GaAs. For Si both local, dashed line, and non-local, solid line, results are shown. Results shown here are from literature and were obtained using the pseudo-potential calculation method [34].

It's inverse value is the conductivity, $\sigma = 1/\rho$ and

$$J = \sigma \mathcal{E} \quad (1.8)$$

For intrinsic semiconductors where both holes and electrons are carriers ρ is given by,

$$\rho = \frac{1}{\sigma} = \frac{1}{q(\mu_n n + \mu_p p)} \quad (1.9)$$

where n and p are the carrier concentrations of electrons and holes respectively and μ is the mobility. Mobility is the magnitude of the drift velocity of a charge carrier per unit electric field,

$$\mu = \frac{|v|}{\mathcal{E}} \quad (1.10)$$

and is positive for both electrons and holes. The drift velocity, v , of a charge q can be given in terms of the relaxation time, τ , which is the time between collisions as

$$v = \frac{q\tau\mathcal{E}}{m} \quad (1.11)$$

and so the mobility for n and p type electrons can be given as,

$$\begin{aligned} \mu_n &= \frac{q\tau_n}{m_n} \\ \mu_p &= \frac{q\tau_p}{m_p} \end{aligned} \quad (1.12)$$

where m is the mass. If $n \gg p$, as it is in n-type semiconductors [35],

$$\begin{aligned} \rho &\simeq \frac{1}{q\mu_n n} \\ \text{or} \\ \sigma &\simeq q\mu_n n \end{aligned} \quad (1.13)$$

The easiest way to measure the carrier concentration is to use the Hall Effect. An electron moving along a direction that is perpendicular to an applied magnetic field experiences a force acting normal to both directions. The electron moves in response to this force, which is basically the Lorentz force and the force from the internal electric field. Figure 1.10 shows a bar shaped n-type semiconductor, where obviously, the charge carriers are predominately electrons with a bulk density, n . Here the bulk density is considered to be the same as the carrier concentration. I is a constant current flowing along the x-

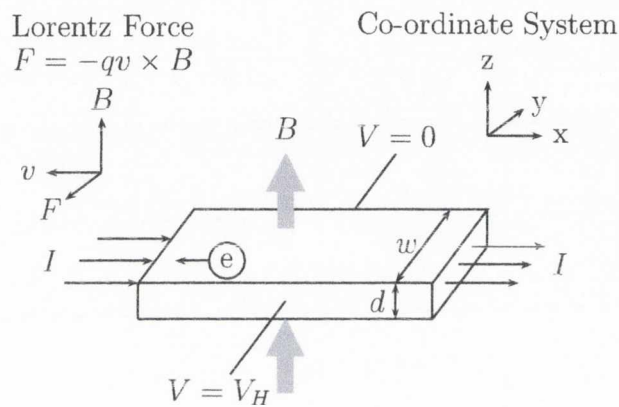


Figure 1.10: An n-type, bar shaped semiconductor.

direction in the presence of a z-direction magnetic field. Due to the Lorentz force mobile electrons initially drift away from the current line toward the negative y-axis, giving an excess surface electrical charge on one side of the sample. There is then a potential drop across the two sides of the sample, which is the Hall voltage, V_H [37]. The magnitude of the Hall voltage is,

$$V_H = \frac{IB}{qnd} \quad (1.14)$$

where d is the thickness of the sample. Thus by measuring the Hall voltage, V_H , in known values of B and I the carrier concentration (bulk density) can be calculated by re-arranging equation 1.14 as

$$n = \frac{IB}{qd|V_H|} \quad (1.15)$$

The van der Pauw technique is a convenient method used to determine both the mobility, μ , semiconductor type and the carrier concentration, n , through a combination of resistivity and Hall measurements. The experimental procedure in how to use this technique has been outlined in Chapter 2. Figure 1.11 shows a graph of resistivity versus carrier (impurity) concentration for Si, GaAs and Ge semiconductors, n and p-type for all cases [36].

1.3 Schottky Barriers

A metal-semiconductor (M-S) junction consists very simply of a metal in contact with a piece of semiconductor. This junction is of great importance as it is present in every semiconductor device. An M-S junction will behave as either an ohmic contact or a Schottky barrier, depending on the characteristics of the interface between the metal and semiconductor. An ideal ohmic contact exists where there is no potential step between the metal and semiconductor. This section will focus on the other type of contact that can be formed, the Schottky barrier. As previously mentioned the ohmic contact is a fundamental obstacle to efficient spin injection, whereas injection through a Schottky barrier provides a way around this.

The formation and nature of a barrier between a metal and semiconductor can most easily be explained through a series of energy band diagrams. First consider part (a) of figure 1.12. The metal and semiconductor are not yet in contact but they are aligned along the same vacuum level. As the metal and semiconductor are brought into contact

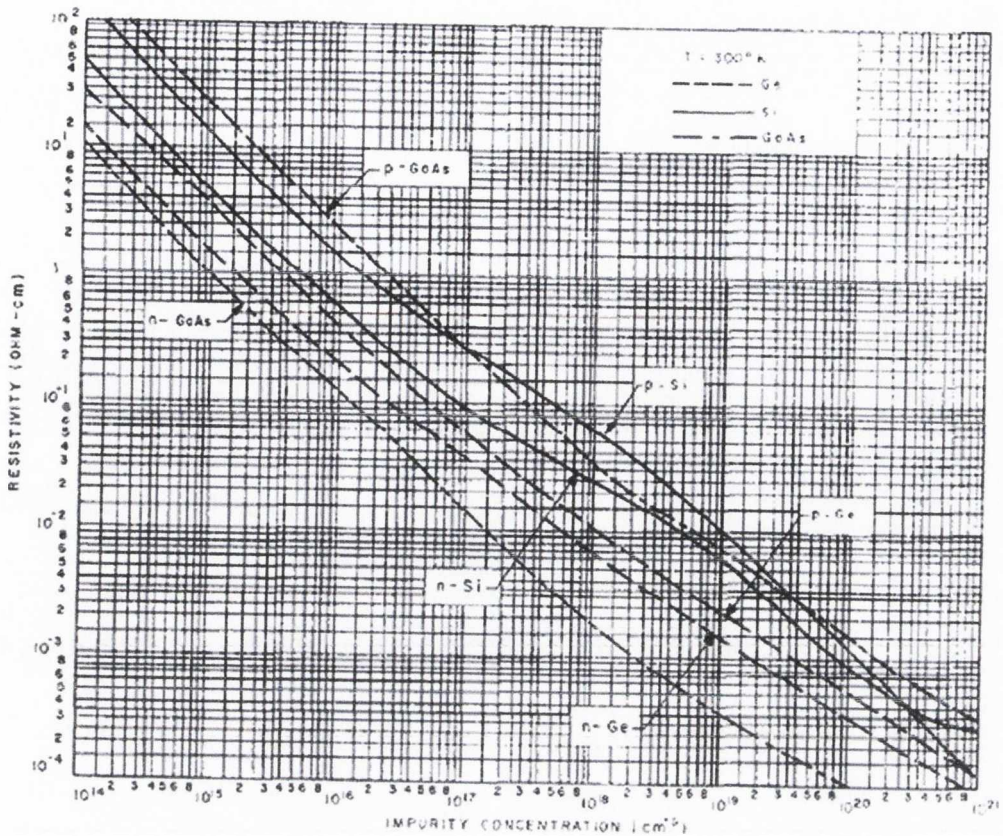


Figure 1.11: Resistivity vs impurity (carrier) concentration for n and p-type Si, GaAs and Ge semiconductors taken from [36].

the Fermi energies do not change right away because the metal and semiconductor are not yet in *equilibrium*. This is demonstrated by part (b) of figure 1.12.

The barrier height, ϕ_B in figure 1.12, is defined as the potential difference between the Fermi energy of the metal and the the band edge where the minority carriers reside. ϕ_M is the work function of the metal and χ is the electron affinity of the semiconductor. From figure 1.12, part (b), it can be seen that the barrier height of an n-type semiconductor can be obtained from,

$$\phi_B = \phi_M - \chi \quad (1.16)$$

For a p-type semiconductor it is given by the difference between the valence band and the

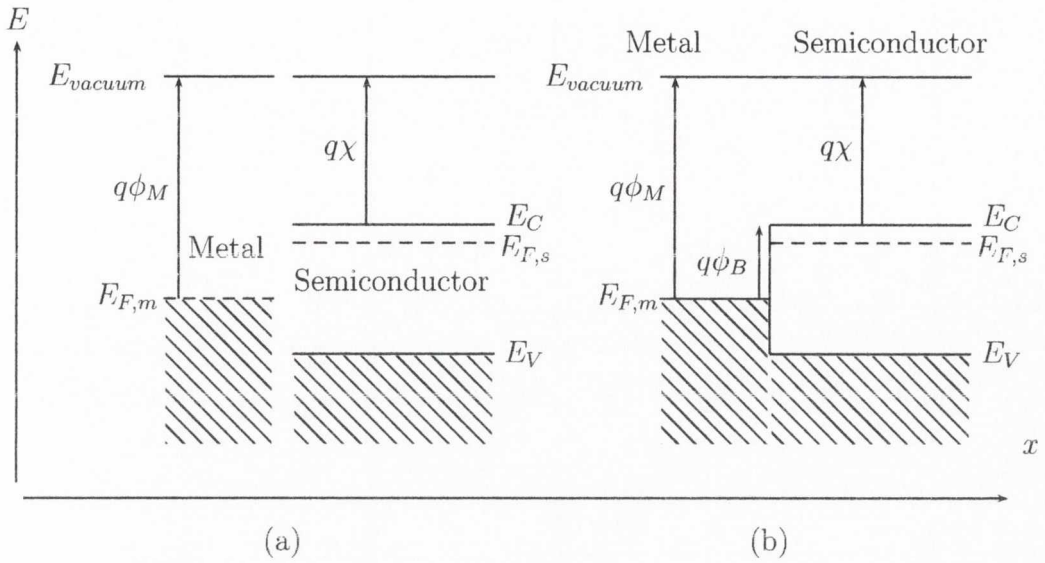


Figure 1.12: Energy band diagram of the metal and n-type semiconductor not in equilibrium (a) before and (b) just after they are brought into contact

Fermi energy in the metal,

$$\phi_B = \frac{E_g}{q} + \chi - \phi_M \tag{1.17}$$

where E_g is the bandgap of the semiconductor. Therefore, as demonstrated, a barrier will form at a M-S junction for holes and electrons if the Fermi level of the metal is somewhere between the conduction and valence band edges of the semiconductor. The difference between the Fermi energy levels of the metal and semiconductor is defined as the built-in potential, ϕ_I ,

$$\phi_I = \phi_M - \chi - \frac{E_C - E_{F_n}}{q} \quad \text{n-type} \tag{1.18}$$

$$\phi_I = \chi + \frac{E_C - E_{F_p}}{q} - \phi_M \quad \text{p-type} \tag{1.19}$$

Table 1.3 is a list of measured barrier heights reported in the literature. These are often different from the ones calculated using equations 1.16 and 1.17. This is due to the behaviour of the metal-semiconductor interface. The theory assumes both materials are perfectly pure, with no interaction between the two layers and no unwanted interfacial states formed between them. At least one, if not all of these assumptions are invalid in every case. The barrier height can also be altered by chemical reactions that can

	Ag	Al	Au	Cr	Ni	Pt	W
ϕ_M (in vacuum)	4.3	4.25	4.8	4.5	4.5	5.3	4.6
n-Si	0.78	0.72	0.8	0.61	0.61	0.9	0.67
p-Si	0.54	0.58	0.34	0.5	0.51		0.45
n-GaAs	0.88	0.8	0.9			0.84	0.8
p-GaAs	0.63		0.42				

Table 1.2: Workfunctions, ϕ_M , of selected metals and their measured barrier heights, ϕ_B , on p and n type silicon and gallium arsenide. All are in units of eV.

take place between the the metal and semiconductor and interface states at the surfaces of the semiconductor and interfacial layers. Despite this, some general trends can be observed using the theory. Equation 1.16 predicts the barrier height of metals on n-type semiconductors will increase with increasing workfunction. This has been verified on Si. GaAs however has a large density of surface states and so the barrier height can become virtually independent of the metal, as seen for n-type GaAs in table 1.3. Reported barrier heights may vary significantly due to different cleaning methods.

As mentioned earlier figure 1.12 is **not** in equilibrium since the Fermi energy levels in the metal and semiconductor are different from one another. Electrons in the n-type semiconductor can lower their energy by traversing the junction and as they leave the semiconductor, a positive charge due to the ionized donor atoms, stays behind. A negative field is then created, which lowers the band edges of the semiconductor. The

electrons flow into the metal until equilibrium between the electron diffusion into the metal and the electron drift caused by the field created by the ionized donor atoms is reached. Equilibrium is characterised by a constant Fermi energy level throughout the system, as shown in figure 1.13. It should be noted at this point that there is a region in the

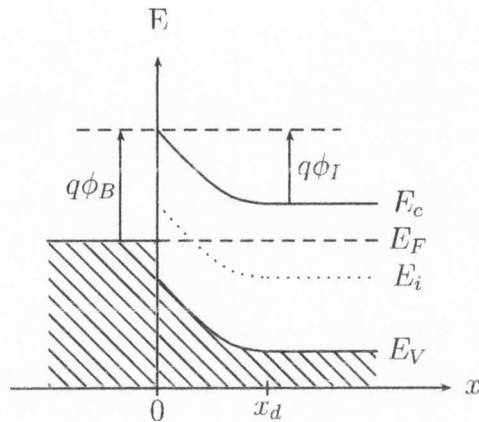


Figure 1.13: Energy band diagram of the metal and semiconductor in thermal equilibrium.

semiconductor when it's in thermal equilibrium, which is depleted of mobile carriers when no external voltage is applied. This is the depletion region and lies between $0 \leq x \leq x_d$ in figure 1.13. The potential across the semiconductor is equal to the built-in potential, ϕ_I , as defined earlier by equations 1.18 and 1.19.

1.3.1 Forward and reverse bias

The energy band diagram of the operation of a M-S junction under forward and reverse bias is shown in figure 1.14. When a positive bias is applied to the metal, the Fermi energy of the metal is lowered with respect to the Fermi energy in the semiconductor resulting in a smaller potential drop across the semiconductor. The diffusion-drift balance is disturbed and more electrons diffuse towards the metal than the number drifting into the semiconductor. There is now a positive current through the junction when the voltage is comparable to and greater than the built-in potential.

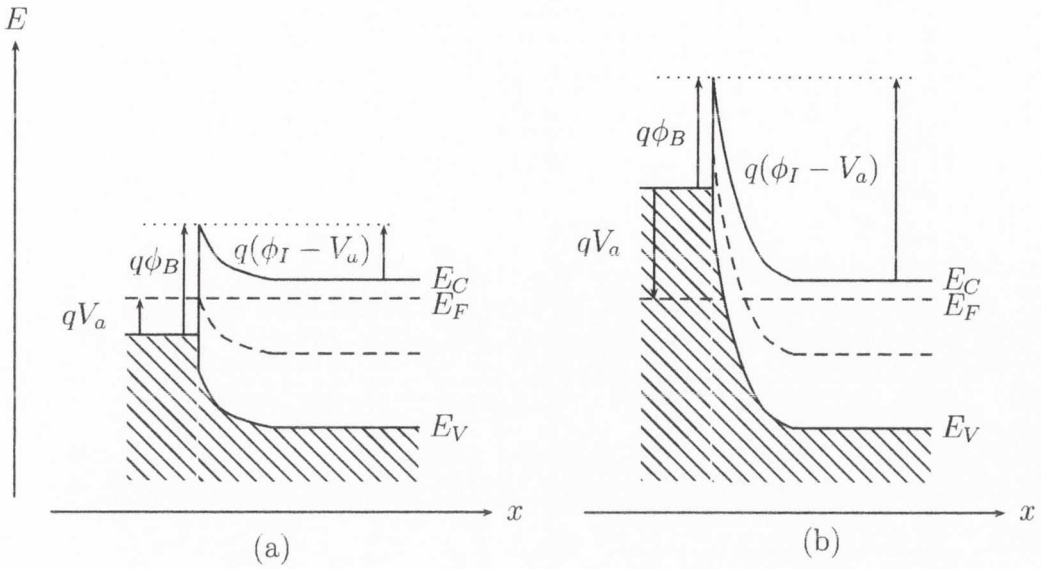


Figure 1.14: Energy band diagram of metal-semiconductor junction under (a) forward and (b) reverse bias

When a negative voltage is applied, part (b) figure 1.14, the Fermi level in the metal is raised with respect to the Fermi level in the semiconductor, which increases the potential across the semiconductor. This means a larger depletion region and a larger electric field at the interface. The barrier, which restricts the flow of electrons into the metal, is unchanged and so the barrier current is limited by the barrier regardless of the applied voltage. The potential of the semiconductor is the built-in potential, ϕ_I , minus the negative applied voltage V_a ,

$$\phi(x = \infty) - \phi(x = 0) = \phi_I - V_a \quad (1.20)$$

1.3.2 Current Transport Mechanisms

The various ways in which electrons can be transported across a metal-semiconductor junction are,

- emission of electrons from the semiconductor over the top of the barrier into the

metal, route a in figure 1.15

- quantum-mechanical tunneling through the barrier, b in figure 1.15
- recombination in the space-charge region, route c in figure 1.15
- recombination in the neutral region, route d in figure 1.15

It possible to fabricate practical Schottky barrier diodes in which the emission of the electrons is the most important method of transport. Such diodes are referred to as nearly ideal. This method of transport will be the main focus of this section. However it is important to note that contributions from the other methods of transport cause deviations from the ideal diode behaviour.

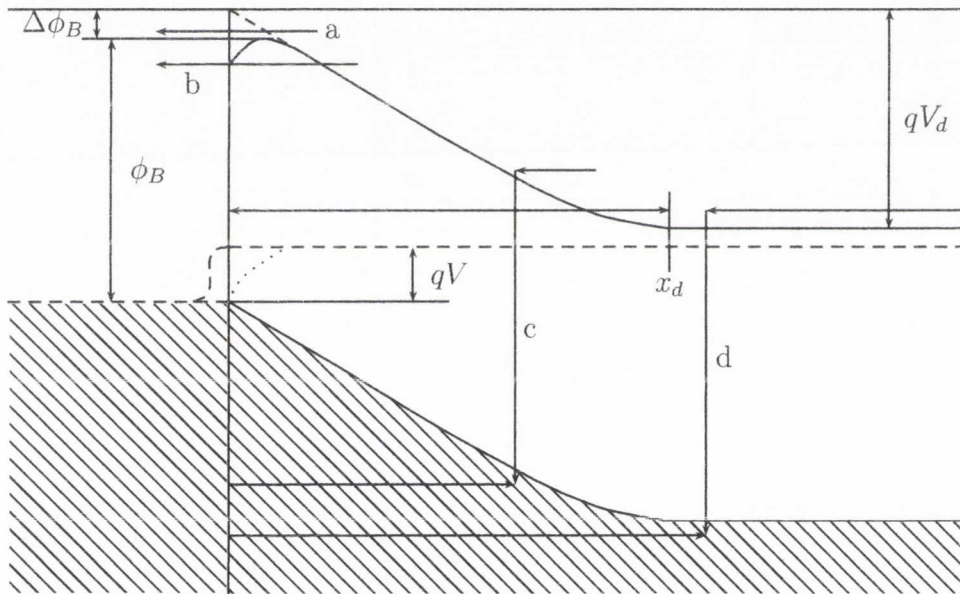


Figure 1.15: Energy band diagram illustrating the various current transport mechanisms.

Before being emitted over the barrier into the metal the electrons must first travel from the interior of the semiconductor to the interface. To do this they must pass through the depletion region of the semiconductor and in this region their motion is governed by drift and diffusion in the electric field of the semiconductor, which have been described

in in the beginning of this section on Schottky barriers. Arriving at the interface, their emission over the barrier is determined by the rate of transfer of electrons across the boundary between the metal and semiconductor. The two processes, drift and diffusion, are effectively in series and the current is determined by whichever of these processes causes the largest impediment to the flow of electrons. There are different theories to described the the two different processes, depending on whether the diffusion current is considered the limiting factor (Wagner 1931 and Schottky and Spenke 1939) or thermionic emission (Bethe 1942) is considered the limiting factor.

The diffusion theory states that the concentration of conduction electrons in the semiconductor immediately adjacent to the interface is not altered by the applied bias. This is the same as assuming that at the interface the quasi-Fermi² level in the semiconductor coincides that with the Fermi level in the metal. In this case the quasi Fermi level drops down through the depletion region in order to align with metal Fermi level.

The emission theory states that electrons emitted from the semiconductor into the metal are not in thermal equilibrium with the conduction electrons in the metal. Instead their energy exceeds the Fermi energy in the metal by the barrier height. They can loosely be described as “hot” electrons and in the metal can be though of as different from the ordinary metal conduction electrons. They can be described by their own quasi-Fermi level. As they travel through the metal they lose energy via collisions with conduction electrons and the lattice, eventually coming into equilibrium with the metal conduction electrons signified by the coincidence of the hot electron quasi-Fermi level with the metal Fermi level.

²The quasi-Fermi level, ζ , is a hypothetical energy level which has been introduced to describe the behaviour of electrons under non-equilibrium conditions. It predicts the concentration of the electrons in the conductance band as long as the electrons are in thermal equilibrium at the lattice temperature, and that the quasi-Fermi level is used in the Fermi-Dirac distribution function in place of the equilibrium Fermi level. ζ is shown as predicted by the diffusion theory and the emission theory in figure 1.16. It can also give the electron current in x direction by $qn\mu(d\zeta/dx)$ where n is the concentration of the electrons and μ their mobility.

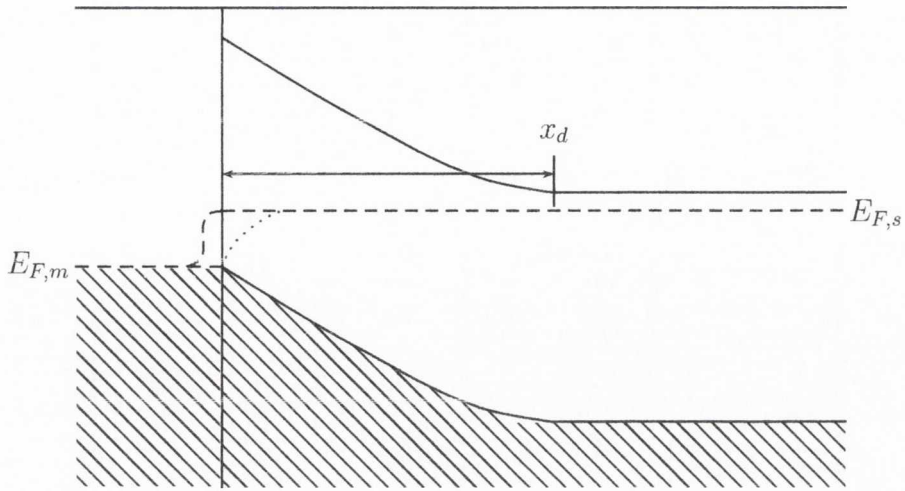


Figure 1.16: Illustration of the major difference between the diffusion theory and the emission theory. The electron quasi-Fermi level is represented by the dotted line according to the diffusion theory and the dashed line according to the emission theory.

The difference between the theories has been explained by looking at the different behaviour of the quasi-Fermi level in the theories. These differences are nicely illustrated in figure 1.16. Each theory assumes they are the important transport mechanism and the other can be neglected. Of course in reality the true behaviour lies somewhere between the two extremes of the diffusion theory and the thermionic emission theory. The derivation of the current-voltage characteristics will be outlined for each model in the following sections.

The diffusion theory

The current density in the depletion region can be given as,

$$J = qn\mu\mathcal{E} + qD_n\frac{dn}{dx} \quad (1.21)$$

where n is the carrier concentration in an n-type semiconductor, μ their mobility, D_n their diffusion constant, \mathcal{E} is the electric field in the barrier and $-q$ the charge on the electron. The mobility and diffusion constant must be independent of the electric field

for equation 1.21 to be valid, which is not true near the top of the barrier where \mathcal{E} has a maximum value. Also if the electron distribution function changes within the mean free path, which it does near the top of the barrier, it is not even valid to split the current into independent drift and diffusion components. However such a simplification is necessary for a manageable analysis and so equation 1.21 will be assumed true. The accuracy of any analysis always depends on the truth of the assumptions used and this must be borne in mind at all times.

The quasi-Fermi level, ζ_n , for the electrons is defined as,

$$n = \mathcal{N}_C \exp \left[\frac{-q(E_C - \zeta_n)}{kT} \right] \quad (1.22)$$

using the Boltzmann approximation to the Fermi-Dirac function. \mathcal{N}_C is the effective density of states in the conduction band and E_C is the energy at the bottom of the conduction band. Einstein's diffusion equation, $\mu/D_n = q/kT$, is used to rewrite equation 1.21 in the form

$$J = q\mu n \frac{d\zeta_n}{dx} \quad (1.23)$$

which shows that the gradient of ζ_n is the "driving force" for the electrons. Combining equations 1.22 and 1.23 gives,

$$\begin{aligned} J &= q\mu\mathcal{N}_C \exp \left[-\frac{q(E_C - \zeta_n)}{kT} \right] \frac{d\zeta_n}{dx} \\ &= kT\mu\mathcal{N}_C \exp \left[-\frac{qE_C}{kT} \right] \frac{d}{dx} \left(\exp \left[\frac{q\zeta_n}{kT} \right] \right) \end{aligned} \quad (1.24)$$

Integrating equation 1.24 between $x = 0$ and $x = x_d$ gives,

$$\begin{aligned} \frac{J}{kT\mu\mathcal{N}_C} \int_0^{x_d} \exp \left[\frac{qE_C}{kT} \right] dx &= \left[\exp \left(\frac{q\zeta_n}{kT} \right) \right]_0^{x_d} \\ &= \exp \left[\frac{q\zeta_n(x_d)}{kT} \right] - \exp \left[\frac{q\zeta_n(0)}{kT} \right] \end{aligned} \quad (1.25)$$

The current-voltage relationship can now be determined if E_C is known as a function of x and the values of $\zeta_n(0)$ and $\zeta_n(x_d)$ are specified for a particular applied bias value. Taking the Fermi level in the metal as the zero energy level gives $\zeta_n(x_d) = V_a$ since the applied voltage is equal to the difference between the Fermi levels at the terminals of the diode in eV. The depletion approximation³,

$$E_C = q\phi_B + \frac{qN_d}{2\epsilon_s} (x^2 - 2x_d x) \quad (1.26)$$

where N_d is a constant donor density, ϕ_B is the barrier height and $\epsilon_s (= \epsilon_{sr}\epsilon_0)$ is the permittivity of the semiconductor, is used to integrate the left hand side of equation 1.25.

Now the integral is written as,

$$\begin{aligned} \int_0^{x_d} \exp\left[\frac{E_C}{kT}\right] dx &= a^{-1} \exp\left[\frac{q\phi_B}{kT}\right] \exp(-a^2 x_d^2) \int_0^{aw} \exp(y^2) dy \\ &= a^{-1} \exp\left[\frac{q\phi_B}{kT}\right] F(ax_d) \end{aligned} \quad (1.27)$$

where $a = \left(\frac{q^2 N_d}{2\epsilon_s kT}\right)^{\frac{1}{2}}$ and $F(ax_d)$ is known as Dawson's integral. If $ax_d > 2$ then $F(ax_d)$ is approximately equal to $(2ax_d)^{-1}$. $ax_d > 2$ is equivalent to $qV_d > 4kT$, where V_d is the diffusion potential, and is generally satisfied except for very large values of forward bias.

Using this approximation, equation 1.25 can finally be written as

$$\begin{aligned} J &= 2kT\mu\mathcal{N}_C a^2 x_d \frac{\exp\left(\frac{qV}{kT}\right) - 1}{\exp\left(\frac{q\phi_B}{kT}\right)} \\ &= q\mathcal{N}_C \mu \mathcal{E}_{max} \exp\left[-\frac{q\phi_B}{kT}\right] \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \end{aligned} \quad (1.28)$$

The maximum field strength is given by Gauss's theorem⁴ as $\mathcal{E}_{max} = \frac{qN_d x_d}{\epsilon_s} = \frac{2kT a^2 x_d}{q}$.

This final equation, equation 1.28, gives the current-voltage dependence as predicted by the diffusion theory. It is almost in the form of the ideal diode expression, $J =$

³Please see Appendix A for more information on the depletion region approximation.

⁴again see Appendix A

$J_0 \left(\exp \left(\frac{qV}{kT} \right) - 1 \right)$. The deviation from ideal arises because \mathcal{E}_{max} is not independent of applied bias, it is actually proportional to $(V_{d0} - V_a)^{\frac{1}{2}}$. In reverse bias the current does not saturate but increases roughly as $|V_a|^{\frac{1}{2}}$.

The thermionic emission theory

The assumption in this theory is that the current is limited here by the actual transfer of electrons across the semiconductor-metal interface and that the drift and diffusion effects in the depletion region are negligible. This is the same as assuming the electrons have an infinite mobility and that $d\zeta_n/dx$, equation 1.23, is small enough to be neglected. As previously mentioned, the quasi-Fermi level for electrons remains flat through the depletion layer, figure 1.16, and coincides with the Fermi level in the bulk semiconductor, similar to a p - n junction. When a bias voltage V is applied, the concentration of electrons on the semiconductor side of the interface is increased by a factor of $\exp \left(\frac{qV}{kT} \right)$.

Imagine the existence of a thin insulating layer at the interface between the metal and semiconductor. Electrons coming from the semiconductor can tunnel through this layer with a probability p . If $p \ll 1$ most of the electrons will be reflected back into the semiconductor and remain in thermal equilibrium with the bulk electrons. The electron concentration on the semiconductor side of the boundary can be now given by,

$$n = \mathcal{N}_C \exp \left[-\frac{q(\phi_B - V)}{kT} \right] \quad (1.29)$$

Electrons in a semiconductor with spherical constant energy surfaces will have an isotropic Maxwellian distribution of velocities and, from kinetic theory, the number incident on a unit area per second is $\frac{n\bar{v}}{4}$, where \bar{v} is the average thermal velocity of the electrons in the semiconductor. The current density of electrons going into the metal is⁵

$$J_{sm} = \frac{pq\mathcal{N}_C\bar{v}}{4} \exp \left[-\frac{q(\phi_B - V)}{kT} \right] \quad (1.30)$$

⁵sm - semiconductor to metal, ms - metal to semiconductor.

p being the fraction of electrons that can tunnel into the metal. There is also a flow of electrons from the metal into the semiconductor, J_{ms} , which, assuming no bias dependence of ϕ_B , is unaffected by the applied bias as the barrier ϕ_B does not change from the metal side. At zero bias the semiconductor and metal currents are balanced so that J_{ms} is

$$J_{ms} = \frac{pq\mathcal{N}_C\bar{v}}{4} \exp\left(-\frac{q\phi_B}{kT}\right) \quad (1.31)$$

So now,

$$\begin{aligned} J &= J_{sm} - J_{ms} \\ &= \frac{pq\mathcal{N}_C\bar{v}}{4} \exp\left(-\frac{q\phi_B}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \end{aligned} \quad (1.32)$$

where this time \bar{v} is a Maxwellian distribution of velocities equal to $\frac{8kT}{\pi m^*}^{\frac{1}{2}}$ and m^* is the effective mass of the electrons in the semiconductor.

Another major assumption is now needed and that is that the imaginary insulating layer becomes so thin that p approaches unity. This means the number of electrons incident on the interface is unchanged and the current can be simply calculated by putting $p = 1$. $p = 1$ means no electrons are reflected back into the semiconductor and the velocity distribution at the top of the barrier is unidirectional, which, at first seems quite a drastic assumption and this assumption casts doubt over whole the concept of a quasi-Fermi level. However in 1976 Baccarani and Mazzone used the Monte Carlo method to calculate the trajectories of electrons crossing the barrier. They assumed the electrons to have isotropic Maxwellian velocity distribution at the edge of the depletion region and found that the electron velocity distribution at the top of the barrier is actually quite close to a unidirectional distribution, called a ‘‘hemi-Maxwellian’’ distribution. The concentration of these electrons is almost exactly half the concentration predicted by equation 1.29. The distribution’s mean velocity in the direction normal to the interface is $\frac{\bar{v}}{2}$ so the current density due to the electrons flowing from the semiconductor is very

close to what equation 1.30 predicted with $p = 1$. This was later confirmed again by Berz in 1985. So it seems that it is relatively acceptable to carry on with the assumption that $p = 1$ without needing to change the flux of electrons incident on the interface.

Substituting $p = 1$ and $\mathcal{N}_C = 2 \left(\frac{2\pi m^* kT}{h^2} \right)^{\frac{3}{2}}$ in equation 1.32 gives the current-voltage relationship according to the thermionic emission theory as,

$$J = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \quad (1.33)$$

where,

$$A^* = \frac{4\pi m^* q k^2}{h^3} \quad (1.34)$$

and this is of the form of the ideal diode characteristic, $J = J_0 \left[\exp\left(\frac{qV}{kT}\right) - 1 \right]$ where $J_0 = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right)$, assuming the barrier height is independent of applied bias.

This assumption is not true for a number of reasons and so further refinement and analysis is necessary. Even in a perfect junction with no interfacial layer the barrier height can be lowered due to the image-force by an amount $\Delta\phi_{BI}$, which depends on the applied bias. Now the effective barrier, ϕ_E , that the electrons must overcome can be written as,

$$\phi_E = \phi_B - \Delta\phi_{BI} \quad (1.35)$$

The bias dependence of ϕ_B when there is an interfacial layer between the semiconductor and metal gives further bias dependence to ϕ_E and such a dependence will modify the current-voltage relationship.

Supposing $\frac{\partial\phi_E}{\partial V}$ is constant so that it is possible to write,

$$\phi_E = \phi_{B0} - (\Delta\phi_{BI})_0 + \beta V \quad (1.36)$$

where ϕ_{B0} and $(\Delta\phi_{BI})_0$ refer to zero bias and the coefficient β is always positive as ϕ_E is always increasing with increasing forward bias. The current density is now,

$$\begin{aligned} J &= A^*T^2 \exp \left[-q \left(\frac{\phi_{B0} - (\Delta\phi_{BI})_0 + \beta V}{kT} \right) \right] \left[\exp \left(\frac{qV}{kT} \right) - 1 \right] \\ &= J_0 \exp \left(-\frac{\beta qV}{kT} \right) \left[\exp \left(\frac{qV}{kT} \right) - 1 \right] \end{aligned} \quad (1.37)$$

where

$$J_0 = A^*T^2 \exp \left[-q \left(\frac{\phi_{B0} - (\phi_{BI})_0}{kT} \right) \right]$$

now equation 1.37 is written as

$$J = J_0 \exp \left(\frac{qV}{nkT} \right) \left[1 - \exp \left(-\frac{qV}{kT} \right) \right] \quad (1.38)$$

where

$$\frac{1}{n} = 1 - \beta = 1 - \left(\frac{\partial \phi_E}{\partial V} \right) \quad (1.39)$$

where n is the ideality factor and **not** the carrier concentration. If $\frac{\partial \phi_E}{\partial V}$ is constant then n is also constant. For values of V greater than $3kT/q$ equation 1.38 is

$$J \approx J_0 \exp \left(\frac{qV}{nkT} \right) \quad (1.40)$$

Other methods of analysis also give the current-voltage relationship in the same form as equation 1.38.

It is often written in literature as

$$J = J_0 \left[\exp \left(\frac{qV}{nkT} \right) - 1 \right] \quad (1.41)$$

However this form is not strictly correct because the barrier lowering due to the image

force affects the flow of electrons from the metal to the semiconductor as well as the other way round. For $V > 3kT/q$ the difference between the two forms is negligible but the advantage to equation 1.38 is that n can be found experimentally by plotting a graph of $\ln \left[\frac{J}{1 - \exp(-qV/kT)} \right]$ against V , even for $V < 3kT/q$. The graph should be linear and the slope is equal to q/nkT if n is constant. Usually though $\frac{\partial \phi_E}{\partial V}$ is not constant and so the slope of $\ln \left[\frac{J}{1 - \exp(-qV/kT)} \right]$ against V is not linear. n then becomes a function of V and can still be found but only for a particular operating point in the current-voltage relationship.

Refinement of the thermionic-emission theory, A^* becomes A^{**}

A^* was introduced in equation 1.33 by assuming that all electrons incident on the interface cross into the metal and do not return. However according to quantum mechanics an electron can be reflected by a potential barrier *even if* it has the energy to cross the barrier. In fact even after it has crossed the barrier the electron may be scattered through a large enough angle with the absorption or emission of a phonon to return to where it came from. The most likely place for this type of scattering to take place is between the metal and within the semiconductor, here the conduction band slopes very steeply giving most electrons along this path enough energy to emit an optical phonon. This is the most likely form of scattering to take place where electrons have energies just above the energy threshold needed to emit a phonon.

Crowell and Sze calculated the probability, f_p , of an electron reaching the metal without being scattered back into the semiconductor and gave it as a function of the maximum electric field \mathcal{E}_{max} in the depletion region. As the position of the potential maximum gets nearer to the metal, \mathcal{E}_{max} increases and f_p approaches unity meaning that the distance within which phonon scattering can occur is reduced.

They also investigated the effect of quantum mechanical tunnelling. Included in their work was the additional effect of electrons tunnelling through the top of the barrier. The

combination of these two effects gives a factor, f_q , which depends on temperature⁶ and the maximum electric field as it is \mathcal{E}_{max} that determines the height and shape of the barrier.

A number of problems exist in their calculations of f_p and f_q . Acoustic phonon scattering was neglected in the calculation of f_p and this must result in an overestimation of f_p . In order to calculate f_q an assumption had to be made about the exact form of the image potential close to the surface of the metal, which casts some uncertainty over the calculations. Also their use of an effective mass approximation may not be valid when the bottom of the conduction band slopes as steeply as it does between the potential maximum and the metal. Having said this however the inclusion of these terms is more accurate than exclusion of them but again it is important to bear in mind the uncertainties associated with them.

For cases where the thermionic-emission theory is valid the effect of f_p and f_q is to replace A^* in equation 1.33 by $A^{**} = f_p f_q A^*$. A^{**} can be as low as half of A^* . This has about the same effect on the current as a change in ϕ_B of less than kT/q , *i.e.* not much, so the difference between A^* and A^{**} is not all that important. However with this final refinement the equation used for later analysis has been explained.

References [38] to [35] are used throughout this section.

1.4 Tunnel Barriers

Tunnelling is a quantum mechanical process in which electrons have a finite probability to cross an insulating barrier. Tunnelling through such a barrier depends on the application of a bias between two electrodes, usually metallic, on either side of the barrier. At zero bias the Fermi levels of the two electrodes are aligned and so currents from either side of the junction cancel each other out. When a non-zero bias voltage, V , is applied the electrode Fermi levels shift by electron volts (eV) relative to each other. There are two unique wave

⁶The temperature dependence comes from the dependence of electron energy on temperature.

functions on either side of the barrier which give the tunnel current through the barrier as demonstrated in figure 1.17. Baden used a perturbation technique to describe these

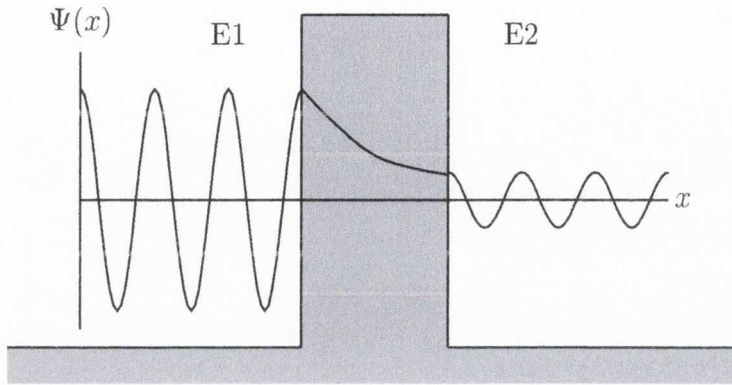


Figure 1.17: Depiction of the wave nature of the tunnelling of electrons.

unique wave functions on either side of barrier, assuming a finite length and an abrupt potential step. Hence the tunnel current can now be given as [40],

$$I(V) = \int \rho_1(E) \rho_2(E - eV) [f(E) - f(E - eV)] |M(E)|^2 dE \quad (1.42)$$

Where $\rho_1(E)$ and $\rho_2(E)$ are the density of states in electrodes E1 and E2, $f(E)$ is the Fermi function and $M(E)$ is the tunnel transfer matrix for electrons with energy E tunnelling from one side of the barrier to the other. The velocity of the electrons entering $M(E)$ is proportional to $\partial E / \partial k$ and inversely proportional to the density of states, ρ . Multiplying these results in the complete absence of the density of states results in the formula given by Harrison [41],

$$I = \frac{4\pi m_i e}{h^3} \int_0^\infty \int_0^{\frac{m_i E}{m_i}} \mathbf{T}(E, E_t) [f(E) - f(E - eV)] dE_t dE \quad (1.43)$$

f is the Fermi distribution and E_t is the energy component perpendicular to the direction of tunnelling and equal to $m_i / 2k_t$. \mathbf{T} is the transmission probability and m_i is the effective

electron mass inside the tunnel barrier. When the Wentzel-Kramers-Brillouin (WKB) [42] approximation is applied, the transition probability becomes,

$$\mathbf{T}(F, F_t) = \exp \left(-2 \int_{x_1}^{x_2} [-K_x^2(F, F_t, x)]^{\frac{1}{2}} dx \right) \quad (1.44)$$

where K_x is the wave vector of the carrier in the barrier. The integrand of equation 1.44 depends on the shape of the tunnel barrier. The simplest shape is a rectangular barrier which assumes that the work functions of both the electrodes are the same. However, even in experiments with the same materials on either side of the barrier, this assumption does not hold true for most tunnel systems as an asymmetry can exist due to the difference in the fabrication of the two interfaces [43]. Therefore a trapezoidal barrier is usually assumed. The one band model for the insulator in this case leads to,

$$K_x^2 = \frac{2m_e}{\hbar^2} \left(E - \psi_1 - (\psi_2 - \psi_1 + eV) \frac{x}{d} - E_t \right) \quad (1.45)$$

where the top of the valence band is at infinitely negative energies.

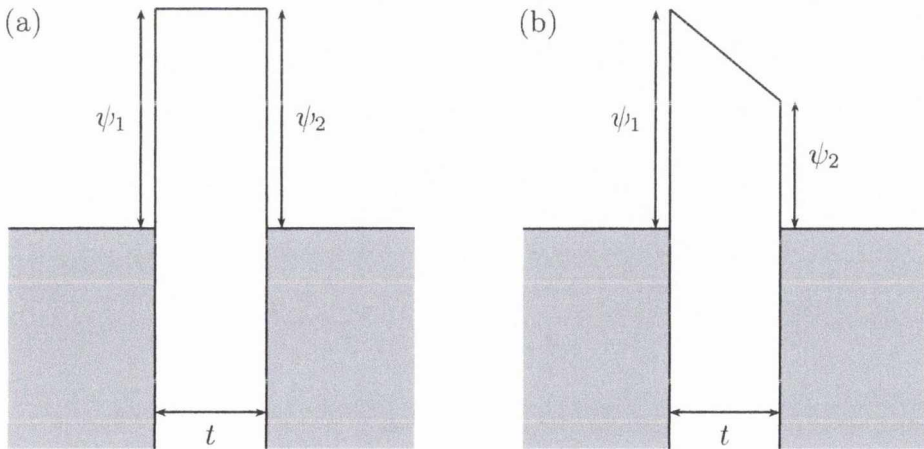


Figure 1.18: Approximations of the barrier shape, (a) rectangular and (b) trapezoidal.

Simmons introduced a mean barrier height, $\bar{\phi}$, in order to treat both rectangular [44] and trapezoidal [45] barriers, arriving at the following formula for voltages below the

barrier height,

$$j = \frac{e}{2\pi\hbar t^2} \left\{ \left(q\bar{\phi} - \frac{eV}{2} \right) \exp \left[-\alpha t \left(q\bar{\phi} - \frac{eV}{2} \right)^{\frac{1}{2}} \right] - \left(q\bar{\phi} + \frac{eV}{2} \right) \exp \left[-\alpha t \left(q\bar{\phi} + \frac{eV}{2} \right)^{\frac{1}{2}} \right] \right\} \quad (1.46)$$

Where j is the tunnelling current density, $\bar{\phi}$ is the barrier height, t is the barrier thickness, m_e is the electron mass, \hbar is Plank's constant and $\alpha = \frac{4\pi}{\hbar} (2m_{eff})^{\frac{1}{2}} = 1.025 \text{ \AA}^{-1} eV^{-\frac{1}{2}}$. Simmons derived the following formula when restricted to very low voltages [45],

$$j = \vartheta (V + \gamma V^3) \quad (1.47)$$

$$\text{where, } \vartheta = \left(\frac{e}{\hbar} \right)^2 \left(\frac{\sqrt{2m_e q \bar{\phi}}}{t} \right) \exp \left(-\alpha t \sqrt{q \bar{\phi}} \right)^{\frac{3}{2}}$$

$$\text{and } \gamma = \frac{(\alpha t e)^2}{96 q \bar{\phi}} - \frac{\alpha t e^2}{32} \left(\frac{1}{q \bar{\phi}} \right)^{\frac{3}{2}}$$

Assuming the barrier height, $\bar{\phi}$, is given in eV, the thickness, t , given in \AA and the current density, j , in Acm^{-2} equation 1.47 becomes,

$$j = 3.16e10 \left(\frac{\bar{\phi}^{\frac{1}{2}}}{t} \right) \exp \left[-1.025 (\bar{\phi})^{\frac{1}{2}} \right] \left(V + \left[0.0109 \left(\frac{t^2}{\bar{\phi}} \right) + 0.032 \left(\frac{t}{\bar{\phi}^{\frac{3}{2}}} \right) \right] V^3 \right) \quad (1.48)$$

having replaced the natural constants with their numerical values.

Brinkman uses a more refined analysis that takes account of the asymmetry of the barrier [46]. The difference between the work functions of the electrodes, $\Delta\phi_M$, is just

$\phi_{M2} - \phi_{M1}$. This results in the expression for the conductance

$$G(V) = G(0) \left[1 - \left(\frac{A_0 \Delta \phi_M}{16 \bar{\phi}^3} \right) eV + \left(\frac{9A_0^2}{128 \bar{\phi}} \right) (eV)^2 \right] \quad (1.49)$$

Where $G(0) = \vartheta$ and is the conductance at very low bias and $A_0 = \frac{4t}{3\hbar} (2m_{eff})^{\frac{1}{2}}$. This can be transformed into an expression for the voltage dependence of the current density, j , in Acm^{-2} .

$$j = 3.16c10 \left(\frac{\bar{\phi}^{\frac{1}{2}}}{t} \right) \exp \left[-1.025 (\bar{\phi})^{\frac{1}{2}} t \right] \left[V - 0.0213 \left(\frac{t \Delta \phi_M}{\bar{\phi}^3} \right) V^2 + 0.0109 \left(\frac{t^2}{\bar{\phi}} \right) V^3 \right] \quad (1.50)$$

The voltage is in volts, the barrier thickness in \AA and the mean barrier height, $\bar{\phi}$, and the asymmetry difference, $\Delta \phi_M$, are both in eV. When compared to the Simmons formula, equation 1.48, it is clear that the first terms are equal in both and the difference between the third terms is related by the second part of the Simmons equation. Using a third order polynomial fit to equation 1.50 it is possible to deduce the barrier parameters of interest.

However using these equations to determine parameters such as the energetic barrier height and the spatial width can be problematic due to the fact that the increase in both of them leads to a higher tunnel resistance. Another problem is that these equations depend on a number of other parameters, which have assumed values that may not be strictly true, for example the effective electron mass, m_{eff} . Also the effect of the valence band cannot always be neglected, particularly using Al_2O_3 based tunnel systems as it has a band gap of 5 eV and in many cases the barrier height can be more than 1 V. Therefore caution must be used when interpreting results from fits to equations 1.43, 1.46, 1.48 and 1.49.

During the tunnelling process the spin of the electron is conserved, making tunnel

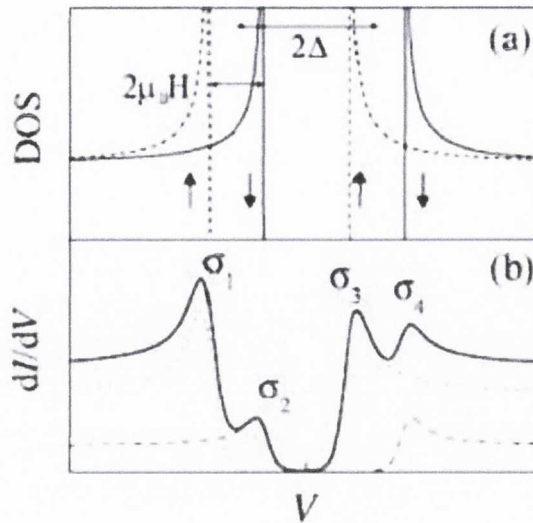


Figure 1.19: Tunnelling in an FM / I / SC junction, (a) is the DOS of a superconductor and (b) is the conductance as a function of voltage for each spin orientation.

barriers of great interest to the field of spintronics. This can be demonstrated looking at the ferromagnet / insulator / semiconductor (FM/I/SC) system used by Tedrow and Meservy [47, 48], which was one of the very first spin polarized tunnelling experiments carried out (1970), and is still one of the preferred methods used to determine tunnelling parameters. The superconducting aluminium layer is the detector of the spin polarization of the current emitted from the ferromagnet that has tunnelled through an AlO_x insulator. The quasi-particle states in the thin superconducting Al film split when a magnetic field is applied parallel to the film. This split is due to Zeeman interaction of the H-field with the spin of the electron. The density of states (DOS) of the superconductor is the superposition of the spin up and spin down contributions, separated by an energy of $2\mu_B B$, allowing the separation of the contributions from spin up and spin down in tunnelling current. Hence the spin conductance of the superconductor ought to be reflected in the peaks in conductance in figure 1.19. The spin polarization, P , of the ferromagnetic near

the Fermi level, E_F , can be given in terms of the conductance as,

$$P = \frac{G^\uparrow - G^\downarrow}{G^\uparrow + G^\downarrow} = \frac{(\sigma_4 - \sigma_2) - (\sigma_1 - \sigma_3)}{(\sigma_4 - \sigma_2) + (\sigma_1 - \sigma_3)} \quad (1.51)$$

List of Symbols

m	– magnetic moment
s	– spin angular momentum
e	– charge of an electron
m_e	– mass of an electron
m_{eff}	– effective mass of an electron
m_i	– effective mass of an electron inside a tunnel barrier
h	– Plank's constant
\hbar	– Planks constant divided by 2π
τ_{sf}	– spin flip scattering time
τ_e	– electron scattering time
E_{vacuum}	– energy of the vacuum level
$\mu_{\uparrow}, \mu_{\downarrow}$ and $\mu_{\uparrow,\downarrow}$	– chemical potentials
μ_0	– chemical potential with no spin effect
E_F	– energy of the Fermi level
$E_{F,m}$	– energy of the Fermi level specific to the metal
$E_{F,s}$	– energy of the Fermi level specific to the semiconductor
E_{F_n}	– Fermi energy in an n-type semiconductor
E_{F_p}	– Fermi energy in an p-type semiconductor
E_C	– energy of the conduction band in the semiconductor
E_V	– energy of the valence band in the semiconductor
E_g	– band gap of the semiconductor
q	– positive charge equal in magnitude to the charge on an electron
ϕ_B	– barrier height
ϕ_M	– work function of the metal
ϕ_I	– built-in potential
ϕ_E	– effective barrier
$\bar{\phi}$	– mean barrier height
$\Delta\phi_{BI}$	– amount by which the barrier height is lowered due to the image force
$\Delta\phi_M$	– difference between two work functions
χ	– semiconductor electron affinity
V and V_a	– applied voltage
V_d	– diffusion potential
V_{d0}	– diffusion potential for zero applied bias
ζ	– quasi Fermi level
ζ_n	– quasi Fermi level for electrons
J	– current density
J_0	– current density for zero applied bias
j	– tunnelling current density
n	– carrier concentration
μ	– mobility of the charge carriers in the semiconductor

D_n	–	diffusion constant of charge carriers in the semiconductor
\mathcal{E}	–	electric field
k	–	Boltzmann's constant
T	–	temperature
\mathcal{N}_C	–	effective density of states in the conduction band
N_d	–	donor density
ϵ_s	–	permittivity of the semiconductor
p	–	tunnelling probability, also fraction, of electrons from the semiconductor into the metal
\bar{v}	–	Maxwellian distribution of velocities
m_{eff}	–	effective mass of an electron
A^*	–	Richardson's constant
A^{**}	–	effective Richardson constant
n	–	ideality factor
f_p	–	probability of an electron reaching the metal
f_q	–	quantum tunnelling factor
$\rho(F)$	–	density of states of an electrode
$f(F)$	–	Fermi distribution function
$M(E)$	–	tunnel transfer matrix
\mathbf{T}	–	transmission probability
K_x	–	wave vector of a carrier in a tunnel barrier
t	–	thickness
G	–	conductance
P	–	spin polarization

The chemical potential and mobility must not be confused with each other.

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Chapter 2

Experimental Techniques

2.1 Sample Deposition

2.1.1 Magnetron Sputtering

Sputtering is a physical process in which atoms in a solid target are ejected into the gas phase due to the bombardment of the surface of the target material by energetic ions. The ions for the process are supplied by a plasma which is created by applying a voltage across a gas, usually Argon, at low pressure, $\sim 10^{-3}$ mbar after the gas has been let into the chamber. The Ar ions then strike the target with sufficient energy to cause the ejection of surface atoms which are deposited onto a substrate. Secondary electrons are also ejected, which cause further ionization of the gas. Magnetron sputtering is a technique where a magnetic field is incorporated into the target gun in order to trap electrons and increase the plasma ionization [1]

2.1.2 Leybold Sputtering System

The Leybold sputtering system used in the deposition of the Fe_3O_4 films was originally designed as an industrial batch deposition tool and it was adapted for use as a experimental sputtering tool after we acquired it in 2002. It is capable of reactive dc magnetron

sputtering and has three separate target slots so it can be used to grow simple multi-layered structures. Each target must be mounted onto a backing plate, inside which sits a permanent magnet. The targets are water-cooled and connected to a dc power supply.

There are two different substrate heaters for the system. One is a large substrate heater that can hold four-inch round substrates. This heater is placed directly under the target to be sputtered and cannot be moved when the chamber is closed. The smaller heater can be rotated between targets. There is an oxygen line and a nitrogen line into the chamber to enable reactive sputtering with either of these gases. The chamber is pumped by a rotary pump for primary vacuum and then a cryopump for high vacuum. The base pressure achieved was typically 4×10^{-7} mbar.

2.1.3 Shamrock Sputtering System

The Shamrock is a fully automated sputtering tool that consists of four high vacuum chambers. The cassette module, the transfer module and two different deposition chambers. The transport module is separated from the deposition chambers and the cassette module by slot valves. The system is housed in a class 10,000 clean-room.

The transfer module is the central chamber and it houses the robot arm which transfers samples to and from the cassette module and deposition chambers. The cassette module is where samples are loaded into a cassette elevator. This can hold up to sixteen $4\frac{1}{2}$ inch square substrates. $4\frac{1}{2}$ inch square metal adaptors are used which can hold 4" and 2" round, 1" \times 1", 10 mm \times 10 mm and 5 mm \times 5 mm square substrates.

Chamber A

This chamber was originally a commercial magnetron sputtering tool similar to those used for the fabrication of AMR and GMR devices at Seagate. It was the original chamber and was acquired by the group in 2002.

Chamber A is a sputter up deposition system. The chamber base holds six three

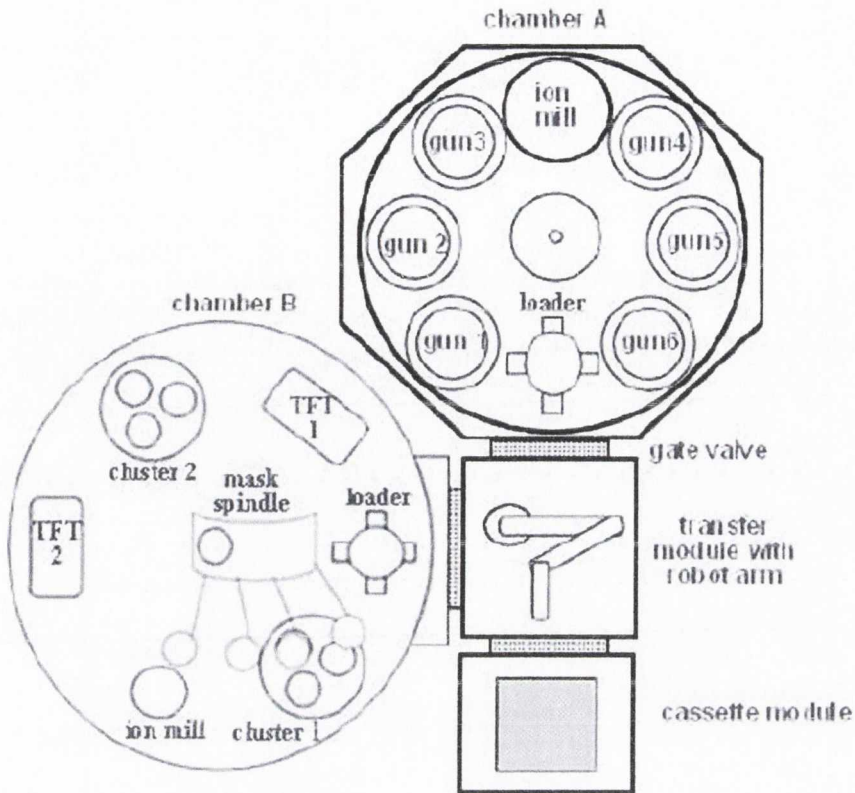


Figure 2.1: Schematic of the all chambers of the Shamrock as it existed in 2008.

inch, dc mode, water-cooled Series III magnetron S-guns. A magnetic field parallel to the cathode surface is produced by an array of permanent magnets surrounding the cathode water jacket. This field intercepts the cathode surface at two places to form an electron trap to limit the primary electron motion to the vicinity of the cathode, which increases the ionization efficiency. An anode bias can also be applied to the guns to increase the deposition rate if required but this is not essential. There are six power supplies to control the cathode bias and two to control the anode bias, one between three guns denoted 1-3 and 4-6. Guns 5 and 6 can also work in RF mode and gun 2 can use a pulsed dc supply. The targets used are cup shaped with a three inch diameter, as shown in figure 2.2. Changing these targets is a simple process that can be carried out in about fifteen minutes. One disadvantage of the magnetron sputtering configuration as evidenced by

six-inch, substrates from three inch targets. Each substrate planet contains an integrated array of permanent magnets with in-plane field strength of 5 mT for growth-induced easy axis, figure 2.3 part (b). A disadvantage of the planetary motion is that the substrates cannot be easily heated.

Typical base pressure in Chamber A is 2×10^{-7} Torr. The process pressure through the introduction of high purity Ar is usually 4×10^{-3} Torr. The chamber is capable of reactive sputtering, oxygen can be introduced into the whole chamber via a mass flow controller (MFC) or just to gun 5. Gun 5 has a special reactive gas ring with a separate MFC to allow reactive sputtering. This was typically designed and originally used for the fabrication of AlO_x tunnel barriers. Film thickness is controlled by deposition time. The rate is calibrated by measuring the thickness of calibration samples using X-ray reflectometry, which will be described later. Typical deposition parameters are shown in table 2.1

Targets	Deposition Pressure (mTorr)	Ar flow (sccm)	Gun no.	Power (watts)	Deposition rate ($\text{\AA}/\text{s}$)
$\text{Ni}_{81}\text{Fe}_{19}$	4	25	1	100	0.186
$\text{Co}_{90}\text{Fe}_{10}$	4	25	2	100	0.114
$\text{Co}_{80}\text{Fe}_{10}\text{B}_{10}$	4	25	3	100	0.112
$\text{Co}_{40}\text{Fe}_{40}\text{B}_{20}$	4	25	3	100	0.103
$\text{Ir}_{20}\text{Mn}_{80}$	4	25	4	100	0.800
Ru	4	25	5	100	0.056
Ta	4	25	6	150	0.107
Cu	4	25	5	100	0.202
Al	4	25	5	100	0.134

Table 2.1: Typical deposition parameters for the most commonly used targets in Chamber A.

Chamber B

The PLASSYS MP900 (Chamber B) was installed on the left side of the transfer module and shares the sample loading and unloading system with Chamber A. This chamber was new and specifically designed for the deposition of oxides and alloys. There are a number of components making up this chamber, a schematic of these is shown in figure 2.4 part (b).

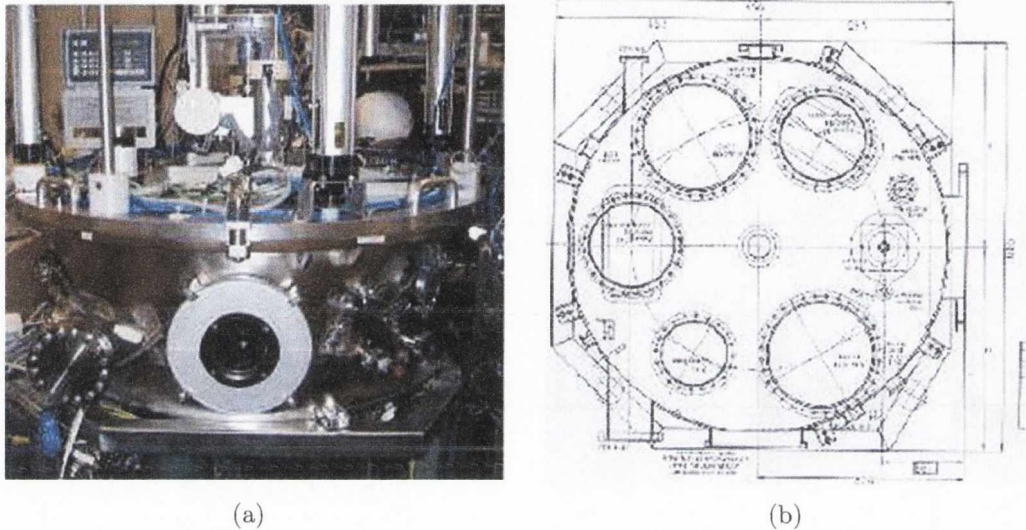


Figure 2.4: (a) Outside view of PLASSYS MP900 Sputtering System, Chamber B (b) schematic for components in Chamber B.

There are two target facing target (TFT) guns that are connected to the same RF power supply. These can be used to sputter both conductive and insulating materials. High quality MgO , AlO_x and SiO_2 thin films have been produced using these targets. There are two three-target clusters for dc sputtering. Each target incorporates an automated shutter, gas ring for reactive sputtering and a shielding chimney to prevent cross contamination. The targets in each cluster are tilted, giving a focal point to each cluster to convert from sequential to co-deposition, allowing the formation of alloys from up to three elemental targets. For example in the past one cluster has been used to successfully produce Co doped ZnO using a cluster containing a Zn and Co target which were

reactively sputtered.

There is also an ion milling gun. This can be used for substrate cleaning and surface smoothing. There is an oxygen line and a argon line connected to the gun allowing cleaning with an oxygen plasma, ideal for removing organic dirt, and an argon plasma, ideal for removing oxides. The substrate heater in the chamber can heat up to 750°C during deposition, or afterwards for in-situ annealing. Typical deposition parameters for

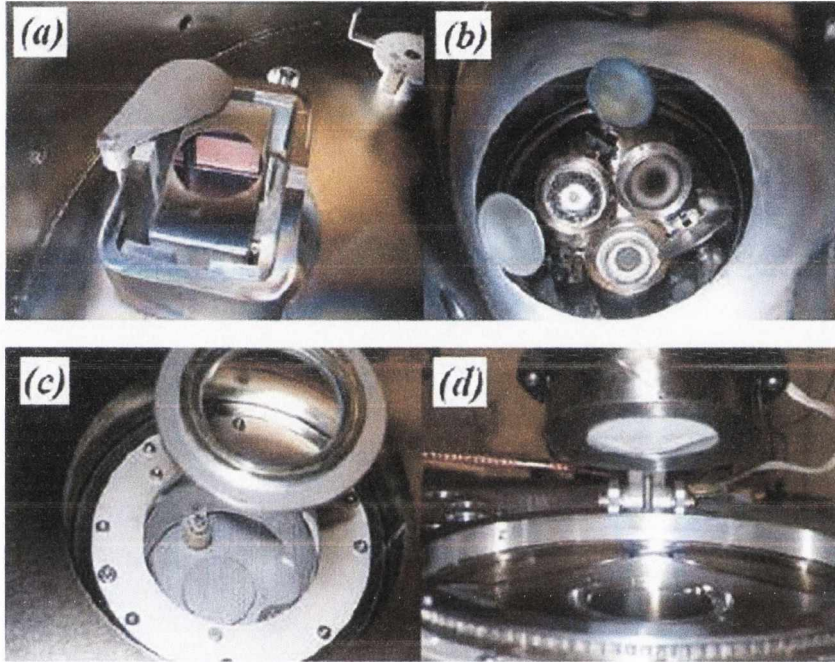


Figure 2.5: Photographs of some of the various components in Chamber B (a) TFT gun (b) cluster (c) ion milling gun (d) substrate heater.

Chamber B are shown in table 2.2

2.1.4 Thermal Evaporation

Thermal evaporation is a technique used to deposit a thin film of a metal onto a substrate. The desired metal is evaporated in a vacuum environment and the atomic cloud formed coats all surfaces in a line the sight of the metal source. This method can produce smooth, shiny films up to about $0.5\ \mu\text{m}$ thick. However the coating is fragile and can easily peel

Targets	Deposition Pressure (mTorr)	Ar flow (sccm)	Gun no.	Power (watts)	Deposition rate ($\text{\AA}/s$)
MgO	0.7	5	TFT1	75	0.129
MgO	5.0	35	TFT1	75	0.083
MgO	10	90	TFT1	75	0.071
SiO ₂	2.1	20	TFT2	100	0.156
AlO _x	2.1	20	TFT2	100	0.110

Table 2.2: Typical deposition parameters for the most commonly used targets in Chamber B.

off, which renders the technique unsuitable for high-resolution lithography applications. It is also unsuitable for metals with a high melting point. It is very useful for the creation of metallic contacts and all ohmic contacts to GaAs were made using using this technique. The evaporator used here is an Edwards Auto 306 evaporator and the operating vacuum in the chamber is typically 5×10^{-6} mbar.

2.2 Structure Characterization

2.2.1 X-ray analysis

X-ray scattering is a very good and widely used tool to obtain structural information about materials and films. The characteristic wavelengths of x-rays are of the order of inter-atomic distances in typical lattice structures, their penetration depths in metals are several μm and all analysis is non-destructive. All scans in this thesis were taken using a Philips Xpert Pro system, which uses Cu-K $_{\alpha}$ radiation. This has a wavelength of $\lambda = 1.5406\text{\AA}$.

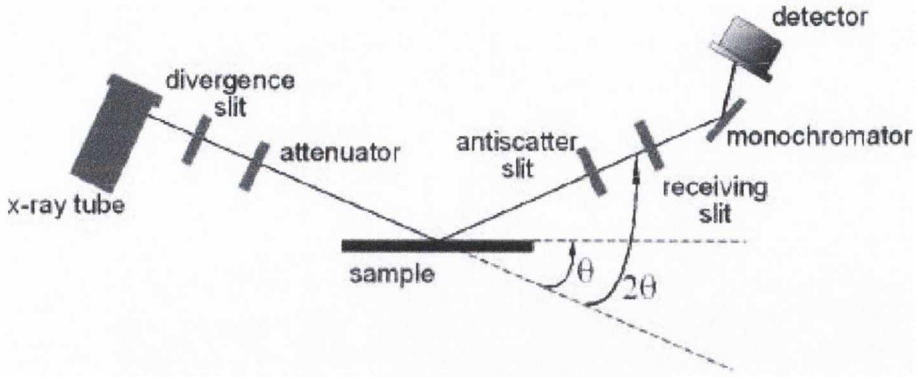


Figure 2.6: Experimental setup for x-ray analysis.

X-ray Reflectometry

X-ray reflectometry (XRR) is a technique used to measure the thickness and roughness of thin films. When x-rays are applied to a metal's flat surface at a grazing angle of incidence ($0^\circ < \theta \leq 10^\circ$), total reflection will occur at or below a certain critical angle, θ_C , and the value of this angle depends on the electronic density and refractive index of the material. The higher the incident x-ray angle is relative to θ_C the deeper the x-rays penetrate the material. Above θ_C an interference pattern is formed between reflections from the film surface and from the film / substrate interface. This results in a series maxima in the reflected intensity. The maxima positions can be determined by analogy to the Bragg positions in lattice diffraction. The Bragg equation at low angles can be approximated as,

$$\sin^2 \theta_m = \left(\frac{m\lambda}{2D} \right)^2 \quad (2.1)$$

where θ_m is the position of the m^{th} fringe, D is the film thickness, λ is the wavelength of X-ray radiation. A plot of $\sin^2 \theta_m$ versus the order m peaks should give a straight line, the slope of which gives the film thickness [2].

A typical low angle reflectometry scan is shown in figure 2.7. X-ray scans that were

generated were fitted using the Philips software WINGIXA. All features that can appear in a thickness scan are highlighted in figure 2.7 and the sources of these features are briefly explained.

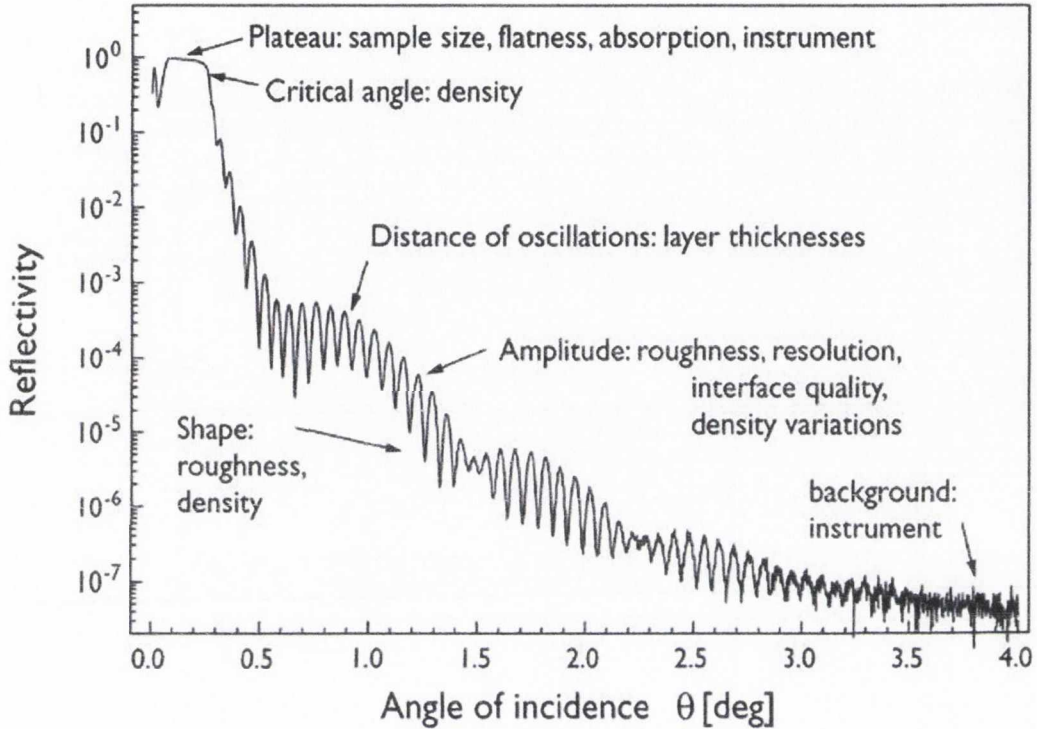


Figure 2.7: A sample x-ray reflectivity curve with its features highlighted and their sources explained (from Philips / Panalytical).

Wide angle diffraction

The term “wide angle” corresponds to the measurement of Bragg reflections of a crystal lattice within the 2θ angle range of $\sim 15^\circ$ to $\sim 170^\circ$. The lattice is a regular three-dimensional distribution of points in space, which is arranged such that a series of parallel lines can be formed in going from one lattice point to another in the same direction. These parallel lines are separated from each other by a distance d , which varies according to the material. Each crystal plane has a number of different orientations, each with its own

specific d value.

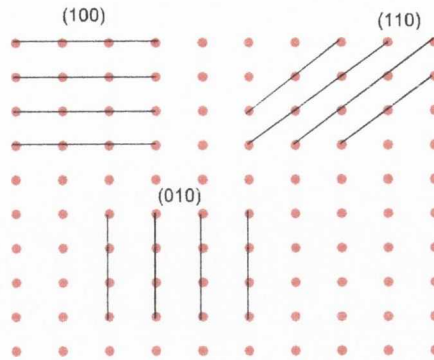


Figure 2.8: Different orientations of crystal planes

Diffraction occurs only when the reflected beam of an incident monochromatic x-ray beam with a wavelength λ at an angle θ have travelled distances that differ by a complete number of n wavelengths, Bragg's law,

$$n\lambda = 2d \sin \theta \quad (2.2)$$

follows from this condition. By varying the angle θ , the Bragg's law condition is satisfied by different d spacings in polycrystalline materials. A plot of the resultant intensities of the diffraction peaks against angular position produces a pattern that is characteristic of the sample measured. Identification of the sample is achieved by comparing the diffraction pattern obtained from the sample with an internationally recognized database containing reference patterns.

2.2.2 Transmission Electron Microscopy (TEM)

The transmission electron microscope (TEM) operates on the same basic principles as the light microscope but uses an electron beam instead of light. The ultimate limiting factor

in resolution when using a microscope is the wavelength of the radiation. Since electrons have a much lower wavelength it is possible to get a resolution of the order of a few \AA , which is comparable to atomic spacing.

The source radiation is generated using an electron gun, which travels through the microscope column under vacuum. A series of electromagnetic lenses and apertures are used to focus the electrons into a tight, coherent beam. The beam then travels through the sample to be studied. As the beam passes through the sample a number of electrons will be lost through scattering, the amount depends on the density of the material being studied. At the bottom of the column the electrons hit a fluorescent screen, which displays a “shadow image” of the sample. The different contrasts correspond to materials of different density and information about interface roughness and diffusion of one layer into another can clearly be seen.

The TEM pictures shown in this thesis are from Departamento de Ciencia de los Materiales e IM y QI, Universidad de Cádiz, Spain.

2.2.3 Superconducting Quantum Interface Device (SQUID)

A Quantum Design Magnetic Property Measurement System (MPMS) magnetometer was used to characterise the magnetic properties of thin films. It uses a superconducting quantum interface device (SQUID) detection system, which is integrated with a temperature control unit, a high field superconducting magnet and a computer operating system. Liquid helium is used both for the refrigeration of the superconducting magnet and for sample cooling allowing measurements to be made from 1.7 K to 300 K in a field of up to 5 T. The sensitivity of the magnetometer is in the order of 10^{-11} Am^2 , which makes it ideal for measuring thin films where the signals may be too weak for detection in a VSM. The magnetic moment of a monolayer of ferromagnetic iron on a $5 \times 5 \text{ mm}^2$ substrate, for example, is of the order of 10^{-8} Am^2

In this thesis, the SQUID was mainly used as a tool to verify film quality, particularly

the Fe_3O_4 thin films, along with x-ray analysis.

2.3 Junction Fabrication Process

The first junctions measured were made by simply cutting the substrate / film stack into small pieces, just less than 1 cm^2 . The edges of the samples were covered with Kapcon tape and the front and back contacts were either evaporated, sputtered or soldered depending on the substrate and whether it was a front or back contact. Later it was decided to fabricate the junctions using a lithographic process in order to have a reproducible, well defined junction area. Later still it was decided to look at the behaviour of the junctions as function of size and further, more difficult lithographic processes were needed to decrease the junction size from the μm range to the 100 nm range. For each junction size a different lithographic method was used.

2.3.1 Ultra Violet (UV) Lithography

UV lithography was used to fabricate the junctions in the μm range. The substrate and films are thoroughly cleaned using an acetone ultrasonic bath. It is extremely important to have clean wafers before the photo-resist is put on as dirt particles can cause flaws in the resist coating far greater than their size. The substrates are dipped in IPA immediately after being removed from the acetone to prevent any acetone residue forming on the substrate and are then blow dried with a high pressure nitrogen gun. To ensure all water vapour has been removed, the wafers are baked at 115°C for 2 minutes prior to resist coating. The substrates are then held on a vacuum spinner and typically spun at 5000 rpm (rotations per minute) for 55 seconds. Provided the wafers are clean this produces a uniformly thick resist coating. The resist used is a positive resist, Shipley S1813. Positive resist means that the area of resist exposed to the UV light is the area removed during development. After spin coating the resist is baked at 115°C for 2 minutes on a hot plate,

which evaporates the solvent in the resist and gives a resist thickness of approximately $1\ \mu\text{m}$. The pattern was exposed through a photo-mask using a Karl Suss MJB 3 mask aligner, which uses a UV light with wavelength of 250 nm. A change occurs in the chemical properties of the resist after an exposure of typically 6 seconds. The exposed resist was then washed away after immersion in a bath of the developer MF319 for 40 to 60 seconds. Excess developer is washed away with DI water and the wafers are again blow dried with the nitrogen gun. At this stage the pattern transfer is complete. All this was carried out in a specially lit class 100 clean room to minimise the risk of dirt particles after cleaning.

At this point, a number of small junctions have been defined on the thin film. To remove the conductive film between junctions the samples are physically etched in the Millatron as described later in this chapter. Before being contacted, the junctions are isolated from each other by using the insulator SiO_2 , which is deposited by sputtering in Chamber B. This also ensures that current flows through the defined junctions and not just through the semiconductor. The resist is then lifted off by leaving the samples in an acetone bath overnight and then placing the acetone bath in an ultrasonic bath for half an hour, sometimes longer. Once the resist is fully removed another UV lithography step is needed to pattern the top contacts. All the lithography steps are the same as before. Once the the contact pattern is transferred to the samples the top contacts are deposited and then the resist is lifted off as before. These steps are shown in figure 2.9. The samples were mounted on the sample space in the cryostat of the RT rig, as shown in figure 2.12, part (b).

2.3.2 E-beam Lithography

As with microscopy, the limiting factor in resolution with lithography is the wavelength of the light source used during exposure. And again the way around this is to use a well focused electron beam. The electron beam used for patterning here comes from a scanning electron microscope that is a component of an FEI strata 235 dual beam FIB.

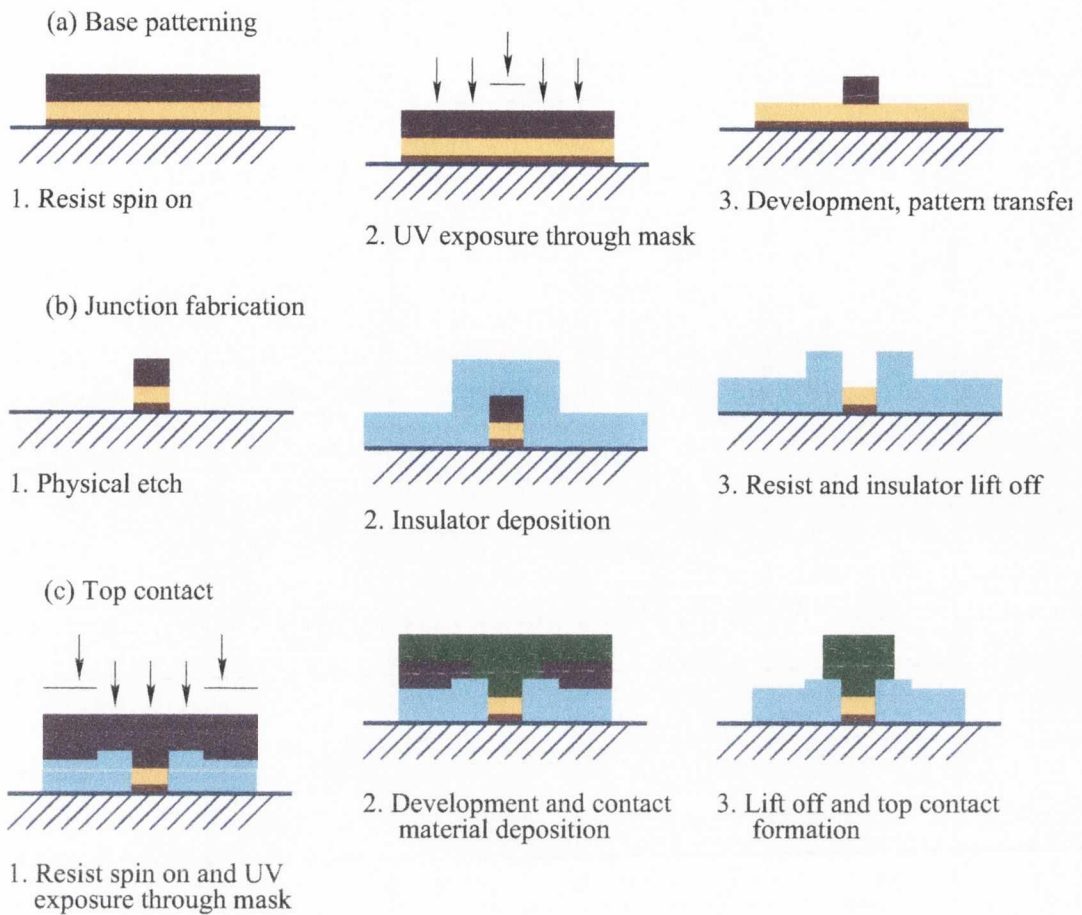


Figure 2.9: Outline of the steps used for the fabrication of junctions in the μm range.

A larger accelerating voltage (30 kV) is used for e-beam lithography than would normally be used for imaging (5 kV). The electron beam is scanned over the resist according to the desired pattern, which is controlled by a computer and means this is an essentially mask-less process. For research applications this is a very convenient and versatile way to achieve patterning on a nanoscale but each sample takes a long time and uniformity over a large area cannot be guaranteed. E-beam lithography is not particularly suitable for industrial applications. The resist used in this case is the negative resist maN2403 and so the exposed pattern is what remains after development. This is an extremely robust resist and makes focusing the electron beam and lift off that bit easier. The samples are cleaned and dried as before prior to the resist coating. The resist is spun on at 5000 rpm

and this time is baked at 90 °C for 1 minute. The FIB is not located in the class 100 area and so care must be taken when transporting the resist coated sample that dirt does not get on it and that is not accidentally exposed by normal light.

The sample is placed in FIB sample chamber that has a base pressure of 10^{-6} mbar. It is important to have the sample a good bit bigger than the patterning area as the SEM detector needs to be focused using the accelerating voltage, aperture size and spot size that will be used for the patterning. Changing one of these will change the focus and so in focusing the resist will become exposed. It is very important not to focus near the area where the pattern will be. After exposure the sample is brought back to the clean room for development, which takes 20 to 40 seconds. The developer AZ726MF was used. The junctions were checked under an optical microscope at short time intervals to prevent over-development of the pattern. Circular junctions with a diameter of 90-100 nm are fabricated using this method of lithography.

2.3.3 Ion Milling Process with an End Point Detector

Ion beam etching is a physical plasma process whereby ions are produced in a cavity and then accelerated to produce a relatively intense and homogeneous beam using an RF power source. The ions effectively sputter away material not protected by photoresist on the sample. The advantage of this technique is anisotropic etching with high aspect ratios for effective pattern transfer. The Millatron system, figure 2.10, consists of a vacuum chamber with a rotational sample stage and a Hiden end point detector, a plasma beam source with an RF power supply, a DC supply, which controls the Helmholtz coils inside the ion gun and a mass flow controller which lets high purity Ar into the chamber.

The base pressure of the system is typically 2×10^{-7} torr and the working pressure is about 5×10^{-5} torr. The RF power is 400 W with a magnet current of 3.5 A. The sample is usually rotated at an angle of 45° to the beam but this angle can easily be changed. The etch rate of each material is specific to that material. One of the most important issues,

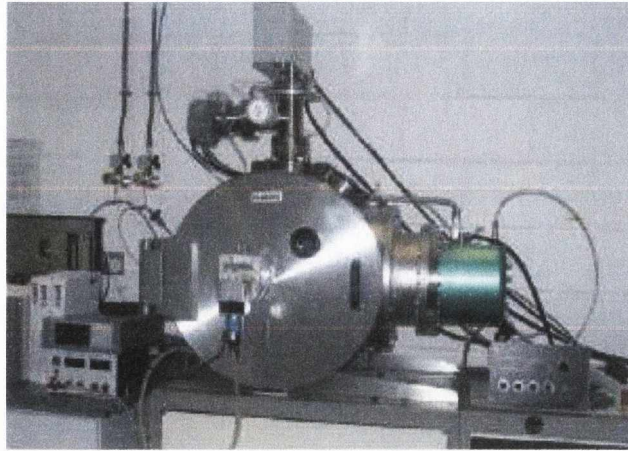


Figure 2.10: The ion etching tool, the Millatron.

particularly for the MJT's grown by the group, was how to stop precisely at a specific layer. For this purpose a Hiden end point detector (EPD) was installed on the top of the Millatron, as shown in figure 2.11. The end point detector consists of an ion milling

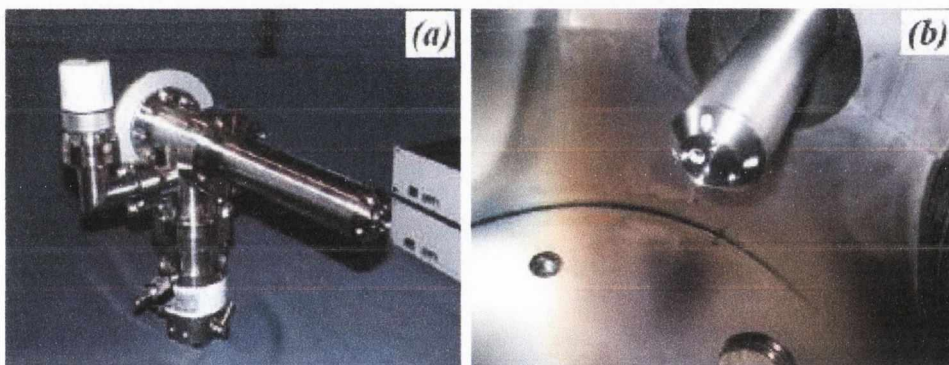


Figure 2.11: Picture of the Hiden end point detector (a) before it was installed and (b) installed inside the Millatron.

probe which in turn consists of an energy filter, quadrupole mass spectrometer and a secondary electron multiplier detector. The EPD also has a radio frequency head with an amplifier and is controlled by a PC running MASsoft. Any ions entering the quadrupole field experience a potential difference deflecting them from their original trajectory, and the extent of the deflection is related to the bias mass-charge ratio (m/e). At each interval

on the RF scan only one mass-charge ratio resonates with the field allowing the ion to pass along the z -axis. All other species are deflected and neutralized by impacting with the rods of the quadrupole. The ion signal is then collected and displayed by the MASsoft software. By monitoring this signal a definite end point / layer can easily be set and achieved.

All lithographically patterned junction sizes were made using the Millatron .

2.3.4 Junction Isolation

Once the junction pillars had been fabricated using the Millatron an insulating layer had to be deposited. This layer served two functions, to isolate the junctions from each other and prevent a short occurring between the top contact and the semiconductor substrate as the top contact was bigger than the actual junction size. The material used was RF sputtered SiO_2 and the typical thickness of this layer was 50 – 65 nm. In order to make sure there was no leakage current through the SiO_2 layer an area of the substrate with no junction was contacted and the resistance measured. The resistance values were between 100's of $\text{M}\Omega$ and $\text{G}\Omega$, depending on the thickness of the SiO_2 layer. These huge resistance values eliminate the possibility of any significant current leakage through the SiO_2 layer.

2.3.5 Ohmic Back Contacts

A lot of work was spent ensuring the back contacts to the semiconductors were actually ohmic, particularly finding the right annealing conditions. For the Silicon the most successful method was scratching the back of the substrate with a diamond scribe immediately prior to high temperature, 400 °C, soldering of indium for more than 2 minutes. The GaAs substrates were contacted by AuGe thermal evaporation, followed by annealing in air at 300 °C for 45 – 60 s. This contact method was used in all van der Pauw measurements outlined in the following section. Part of these measurements provide a quality check to the contacts and in all cases where these methods were used for the correct

semiconductor, the check gave a result indicating good, repeatable ohmic contacts.

2.4 Transport Measurements

The transport measurements were carried out as a function of applied bias and temperature. All junctions were measured in the resistivity rig described below.

2.4.1 The RT Rig

The RT rig, as shown in figure 2.12, is composed of a cryostat that can reach a temperature of 13 K using a He compressor and an electromagnet with a maximum field of 180 mT. This field is generated using a Kepco 10 A bi-polar power supply and no cooling is necessary.

The cryostat can be rotated so that the sample space is in the middle of the two coils of the magnet. This allows measurements as a function of field, temperature and bias to be done relatively quickly and cheaply.

The samples were mounted on the sample space in the cryo-head as shown in figure 2.12, part (b). The samples were held in place using Apiezon N grease, which is thermally

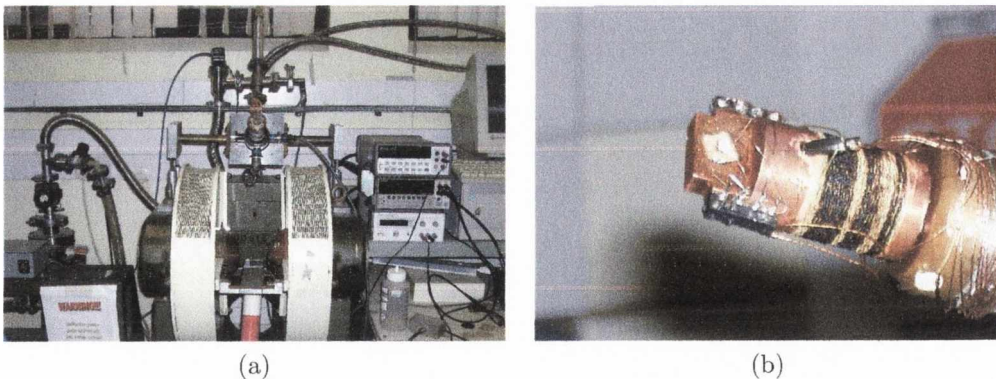


Figure 2.12: Pictures of the RT rig, (a) is the the overall rig consisting of a cryostat and magnet and (b) is the sample holder of cryostat in the rig.

conductive but electrically insulating. Silver wires were attached to the contact pads using silver paint and then wrapped tightly around the pins of the cryo-head. Using a

computer controlled set-up with a Keithley 2400 multimeter a voltage was applied while the current was measured. Current measurements have an error of ± 0.1 nA. To avoid confusion positive bias is always applied to the thin film side of the junctions. A Cryocon temperature controller was used to accurately measure the temperature using two different temperature sensors, a platinum sensor, which is accurate from room temperature to about 40 K, and a Cernox sensor, which is accurate below 50 K. The samples are measured in a four point configuration as a function of bias and temperature.

2.4.2 Van der Pauw Technique

The van der Pauw technique is a method of measuring the Hall voltage and resistivity of a doped semiconductor in order to determine the carrier concentration of the semiconductor. The advantage of this method is that it uses a simply shaped sample of the semiconductor containing four very small ohmic contacts placed in the corners of the sample. The sample should be as square as possible but the van der Pauw technique takes into consideration the fact that perpendicular lengths might not be the same.

Van der Pauw Resistivity Setup

Figure 2.13 shows a typical semiconductor sample used. It is as square as possible but will be deemed to be rectangular to match reality.

The setup shown in figure 2.13 is the setup to determine the resistivity. The two characteristic resistances R_A and R_B are measured by simply applying a dc current, I , from one contact to the other and measuring the voltage, V , across the other two contacts. Using Ohm's Law,

$$V = IR \tag{2.3}$$

the resistances A and B are easily obtained. It is important to pay close attention to

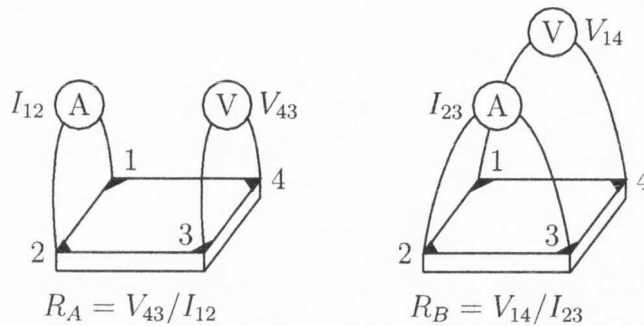


Figure 2.13: Rectangular shaped semiconductor sample set up for van der Pauw method of measuring R_A and R_B , which are needed in order to calculate the resistivity of the semiconductor.

the contact labelling system, the order in which they are numbered has been carefully chosen and all subscript labelling of the current, voltage and resistance corresponds to this system. For example R_A was determined by applying a current into contact 1 and out of contact 2, this is labeled I_{12} , and the voltage was measured from contact 4 to contact 3, this is labeled V_{43} . It is important to know throughout the whole experiment which contact has been chosen as contact 1 ect. The sheet resistance R_S is determined through the van der Pauw equation,

$$\exp\left(-\frac{R_A}{R_S}\pi\right) + \exp\left(-\frac{R_B}{R_S}\pi\right) = 1 \quad (2.4)$$

where R_A and R_B have been shown in figure 2.13 to be $R_A = V_{43}/I_{12}$ and $R_B = V_{14}/I_{23}$. However all ohmic contacts are unlikely to be the same size and as mentioned before the sample sides are unlikely to be exactly equal so an average of four resistances is used. In total eight voltage measurements were performed in order to calculate eight resistances,

all of which *must be positive*. The resistances that were needed are as follows:

$$\begin{aligned}
 R_{21,34} &= \frac{V_{34}}{I_{21}} & R_{12,43} &= \frac{V_{43}}{I_{12}} \\
 R_{32,41} &= \frac{V_{41}}{I_{32}} & R_{23,14} &= \frac{V_{14}}{I_{23}} \\
 R_{43,12} &= \frac{V_{12}}{I_{43}} & R_{34,21} &= \frac{V_{21}}{I_{34}} \\
 R_{14,23} &= \frac{V_{23}}{I_{14}} & R_{41,32} &= \frac{V_{32}}{I_{41}}
 \end{aligned} \tag{2.5}$$

The second half of these resistances are used as consistency check on measurement repeatability, ohmic contact quality and sample uniformity since,

$$\begin{aligned}
 R_{21,34} &= R_{12,43} & R_{43,12} &= R_{34,21} \\
 R_{32,41} &= R_{23,14} & R_{14,23} &= R_{41,32}
 \end{aligned} \tag{2.6}$$

and the reciprocity theorem requires that,

$$\begin{aligned}
 R_{21,34} + R_{12,43} &= R_{43,12} + R_{34,21} \\
 R_{32,41} + R_{23,14} &= R_{14,23} + R_{41,32}
 \end{aligned} \tag{2.7}$$

If either equation 2.6 or equation 2.7 fail to be true within 5 % then sources of error must be investigated.

R_A and R_B are calculated from,

$$\begin{aligned}
 R_A &= \frac{R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21}}{4} \\
 R_B &= \frac{R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32}}{4}
 \end{aligned} \tag{2.8}$$

R_S was found by solving equation 2.4 numerically using a LabVIEW program which is shown in Appendix B. The bulk resistivity, ρ , is then simply calculated from [3]

$$\rho = R_S d \tag{2.9}$$

Van der Pauw Hall Voltage Setup

The van der Pauw Hall voltage measurement consists of a series of voltage measurements using a constant current, I , and a constant magnetic field, B , applied perpendicular to the plane of the sample. The sample set up is shown in figure 2.14. The sheet carrier

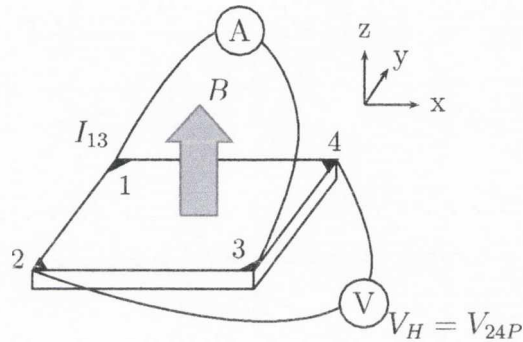


Figure 2.14: Semiconductor sample set up to measure Hall voltage. This is the sample as shown in figure 2.13, making this convenient to measure both resistivity and carrier concentration.

density, n_S , is the first parameter obtained from the Hall measurements and the bulk carrier density (or concentration) is just the sheet density divided by the thickness of the semiconductor sample.

One of the largest difficulties in obtaining accurate Hall results comes from an offset voltage due to non-symmetric contact placement, shape and non-uniform temperature across the sample. A way around this is to take two sets of Hall measurements, one for positive field and one for negative field. The current labelling system stays the same but this time a subscript P and N will be included with voltage labelling to differentiate between the voltages measured in the positive and negative applied magnetic fields respectively. It is important that both fields are of the the same magnitude.

The actual procedure for the Hall measurement is quite straight forward. A positive

B field is applied perpendicular to the sample. A current, I_{13} , is applied to contacts 1 and 3, as specified in figures 2.13 and 2.14, and the voltage, V_{24P} is measured. The current is then applied to contacts 3 and 1 to become I_{31} and V_{42P} is measured. Similarly the current is applied in the I_{24} and I_{42} formation and the voltages V_{31P} and V_{13P} are measured respectively. The field is then reversed and procedure is repeated this time to get V_{24N} , V_{42N} , V_{31N} and V_{13N} . These eight voltage measurements are used to determine if the sample is n or p type and to calculate the sheet carrier density, n_s or p_s .

$$\begin{aligned} V_C &= V_{24P} - V_{24N} & V_D &= V_{42P} - V_{42N} \\ V_E &= V_{13P} - V_{13N} & V_F &= V_{31P} - V_{31N} \end{aligned} \quad (2.10)$$

It is very important that sign of the measured voltages are maintained. The semiconductor type is determined simply from the sum of these four voltages, $V_C + V_D + V_E + V_F$, and if the result is positive the semiconductor is p-type but if it is negative it is n-type.

The sheet carrier density in units of cm^{-2} is calculated using,

$$\begin{aligned} p_s &= \frac{8 \times 10^{-8} IB}{q(V_C + V_D + V_E + V_F)} \\ n_s &= \left| \frac{8 \times 10^{-8} IB}{q(V_C + V_D + V_E + V_F)} \right| \end{aligned} \quad (2.11)$$

The units used here are extremely important, B is the magnetic field in **gauss (G)** and I is the dc currents in **amps (A)**. By dividing the sheet carrier density by the thickness of the sample in **cm** the carrier concentration is extracted. This is done automatically in the programme shown in Appendix B and the carrier concentration is given in units of cm^{-3} .

References

- [1] S.M. Sze and C.Y. Chang, *ULSI Technology*, McGraw-Hill
- [2] M.Hecker, *X-ray Scattering Techniques* chapter in *Metal Based Thin Films for Electronics*, edited by K.Wetzig and C.M. Schneider
- [3] NIST website, section on Hall Effect

Chapter 3

Magnetite / Semiconductor Junctions

3.1 Introduction

A possibility for the generation of spin polarized currents in semiconductors is the use of a half metal as the spin injector. Half metals have a completely spin polarized conduction band, as discussed below, and therefore should give higher spin injection efficiencies than *3d* transition metal injectors.

3.1.1 Half Metals

Half metals, by definition, have only one spin channel for conduction electrons at the Fermi level [1]. For electrons with spin orientation in one direction the material behaves as a metal, however for electrons orientated in the other direction the material behaves as an insulator [2]. The existence of only one spin orientation at the Fermi level makes these materials of considerable interest as a spin injection source. Not even the strong normal ferromagnets have electrons at the Fermi level with only one spin orientation. For example, cobalt and nickel, which are strong ferromagnets, have fully spin polarized

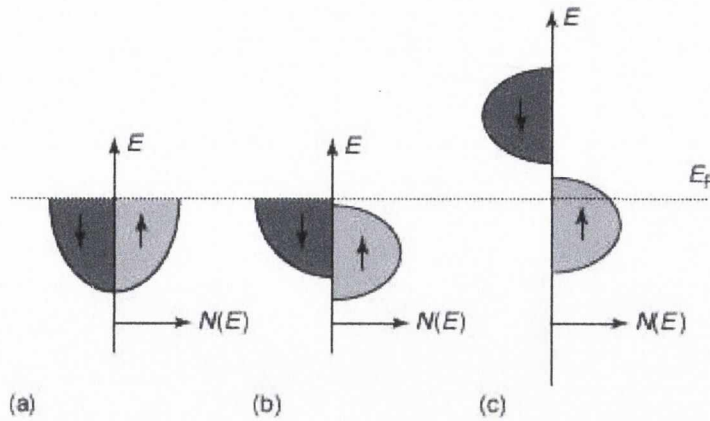


Figure 3.1: Schematic of the density of states for (a) a normal (b) a ferromagnet and (c) a half metal.

d -bands with a filled $\uparrow 3d$ band, leaving only $\downarrow d$ electrons at the Fermi level, E_F . However the Fermi level in these materials also cross the $4s$ band, which is practically unpolarized, giving a population of both \uparrow and \downarrow electrons in the Fermi level. The reason half metals are fully polarized is that they have a band gap which separates the fully polarized d -band from the unpolarized s -band. A schematic comparison of the density of states for a normal, ferromagnetic and half metal is shown in figure 3.1. This band structure occurs by either pushing the $4s$ band above the Fermi level or by depressing the Fermi level below the $4s$ band. This is achieved by hybridization and therefore all half metals consist of more than one element. Most known examples are oxides, sulphides or Heusler alloys.

Classification of Half Metals

There are four categories into which half metals can be classified. Type I half metals have only one spin orientated electrons appearing at E_F . Type II half metals are similar but the electrons lie in a sufficiently narrow band for them to be localized. The heavy carriers can then form polarons and conduction takes place via electron hopping between spin polarized sites. In type III half metals both bands have a density of states at E_F but the carriers in one band have a much larger effective mass than those in the other, they

are also known as transport half metals. In electrical transport only one type of carrier contributes significantly to conduction. Type IV half metals are actually magnetically ordered semimetals with a large difference between the effective masses of electrons and holes. Semimetals and half metals are very different, most semimetals are not magnetic and they have small numbers of electrons and holes, usually equal in number, due to a small overlap between the valence and conduction bands. Bismuth, graphite and antimony are the most common examples of semimetallic materials.

Most of these types of half metals can be sub-divided into A and B groups. The A group corresponds to half metals where the \uparrow spin electrons are present at the Fermi level and in the B group it is the \downarrow electrons. A schematic of the density of states for the different types of half metals is shown in figure 3.2

Magnetite, Fe_3O_4

Magnetite is one of the most famous magnetic materials and has the highest Curie temperature among oxides. A spin polarization of 80% or more has been measured at room temperature [4] & [5]. Fe_3O_4 is a type IIB half metal and so conduction occurs via polaronic hopping in a minority spin band [6]. It has a mixed valence of both Fe^{2+} and Fe^{3+} . These populate the B-sites of the spinel structure in equal proportions giving an average B-site configuration of $(t_{2g}^3 e_g^2)^\uparrow (t_{2g}^{0.5})^\downarrow$. The A-sites contain oppositely magnetized $\text{Fe}^{3+}(t_{2g}^3 e_g^2)^\downarrow$ cores. The two sites have distinct crystallographic structures, A being tetrahedrally and B octahedrally coordinated. This results in different average Fe-O distances, 1.8776 Å for the A site Fe ions and 2.066 Å for the B site Fe ions, hence the sites have different oxidation states [7]. The polarons are formed by the \downarrow B-site electrons and hop among the B-sites [8]. The resistance of magnetite increases with decreasing temperature and this dependence could be utilized to reduce the conductivity mismatch between the Fe_3O_4 film and the semiconductor substrate. At approximately 120 K bulk magnetite undergoes a transition in which a spontaneous inter-correlated change of the lattice sym-

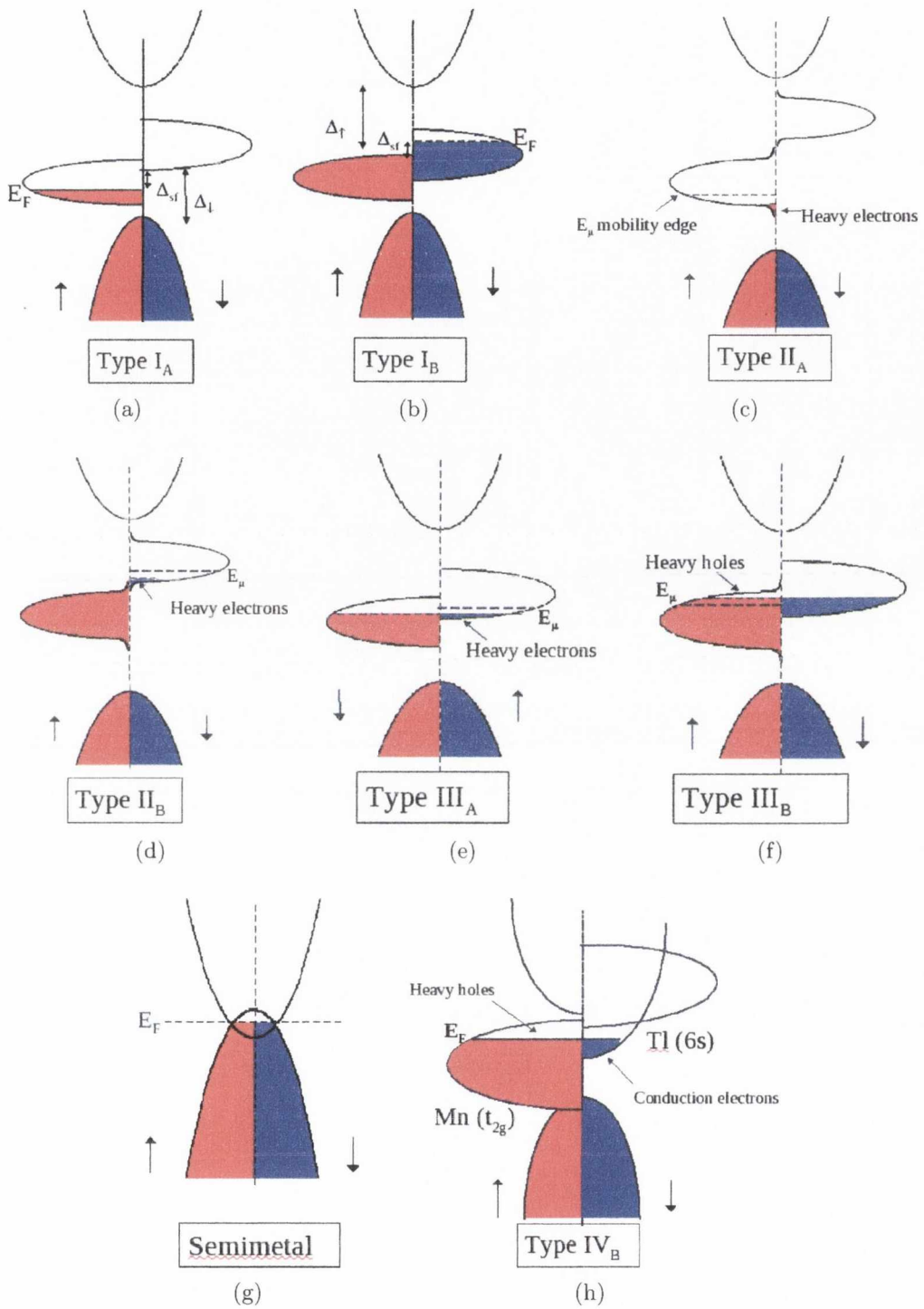


Figure 3.2: Schematic of the density of states for different half metals. (a) Type IA with only \uparrow electrons at E_F , (b) type IB with only \downarrow electrons, (c) type IIA, (d) type IIB, (e) type IIIA, (f) type IIIB, (g) a typical semimetal, Bi, and (h) type IV, a half metallic semimetal, $Tl_2Mn_2O_7$ is shown.

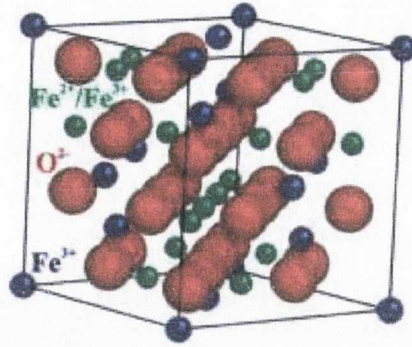


Figure 3.3: Crystal structure of Fe_3O_4 . The A-sites are in blue and the B-sites are in green. Red is oxygen. The Fe-O distances for the Fe A site ions is 1.876 \AA and for the B site ions is 2.066 \AA [7].

metry, electrical conductivity and magnetization occurs [9]. This transition is called the Verwey transition [10].

These properties make Fe_3O_4 an extremely attractive potential candidate as a spin injector source in spintronic devices and hence is the spin injector material of choice in this section.

3.2 Magnetite on differently doped Gallium Arsenide substrates

3.2.1 Introduction to the Experiment

Transport through the magnetite / gallium arsenide interface was studied for four different doping types, mid n and p and high n and p. The Fe_3O_4 thin films were grown by reactively sputtering from a pure Fe target in the Leybold sputtering system, described in the previous chapter. The substrates were heated to $400 \text{ }^\circ\text{C}$ and the partial pressures during deposition for Ar and O_2 were $3 \times 10^{-3} \text{ mbar}$ and $4 \times 10^{-5} \text{ mbar}$ respectively. Gold top contacts were also sputtered using this system. The bare substrate wafers were packed in an inert atmosphere and placed immediately into the chamber once removed

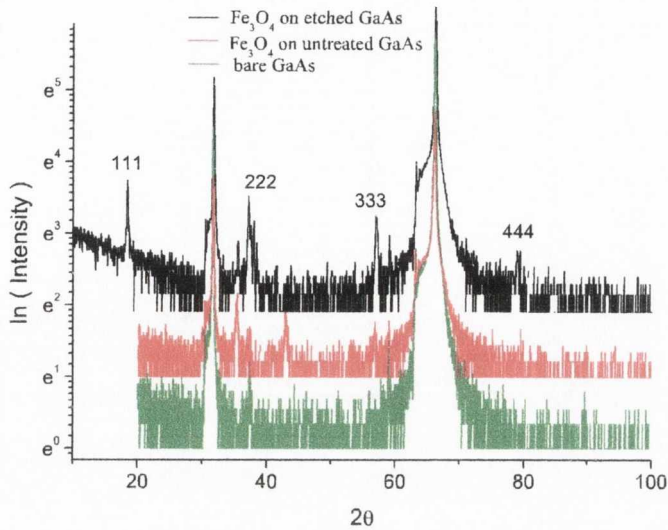


Figure 3.4: XRD scans on bare GaAs substrates and on treated and untreated GaAs. Film and substrate peaks are present in the scan.

from packaging, thereby eliminating any need to etch. In any situation where the GaAs substrates needed etching a 10% HCl solution was used to remove the native oxide. AuGe, approx 88% Au and 12% Ge, was thermally evaporated onto the back side of the GaAs substrates. After annealing briefly in air at 300 °C this formed an ohmic contact to the GaAs. The junction sizes in this case was typically 40 mm².

3.2.2 Fe₃O₄ Film Structure on GaAs (001) Substrates

Before carrying out transport measurements it is important to ensure that good quality Fe₃O₄ films can be grown on GaAs substrates. X-ray diffraction analysis was performed on three different GaAs substrates all orientated in the (001) direction. It can be seen from figure 3.4 that magnetite grows preferentially in the (111) direction when the native oxide has been removed.

X-ray reflectivity scans revealed Fe₃O₄ thickness to be 60 nm.

3.2.3 Verwey Transition

The Verwey transition is a transition that occurs in magnetite around 120 K. The conductivity abruptly decreases by about two orders of magnitude, the symmetry of the crystal structure changes and there is a decrease in the magnetization. Verwey first observed this change and proposed that the transition is caused by the ordering of the Fe^{2+} ions on the B sub-lattice, resulting in the formation of charged (100) planes occupied by alternating Fe^{3+} and Fe^{2+} B site ions [7] & [10].

The Verwey transition was observed by two different methods. The first used the Superconducting Quantum Interface Device magnetometer to measure the magnetization of the films as a function of temperature in an constant field of 50 mT. The graph of this is shown in the left inset in figure 3.5. The main graph in figure 3.5 is the magnetization versus field data, confirming the ferromagnetic nature of the magnetite films before and after the Verwey transition.

Another method of detecting the presence of the Verwey transition is from resistance versus temperature data. The resistance of stoichiometric magnetite increases steeply below 120 K. The graph is in figure 3.6. The transition is not observed as sharply here as it was in figure 3.5 so the resistance of Fe_3O_4 films grown on MgO and SrTiO_3 substrates are included for comparison. These substrates were originally used to parametrize the growth of good quality Fe_3O_4 films in the Leybold system. They were chosen because of the good lattice match between them and Fe_3O_4 , only $\sim 0.3\%$ between MgO and Fe_3O_4 [11], means that good quality films can be achieved once grown in the right conditions. This was achieved using a substrate temperature during deposition of 300 °C, however in order to obtain good crystalline quality with a more extreme lattice mismatch, around 5 % between GaAs and Fe_3O_4 [12], it was necessary to increase substrate deposition temperature to 400 °C. Even then it can be observed in figure 3.6 that the best quality films are grown on the MgO substrate.

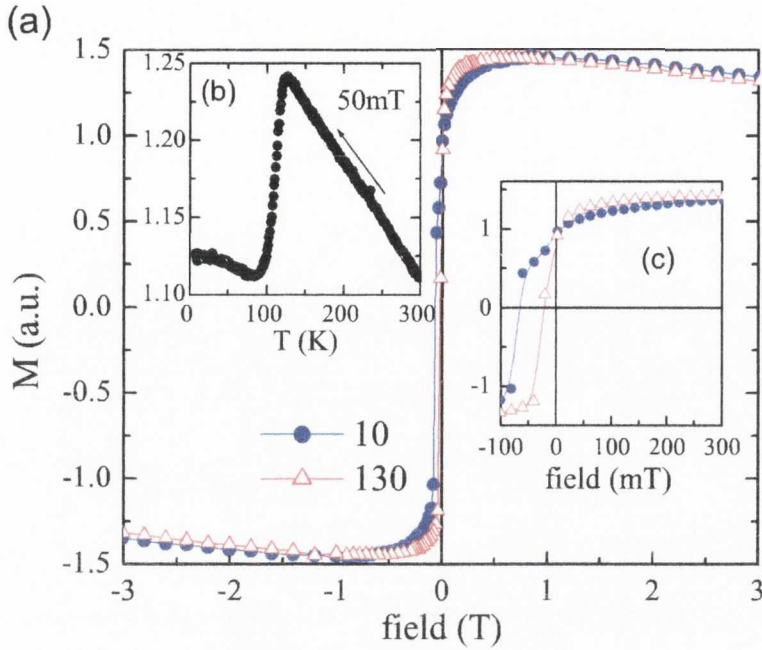


Figure 3.5: Part (a) shows magnetization vs field at 130 K and 10 K taken in a one directional field sweep from +3 T to -3 T only. The left inset (b) shows magnetization vs temperature in a field of 50 mT, which shows the Verwey transition in magnetite. The right inset (c) shows a close up around 0 T.

3.2.4 Electrical Transport

The carrier concentrations of the GaAs substrates were determined by measuring the Hall effect, using the van der Pauw method at room temperature. They were $7.7 \times 10^{17} \text{ cm}^{-3}$ for the mid n-type, $1.0 \times 10^{18} \text{ cm}^{-3}$ for the mid p-type, $3.5 \times 10^{18} \text{ cm}^{-3}$ for the high n-type and $3.4 \times 10^{18} \text{ cm}^{-3}$ for the high p-type.

The temperature-dependent I-V measurements were conducted in a closed-cycle helium refrigerator system, the resistivity rig described earlier. The error in the measured currents is $\pm 0.1 \text{ nA}$. Figure 3.7 shows the $I - V$ curves for magnetite on the four different GaAs substrates at 50 K intervals between 50 K and 300 K (room temperature). For the n- and p-type medium doped samples the data is asymmetric indicating a diode like behaviour that is typical of Schottky barriers. The medium doped n-type substrate has

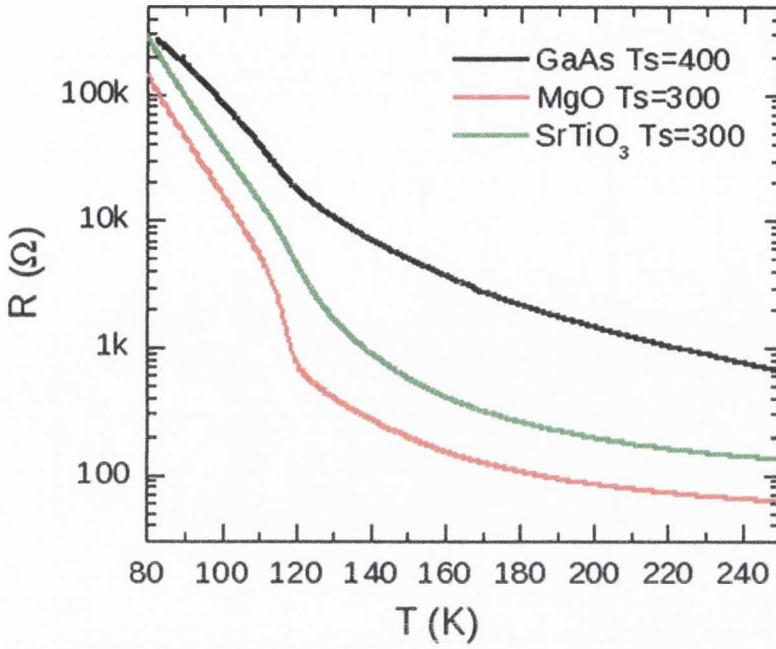


Figure 3.6: R vs T of magnetite thin films grown on GaAs, MgO and SrTiO₃ substrates.

the lowest doping concentration and consequently the leakage current in reverse bias is the lowest for this sample. The higher doped substrates show nearly ohmic characteristics at room temperature but deviate significantly from this linearity at lower temperatures.

Focusing first on the lower doped substrates, transport across the Fe₃O₄ / GaAs interface is through a Schottky barrier and so is dominated by thermionic emission / diffusion at elevated temperatures. In the thermionic emission / diffusion model [13] & [14], the dependence of the current on bias voltage can be expressed as,

$$I = I_S \left(e^{\frac{qV}{nkT}} - 1 \right) \quad (3.1)$$

where,

$$I_S = A_e A^{**} T^2 e^{-\frac{q\phi_B}{kT}} \quad (3.2)$$

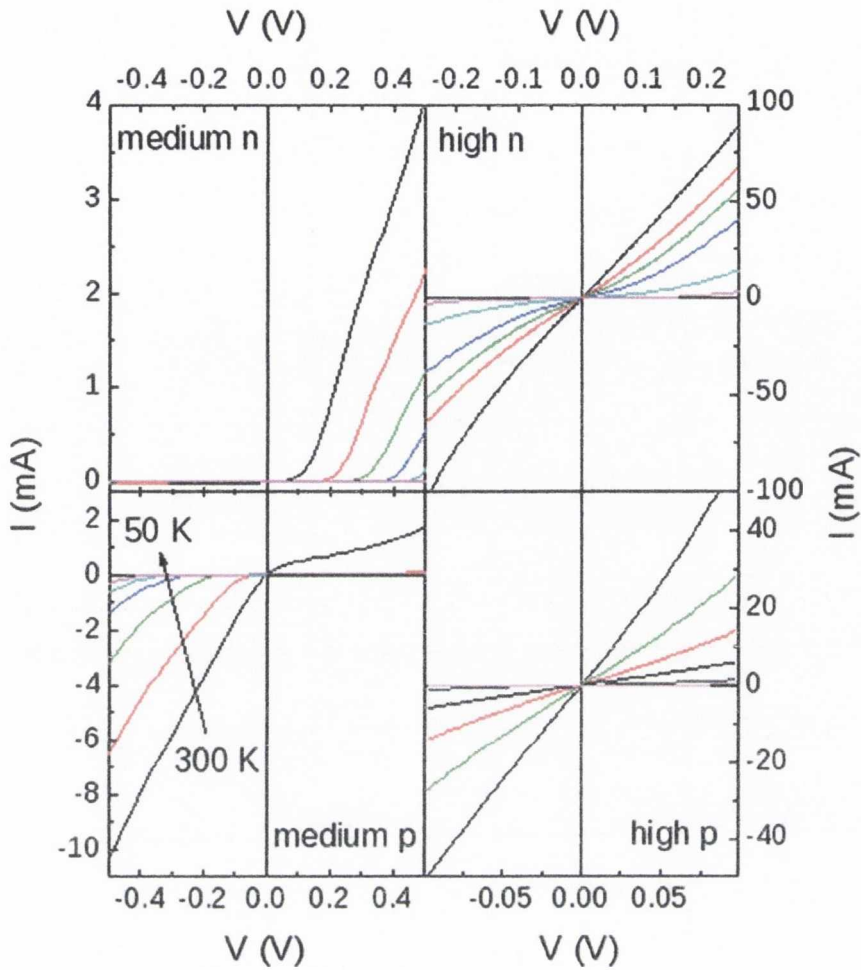


Figure 3.7: I vs V as a function of temperature for magnetite on the four different GaAs (001) substrates. Current measurements have an error of ± 0.1 nA.

A_e is the active area, A^{**} is the effective Richardson constant, ϕ_B is the Schottky barrier height and n is the ideality factor. The theory behind equation 3.1 has been discussed in detail in the first chapter. Differentiating and taking the natural logarithm of equation 3.1 results in,

$$\ln \left(\frac{dI}{dV} \right) = \ln \left(\frac{I_s q}{nkT} \right) + \frac{q}{nkT} V \tag{3.3}$$

$$\begin{matrix} \downarrow & & \downarrow & & \downarrow \\ y & = & c & + & mx \end{matrix}$$

Thus the slope of the straight line fitted to the data plotted as $\ln(dI/dV)$ versus V in the initial forward bias region will give the ideality factor directly and the intercept can be used to calculate the Schottky barrier height. Part (a) of figure 3.8 shows the data for the medium-doped samples after numerical differentiation, plotted in this way.

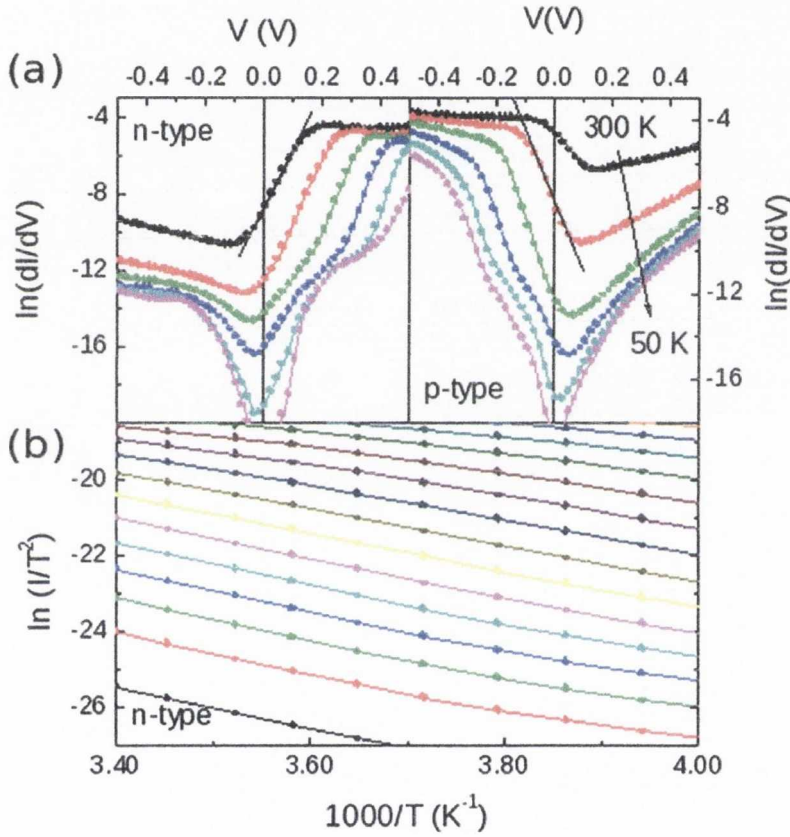


Figure 3.8: Graph of (a) $\ln(dI/dV)$ vs V at 50 K intervals for the medium n- and p-type GaAs substrates, (b) $\ln(I/T^2)$ vs V , an activation energy plot, of the mid n-type sample around room temperature.

For the medium-doped n-type substrate the data for $T > 230$ K can be fitted between zero bias and a forward bias of about 0.2 V, above which the current saturates due to series resistance. Near room temperature an ideality factor, n , of 1.3 and a Schottky barrier

height, ϕ_B , of 0.63 eV are obtained. To determine ϕ_B , we used the total area of the sample (approximately 40 mm²) and an effective Richardson constant of 8.2 Acm⁻²K⁻² [13] in equation 3.2. Alternatively, the Schottky barrier height can also be obtained from an activation energy plot. In this case it is not necessary to specify A_e and A^{**} , which is an advantage for large junction areas. The following expression is used [13],

$$\ln \left(\frac{I}{T^2} \right) = \ln (A_e A^{**}) - \frac{q (\phi_B - \frac{V}{n})}{kT} \quad (3.4)$$

The activation energy plots for different forward biases near room temperature are shown in part (b) of figure 3.8. From the slope of the high temperature data (260 < T < 300) and n as 1.3 we obtain ϕ_B equal to 0.58 eV, which is in rather good agreement with the result in the previous analysis. A comparison of these results is clearly shown in table 3.1

For the medium-doped p-type substrate a series resistance limits the current in forward bias at high temperature. Between 200 K and 250 K, however, the Schottky barrier resistance dominates the series resistance. Thermionic emission / diffusion analysis in this temperature range yields n equal to 1.3 and ϕ_B equal to 0.51 eV. To fit the data to equation 3.4 an even lower temperature region had to be used, 160 K ≤ T ≤ 210 K. This activation energy plot can be seen in figure 3.9. From the slope of this plot and using n as 1.3, ϕ_B was calculated as 0.49 eV, which again is in good agreement with the previous analysis.

The n- and p-type GaAs substrates with higher doping concentrations exhibit similar IV characteristics that are nearly symmetric with voltage and clearly nonlinear at lower temperatures. In this case, carrier transport across the Fe₃O₄ / GaAs interface is dominated by tunneling of electrons or holes through the Schottky barrier. The data can be analyzed within the thermionic field emission model of Padovani and Stratton [15]. In this model the IV dependence is expressed as,

$$I = I_S e^{\frac{qV}{E_0}} \quad (3.5)$$

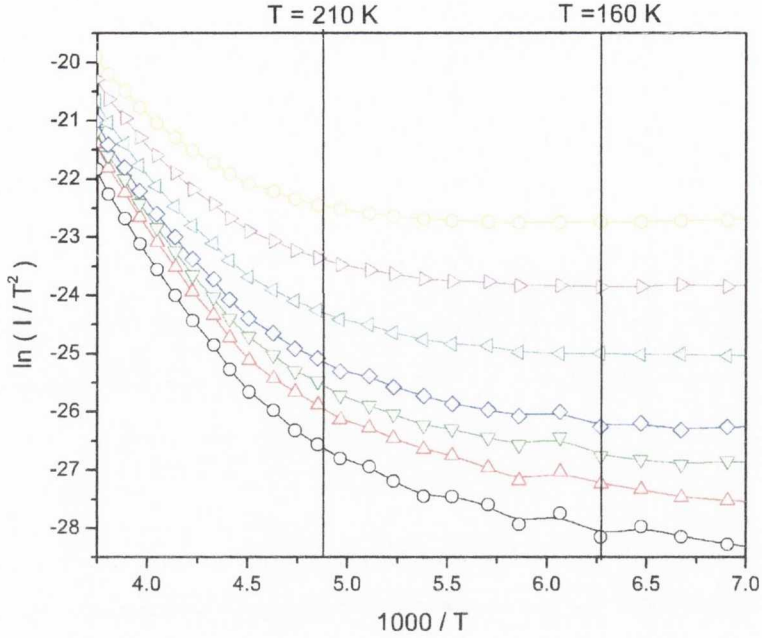


Figure 3.9: Activation energy plot of Fe_3O_4 / mid p-type GaAs. The curves represent measurements for different forward bias voltages.

where I_S is the saturation current and E_0 is an energy term that depends on bias voltage and temperature. For an intermediate temperature regime in which thermionic field emission dominates, I_S and E_0 are given by,

$$I_S = \frac{A_e A^{**} \sqrt{\pi F_{00} (\phi_B - qV + F_{fsc})} \exp\left(\frac{E_{fsc}}{kT} - \frac{\phi_B + E_{fsc}}{E_0}\right)}{kT \cosh\left(\frac{E_{00}}{kT}\right)} \quad (3.6)$$

where,

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT}\right) \quad (3.7)$$

and

$$E_{00} = \frac{q\hbar}{4} \sqrt{\frac{N}{\epsilon m^*}} \quad (3.8)$$

The semiconductor is assumed to have an impurity concentration, N , that is independent of temperature, E_{fsc} is the Fermi level of the semiconductor, ϵ is permittivity and m^* is the effective mass. Similar expressions have been derived for reverse bias voltages [15]. At low temperatures, field emission dominates transport across the metal / semiconductor interface and $E_0 = E_{00}$. The IV characteristics of the n- and p-type GaAs substrates with high doping concentrations were fitted with,

$$V = F_0 (\ln I - \ln I_S) + IR_S \quad (3.9)$$

where R_S is introduced to account for a series resistance. The results are shown in figure 3.10 together with the theoretical predictions for I_S and E_0 for a forward-biased n-type substrate with $n = 3.5 \times 10^{18} \text{ cm}^{-3}$ (based on textbook parameters for GaAs [13]). The experimentally determined value for I_S is of the same order of magnitude as the calculated ones. Whereas the predicted value of E_0 shows only minor temperature dependence, the temperature dependence of the calculated and experimentally determined value of I_S are qualitatively similar above 80 K. This confirms that transport across the Fe_3O_4 / GaAs interface is dominated by thermionic field emission for the higher-doped substrates.

The series resistance R_S of the Fe_3O_4 / GaAs structures increases with decreasing temperature. This effect, which is most pronounced for the p-type substrate, is due to the temperature dependence of the Fe_3O_4 layer and GaAs substrate resistances. While the resistance of the Fe_3O_4 layer increases with decreasing temperature, the variation of the GaAs resistance can either be positive or negative depending on the doping level [13]. In addition, the Fe_3O_4 layer can also contribute to the non-linearity in the IV curves at low temperatures. Current out-of-plane measurements on Au / Fe_3O_4 / Au trilayer structures reveal a nonlinear IV dependence below the Verwey transition [16]. This effect is most likely due to the opening of a gap in the minority spin band below 120 K, which creates an additional transport barrier at the Au / Fe_3O_4 interface.

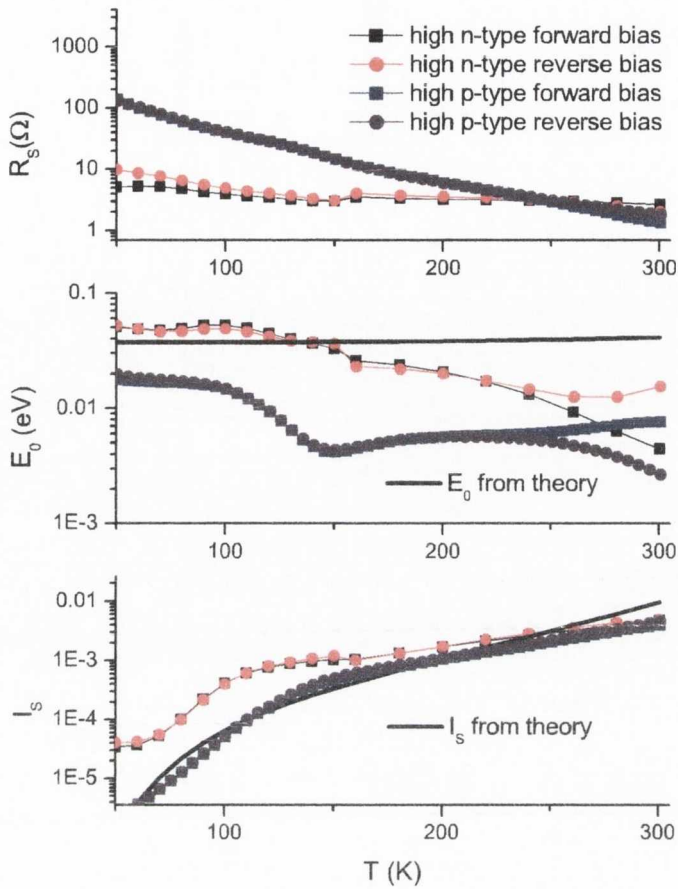


Figure 3.10: Temperature dependence of R_S , E_0 , and I_S . These data were extracted by fitting the experimental data of the n- and p-type GaAs substrates with high carrier concentration to equation 3.9 ($V_{bias} = 10$ mV). The solid black line represents a calculation for the n-type substrate with a high carrier concentration of $3.5 \times 10^{18} \text{ cm}^{-3}$ at a forward bias of 10 mV.

3.3 Magnetite on mid n-type Silicon substrates of different orientations

3.3.1 Introduction to the Experiment

The Fe_3O_4 films were deposited onto silicon substrates orientated in the (001) and (111) directions by reactive dc magnetron sputtering from a pure Fe target at 400 °C in the same Leybold system as before. The Fe target was sputtered at a constant power of 52

W under partial Ar and O₂ pressures of 3×10^{-3} mbar and 4×10^{-5} mbar, respectively. The deposition rate under these growth conditions was about 8 nm/min. The substrates were etched for three minutes using hydrofluoric acid prior to loading into the vacuum deposition system in order to remove a thermally grown 25 nm layer of SiO₂. The carrier concentration and resistivity of the silicon substrates were once more determined by room temperature Hall effect and resistance measurements. The result yielded $n = 1.8 \times 10^{14}$ cm⁻³ ($\rho = 22.4 \Omega\text{cm}$) and $n = 1.7 \times 10^{15}$ cm⁻³ ($\rho = 2.3 \Omega\text{cm}$) for the Si(111) and Si(001) substrates, respectively. For the $I - V$ measurements, the silicon substrates were cut into 6 mm square samples. An ohmic contact was made to the back of the silicon by indium soldering at 450 °C for one minute. To form the top contact an Au layer was sputtered onto the magnetite film using the same magnetron deposition system used to grow the magnetite.

3.3.2 Fe₃O₄ film structure on Si substrates

Figure 3.11 shows x-ray $\theta - 2\theta$ scans for 60 nm thick Fe₃O₄ films on Si(111) and Si(001) substrates. These measurements clearly reveal that magnetite grows with a (111) orientation normal to the film plane irrespective of the substrate orientation. Reflections from other crystalline orientations or other iron oxide phases do not appear in the x-ray scans. The full width at half maximum (FWHM) of the rocking curve for the Fe₃O₄ (111) reflection is about 2.5° , which is larger than the width of the rocking curves for the silicon substrate reflections ($\approx 0.5^\circ$). This indicates a distribution in the orientational quality of the Fe₃O₄ films on the Si(111) and Si(001) substrates. The results obtained here for Fe₃O₄ grown on the Si(001) substrate agree with diffraction data of magnetite films prepared by pulsed laser ablation by Kennedy and Stampe [17].

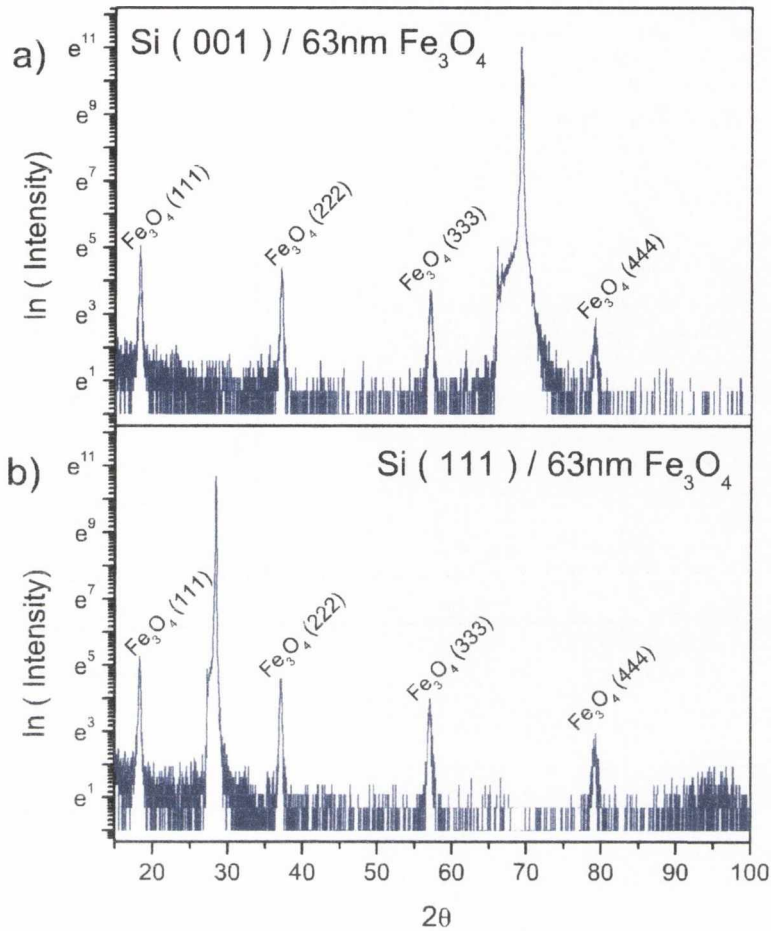


Figure 3.11: $\theta - 2\theta$ XRD scans for 60 nm thick Fe_3O_4 films on Si(111) and Si(001) substrates.

3.3.3 Magnetic Properties of the films

Figure 3.12 shows SQUID magnetization curves for the 60 nm thick Fe_3O_4 films at 300 K. The films exhibit a similar coercive field of 30 mT and a remanence ratio of about 70%. The saturation magnetization at 300 K is $4.0 \times 10^5 \text{ Am}^{-1}$ for Fe_3O_4 and $3.9 \times 10^5 \text{ Am}^{-1}$ for the Fe_3O_4 grown on the Si(111) and Si(001) substrates respectively, which is somewhat smaller than the reported bulk value of $4.7 \times 10^5 \text{ Am}^{-1}$. However, the saturation magnetization of the Fe_3O_4 films on Si(111) and Si(001) is well within the range of reported

values ($3.0 \times 10^5 - 4.4 \times 10^5 \text{ Am}^{-1}$) for thin magnetite films on $\text{MgO}(001)$ and $\text{SrTiO}_3(001)$ substrates [19] - [18].

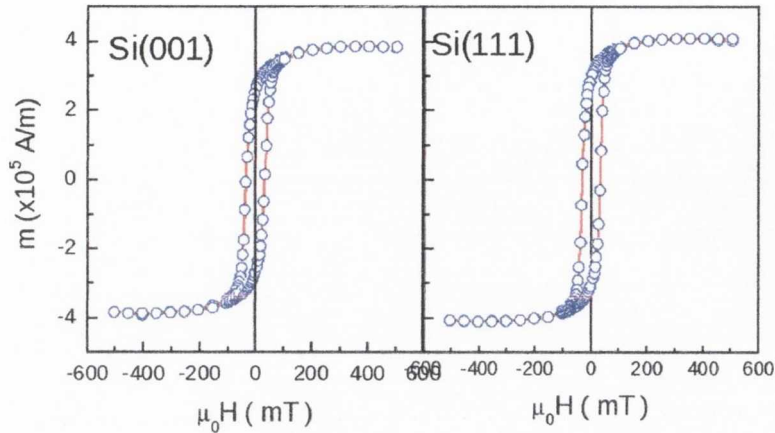


Figure 3.12: Room temperature magnetization curves for 60 nm Fe_3O_4 / $\text{Si}(111)$ and Fe_3O_4 / $\text{Si}(001)$.

Figure 3.13 shows the temperature dependence of the sample magnetization for the Fe_3O_4 films on $\text{Si}(111)$ and $\text{Si}(001)$. The data were measured during cooling in an applied magnetic field of 200 mT, which is enough to saturate the film magnetization. Initially the magnetization increases with decreasing temperature. For the Fe_3O_4 film on $\text{Si}(111)$ the magnetization suddenly drops at 120 K and for the Fe_3O_4 film on $\text{Si}(001)$ a similar although slightly smaller decrease is measured at 108 K. As previously stated and described this step in the film magnetization is characteristic of the Verwey transition in Fe_3O_4 . The change in saturation magnetization is slightly smaller for the Fe_3O_4 film on $\text{Si}(001)$ and the transition is shifted to a somewhat lower temperature. This phenomenon, which is common for thin Fe_3O_4 films [18]- [26], has been attributed to epitaxial stress [20], strong structural coupling between film and substrate [23], and a film thickness dependence on the size of antiphase domains [26]. The observation of a clear Verwey transition in the Fe_3O_4 / $\text{Si}(111)$ and Fe_3O_4 / $\text{Si}(001)$ structures is, as stated before, a good indication of high quality Fe_3O_4 film growth.

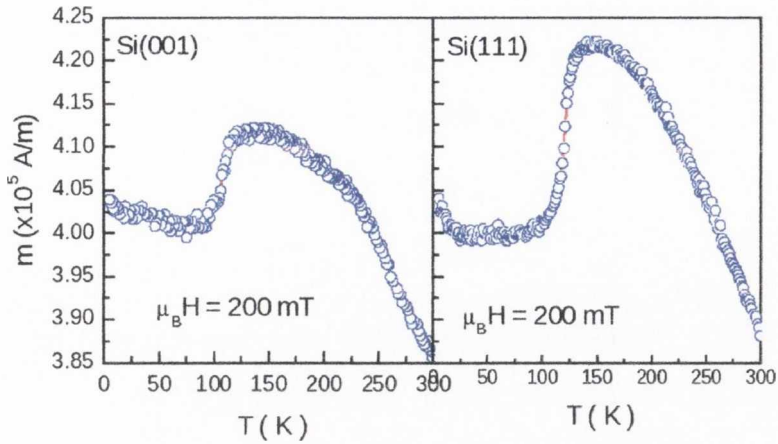


Figure 3.13: Temperature dependence of the film magnetization for 60 nm Fe_3O_4 / Si(111) and Fe_3O_4 / Si(001). The data was collected during cooling in an applied magnetic field of 200 mT.

3.3.4 Electrical Transport

Figure 3.14 shows the $I - V$ measurements for the Fe_3O_4 on Si(111) at 25 K intervals between 75 K and 300 K. Based on the shape of the $I - V$ curves, three distinct regimes can be identified. At low temperatures ($T \leq 150$ K) the $I - V$ curves are quite symmetric at low bias, the curves are fully asymmetric at intermediate temperatures ($175 \text{ K} \leq T \leq 225$ K) and at high temperatures ($T \geq 250$ K) the asymmetry between forward and reverse bias is reduced.

The transport measurements in the intermediate temperature regime show a rectifying behaviour that is characteristic for thermionic emission / diffusion across a Schottky barrier. So again the dependence of the current on forward bias for $V > \frac{3kT}{q}$ can be fitted by the thermionic emission / diffusion model given by equations 3.1 and 3.3. Since the data in the right panels of figure 3.14 are plotted as $\ln(dI/dV)$ vs V , the slope of the curve for forward bias can be used to determine the ideality factor and the intercept can be used to calculate the Schottky barrier height just as before. For $175 \text{ K} \leq T \leq 225$ K, fitting the data and using $A_e = 36 \text{ mm}^2$ and $A^{**} = 110 \text{ Acm}^{-2}\text{K}^{-2}$ yields a barrier height

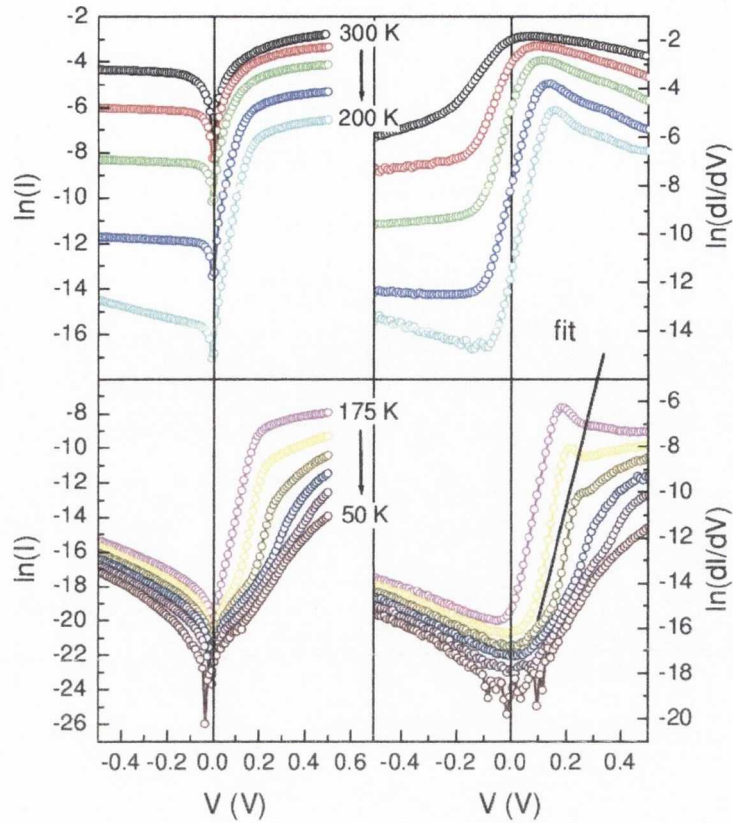


Figure 3.14: $I - V$ measurements for $\text{Fe}_3\text{O}_4 / \text{Si}(111)$. The graphs represent measurements in 25 K temperature intervals. $\ln(I)$ values below -23 can not be trusted as these values are below the accuracy of the Keithly multimeter, ± 0.1 nA. The solid line indicates a fit to the data that can be used to determine the Schottky barrier height and the ideality factor.

of 0.51 eV and an ideality factor of 1.06.

An alternative way to determine the Schottky barrier height is by using an activation energy plot [13] also as discussed earlier. In this case it is not necessary to specify A_e and A^{**} , which is an advantage for large Schottky junctions in which the active area may be considerably smaller than the contact area between the (half-)metal and the semiconductor. Figure 3.15 is an activation energy plot for the $\text{Fe}_3\text{O}_4 / \text{Si}(111)$ structure. The data was fitted for temperature region of $175 \text{ K} \leq T \leq 225 \text{ K}$ (indicated by the vertical lines in figure 3.15) using equation 3.4. The slope of the graph for $V = 0.114 \text{ V}$ in figure 3.15 yields a Schottky barrier height of 0.52 eV, which is very similar to the result from the $I - V$ analysis. This indicates that transport across the $\text{Fe}_3\text{O}_4 / \text{Si}(111)$ junction

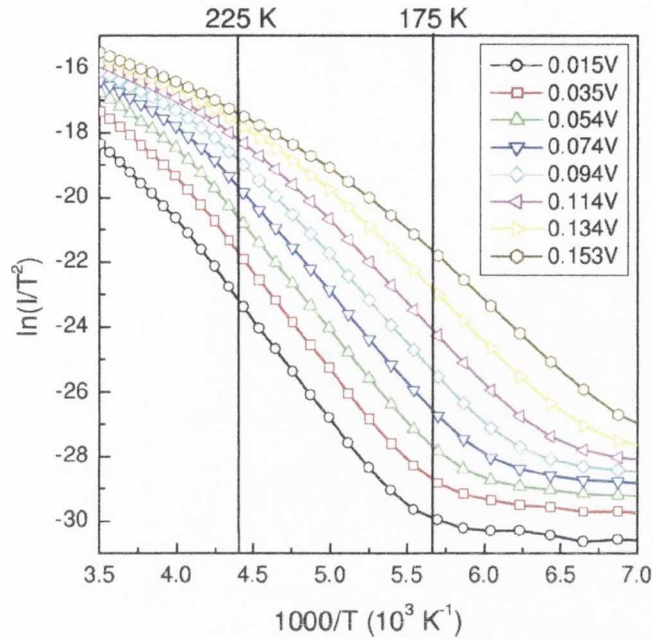


Figure 3.15: Activation energy plots for $\text{Fe}_3\text{O}_4 / \text{Si}(111)$. The graphs represent measurements for different forward bias voltages.

is rather homogeneous, i.e., the effective area is similar to the actual contact area.

The current for reverse bias voltages is predominantly due to leakage through the $\text{Fe}_3\text{O}_4 / \text{Si}(111)$ junction. The magnitude of this reverse current depends on the parameters such as the Schottky barrier height, the carrier concentration of the silicon substrate and temperature (see figure 3.14). The thermionic emission / diffusion model, equation 3.1 predicts an exponential increase with temperature for the forward current as well. However, the forward current is limited at elevated temperatures by a series resistance from the silicon substrate. This series resistance reduces the asymmetry in the $I - V$ curves in the high temperature regime ($T \geq 250 \text{ K}$).

In the low temperature regime ($T \leq 150 \text{ K}$) the $I - V$ becomes more symmetric at low bias. At these temperatures thermally activated transport across the $\text{Fe}_3\text{O}_4 / \text{Si}(111)$ interface becomes negligible and quantum-mechanical tunneling of electrons through the barrier starts to dominate. The transition between these two transport mechanisms is also

clearly observed in the bias dependence of the forward current. At $T = 125$ K, for example, the current is due to tunneling up to a bias of 0.15 V, above which the current suddenly increases due to the onset of thermally activated electron emission. This transition point shifts to higher forward bias with decreasing temperature.

Figure 3.16 shows $I - V$ measurements for $\text{Fe}_3\text{O}_4 / \text{Si}(001)$ at 25 K intervals between 125 K and 300 K. Again, quantum-mechanical tunneling of electrons from the semiconductor into the half-metal is the dominant transport mechanism at low temperatures. However, since the carrier concentration of the $\text{Si}(001)$ substrate is about one order of magnitude larger than that of the $\text{Si}(111)$ substrate it prevails up to higher temperatures (the tunneling current increases exponentially with the square root of the doping concentration). Fitting the data for $T \leq 250$ K with the thermionic emission / diffusion model yields an ideality factor of about 1.07 and a Schottky barrier height of 0.65 eV. This agrees with the estimated Schottky barrier height obtained from the slope of the activation energy plot, figure 3.17, for $V = 0.1$ V, giving $\phi_B = 0.65$ eV.

3.3.5 Interface properties

Although the crystalline texture and magnetic properties of the $\text{Fe}_3\text{O}_4 / \text{Si}(111)$ and $\text{Fe}_3\text{O}_4 / \text{Si}(001)$ structures are very similar, the height of the barrier that is formed during Fe_3O_4 film growth is significantly different. One of the possible and most likely explanations for such dissimilar Schottky barriers is the formation of different oxide or silicide interfacial layers. To confirm this high resolution tunnelling electron microscopy (HRTEM) analysis was performed along the $\langle 110 \rangle$ Si zone axis for atomic structure characterization. All TEM, HRTEM and HAADF images were done by Ana M. Sánchez in Departamento de Ciencia de los Materiales e IM y QI, Universidad de Cádiz, Spain.

Figure 3.18 shows the low magnification conventional TEM and HRTEM images performed on the $\text{Fe}_3\text{O}_4 / \text{Si}(111)$ interface. The panel to the right of part (a) in figure 3.18 is a digitally compressed image, the lateral dimension is scaled by a factor of 10 for

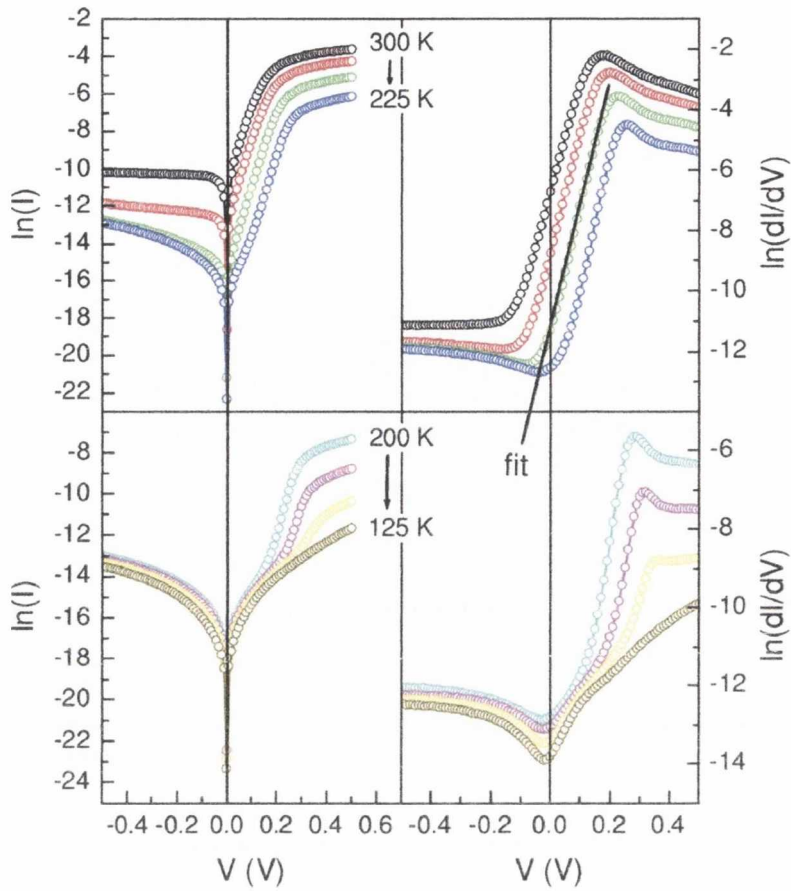


Figure 3.16: $I - V$ measurements for $\text{Fe}_3\text{O}_4 / \text{Si}(001)$. The graphs represent measurements in 25 K temperature intervals. Again $\ln(I)$ below -23 is within the error of multimeter used and can not be trusted. The solid line indicates a fit to the data that can be used to determine the Schottky barrier height and the ideality factor.

a better illustration of the interface roughness. These images clearly indicate that the 60 nm thick Fe_3O_4 film forms a smooth interface with the $\text{Si}(111)$ substrate but that the $\text{Fe}_3\text{O}_4 / \text{Au}$ interface is considerably rougher. The TEM analysis also confirms the growth of a crystalline Fe_3O_4 film with a preferred (111) orientation perpendicular to the film plane. It is important to note the presence of an interfacial bilayer separating the high quality Fe_3O_4 film and the $\text{Si}(111)$ substrate. This bilayer consists of an approximately 5 nm thick crystalline film (dark contrast) whose lattice is distorted and an amorphous layer (light contrast) with a thickness of 2 nm.

High angle annular dark field (HAADF) analysis was also done on this sample, as

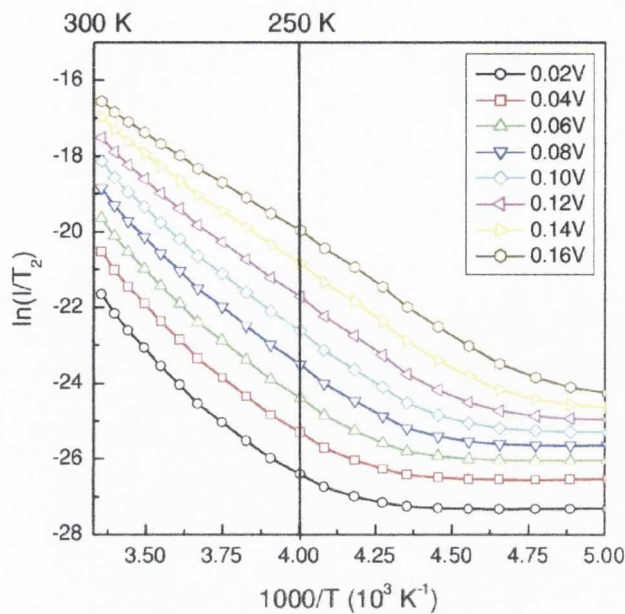


Figure 3.17: Activation energy plots for $\text{Fe}_3\text{O}_4 / \text{Si}(001)$. The graphs represent measurements for different forward bias voltages.

shown in 3.19. The dark contrast layer appears bright in this image. This suggests the formation of a crystalline iron silicide during the initial stages of growth, since the intensity of HAADF images is related to the atomic number Z . Iron silicide also forms when an Fe layer is non-reactively deposited onto a silicon substrate or when an Fe layer is annealed at elevated temperatures [27]. Different silicide interface layers have been identified for this type of system. The most common are Fe_3Si , FeSi and FeSi_2 , which form at different growth and annealing temperatures. For the samples grown here, where the Fe target was reactively sputtered in O_2 and deposited on a substrate at 400°C , it is most likely that the interface layer is either Fe_3Si and / or FeSi as FeSi_2 only forms at higher temperatures. The second interface layer having a bright contrast in the TEM images appear to be dark in the HAADF image, figure 3.19. From this it can be concluded that the 2 nm thick amorphous layer is an oxide that covers the iron silicide.

Figure 3.20 shows the low magnification conventional TEM and HRTEM images pre-formed on the $\text{Fe}_3\text{O}_4 / \text{Si}(001)$ interface along the $\langle 110 \rangle$ zone axis. Again an interface

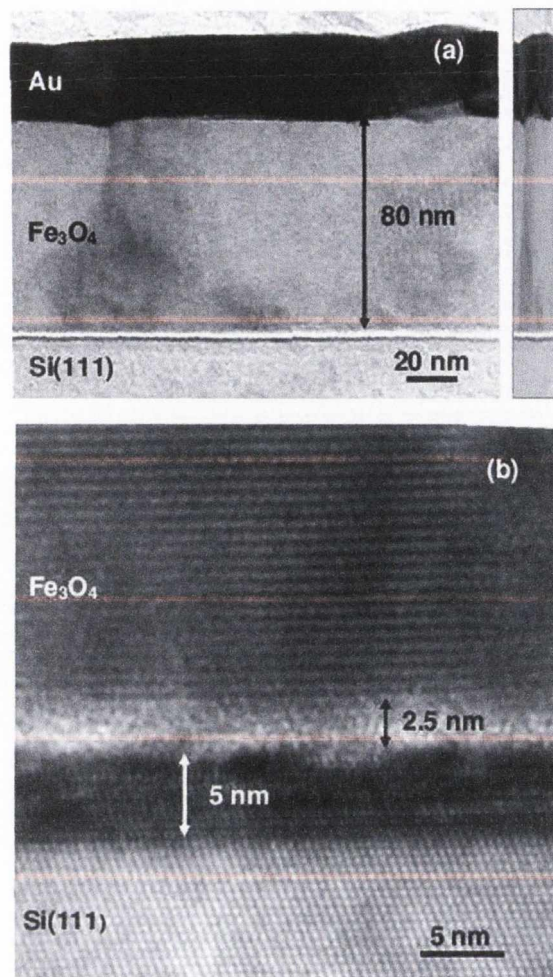


Figure 3.18: (a) Low magnification TEM and (b) HRTEM images of an Fe_3O_4 film on Si(111). The image in the upper right panel is compressed by a factor of 10 in the lateral direction. The arrows indicate the two distinctive interface layers that separate the Fe_3O_4 film and the silicon substrate.

bilayer separates the Fe_3O_4 film and silicon substrate. This time, however, the iron silicide layer is very thin, only one or two atomic layers thick, and the amorphous oxide is considerably thicker than that of the Fe_3O_4 / Si(111) samples. It is approximately 6 nm thick this time.

This difference between the interface structure is the most likely cause for the different Schottky barrier heights on the Si(111) and Si(001) substrates. While the relatively thick iron silicide interface layer on the Si(111) forms a barrier height of 0.52 eV the layer

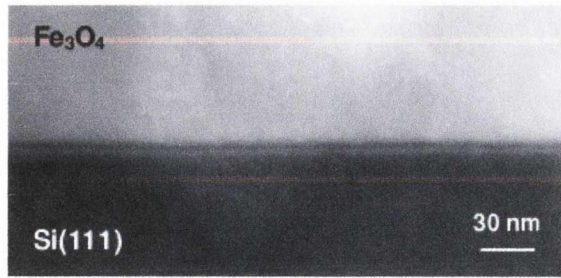


Figure 3.19: HAADF image of the same Fe₃O₄ / Si(111) sample in figure 3.18. The contrast in this image is proportional to the atomic number of the film material.

is too thin to form a similar barrier on the Si(001) substrate. Instead the amorphous oxide interface layer predominantly determines the Schottky barrier height of the Fe₃O₄ / Si(001) sample, giving a considerably higher barrier height of 0.65 eV. The formation of an amorphous interface layer on both orientations of silicon explain why texture and structure of the Fe₃O₄ films is so similar in the two systems. The films consist of grains with (111) texture normal to the film plane and a variety of in-plane crystal orientations, illustrated by the contrasts in figures 3.18 and 3.20.

SQUID magnetization measurements on Fe₃O₄ of varying thicknesses were done in order to obtain information on the magnetic properties of the interface layer. Figure 3.21 shows the saturation moment per sample area for different Fe₃O₄ layers on Si(111). Fitting the data for film thicknesses of 20 nm and greater give a film magnetization of 3.9×10^5 A/m, which agrees well with the SQUID magnetization curves of figure 3.12. However, for the thinner Fe₃O₄ films the saturation magnetization is smaller but not zero. From this and the TEM images it is concluded that the Fe silicide layer at the interface exhibits a magnetic moment at room temperature. As Fe(Si_{1-x}Fe_x) films are only magnetic when $x \geq 0.15$ [28], basically when the Fe content is 35 % larger than the Si content, the interfacial iron silicide layer is most likely to be magnetic Fe₃Si, which has a Currie temperature of 840 K [29].

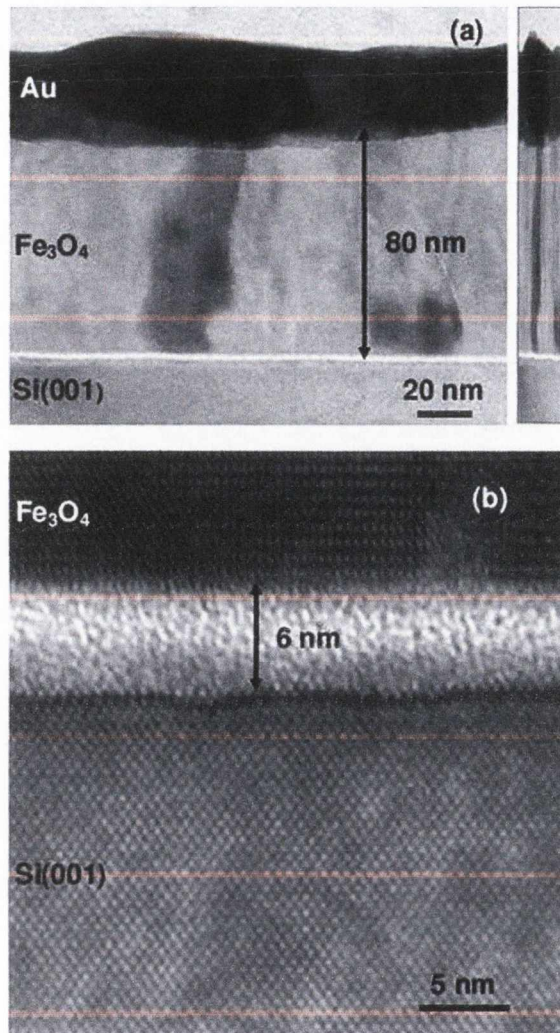


Figure 3.20: (a) Low magnification TEM and (b) HRTEM images of an Fe₃O₄ film on Si(001). The image in the upper right panel is again compressed by a factor of 10 in the lateral direction. The arrow indicates the amorphous oxide layer that separates the Fe₃O₄ film and the silicon substrate. The dark contrast silicide layer is very thin in this sample and can't be seen at all in part (a)

3.4 Conclusions and Summary

Reactive sputtering of Fe₃O₄ results in (111) orientated films on all the GaAs(001) substrates and on both the Si(111) and Si(001) substrates. All these films exhibit a clear Verwey transition which manifests itself by a reduction of the saturation magnetization around 120 K.

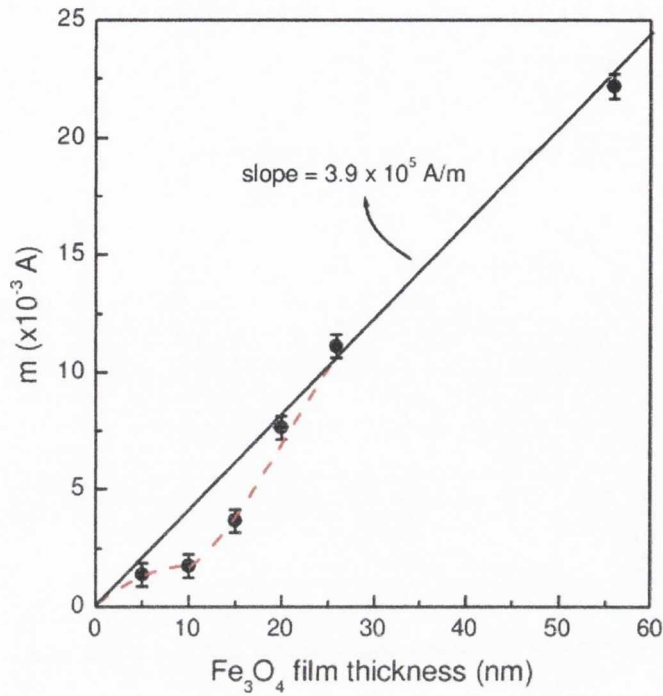


Figure 3.21: Magnetic moment per sample area for $\text{Fe}_3\text{O}_4 / \text{Si}(111)$ as a function of Fe_3O_4 film thickness. The solid line is a fit through the data points for 20 nm and thicker Fe_3O_4 films

For the $\text{Fe}_3\text{O}_4 / \text{GaAs}$ interfaces, different transport mechanisms have been identified. For n- and p-type GaAs substrates with medium doping concentrations we measured a rectifying behavior that is characteristic for thermionic emission / diffusion across a Schottky barrier. It is important to state at this point that forward and reverse bias are **not the same** as positive and negative bias. Fits to the data reveal n is 1.3 and ϕ_B is 0.58 eV and 0.63 eV for the n-type GaAs substrate with a carrier concentration of $7.7 \times 10^{17} \text{ cm}^{-3}$. For the p-type substrate with a carrier concentration of $1.0 \times 10^{18} \text{ cm}^{-3}$, n is 1.3 and ϕ_B is 0.51 eV and 0.49 eV. This work demonstrated for the first time that it is possible to form a high quality Schottky barrier at the interface of the half-metallic hopping conductor Fe_3O_4 and GaAs. For higher doping concentrations ($n, p \approx 3.5 \times 10^{18} \text{ cm}^{-3}$), transport across the $\text{Fe}_3\text{O}_4 / \text{GaAs}$ interface is dominated by thermionic field emission. In this case, electrons and holes tunnel through the Schottky barrier and this results in nonlinear but nearly symmetric $I - V$ curves. Our data show that different

transport modes between a half-metal and a semiconductor could be selected by careful selection of semiconductor doping profile. This is promising for the application of Fe_3O_4 as a spin-polarized source, which is expected to further enhance the polarization of the current in spin injection experiments. However no TEM analysis was available for the GaAs structures and there is a possibility of some similar types of interfacial layers being formed during film growth as the ones seen in the Si structures.

The transport measurements in the Si based junctions show a rectifying behaviour in the intermediate temperature regime for the lower doped Si(111) substrate and similar behaviour at a somewhat higher temperature for the Si(001), which again is characteristic of thermionic emission / diffusion across a Schottky barrier. Fits to the data here reveal barrier heights of 0.52 eV and 0.65 eV for the Fe_3O_4 / Si(111) and Fe_3O_4 / Si(001) structures respectively. The ideality factors for both these junctions is about 1.06. All barrier heights and carrier concentrations are summarized in table 3.1.

Semiconductor	Type	Carrier conc. in cm^{-3}	ϕ_B in eV	n	ϕ_B from AEP in eV, equ. 3.4
Si(111)	n	1.8×10^{14}	0.51	1.06	0.52
Si(001)	n	1.7×10^{15}	0.65	1.06	0.65
GaAs(100)	n	7.7×10^{17}	0.60	1.30	0.58
GaAs(100)	n	$\approx 3.5 \times 10^{18}$			
GaAs(100)	p	1.0×10^{18}	0.51	1.30	0.49
GaAs(100)	p	$\approx 3.5 \times 10^{18}$			

Table 3.1: Table of carrier concentrations and Schottky barrier heights for the various semiconductor substrates.

The difference between the barrier heights on Si(111) and Si(001) is explained by the formation of different interfacial layers during the initial stages of growth. While the

interface layer consists of a crystalline iron silicide layer of approximately 5 nm and an amorphous oxide layer of 2 nm after reactive sputtering of Fe_3O_4 on the Si(111), the iron silicide is very thin (≤ 1 nm) in the Fe_3O_4 sputtered on the Si(001), although a thicker amorphous oxide layer is present. The formation of these interface layers is detrimental for efficient spin injection from Fe_3O_4 electrodes into silicon as only a few atomic layers near the interface with a silicon channel determine the spin polarization of the injected carriers. Unfortunately this means that the objective of creating large negative spin currents in silicon based spin devices using Fe_3O_4 as a spin injector remains elusive.

A possible way around this could be to insert a well-defined tunnel barrier between the Fe_3O_4 and Si interface. This concept has already been demonstrated successfully for GaAs / ferromagnetic 3d transition metal structures using both AlO_x and MgO tunnel barriers at the interface [30] - [32] and so should work particularly well in Fe_3O_4 / GaAs structures. The inclusion of the tunnel barrier prior to Fe_3O_4 deposition might prevent interlayer diffusion, where such diffusion takes place, and hence sharpen the Fe_3O_4 / barrier and barrier / semiconductor interface.

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Chapter 4

Metal / Insulator / Semiconductor Systems

4.1 Introduction

This chapter presents an investigation into increasing spin injection efficiency through Schottky barriers. A tunnel barrier was introduced between the metal and semiconductor to form a ferromagnetic metal / insulator / semiconductor (FM / I / SC) system. The tunnel barriers of choice used in these systems are AlO_x and MgO . The injector source is $\text{Co}_{90}\text{Fe}_{10}$, as it has the highest spin polarization of all Co-Fe alloys, and the semiconductors used are medium doped n-type Si and GaAs. Transport through these junctions was studied as a function of temperature and barrier thickness.

The size of the junctions was reduced from an area of $2.5 \times 10^{-9} \text{ m}^2$ (50×50 square μm pillars) to an area of $7.85 \times 10^{15} \text{ m}^2$ (100 nm circular pillars). Tunnel barriers were also included in the nano sized junctions and transport was also studied as a function of junction size. A brief introduction to insulators follows.

4.1.1 Insulators

An insulator, also called a *dielectric*, is a material that resists the flow of electric current. If the valence electrons of a crystal exactly fill a number of bands, leaving the remaining ones completely empty, the crystal will be an insulator provided that there is an energy gap between the filled band and the next higher band. This means that there is no continuous way for the total momentum of the electrons to change since every accessible state is filled. Therefore when the crystal is subjected to an external electric field no current can flow.

A crystal can only be an insulator as long as the number of valence electrons in the primitive cell is an even integer. However even when a crystal does satisfy this it is still necessary to look at the bands. If the bands do overlap in energy then instead of having one completely filled valence band giving an insulator the crystal could end up with two partially filled bands giving a metal [1]. This is shown in figure 4.1

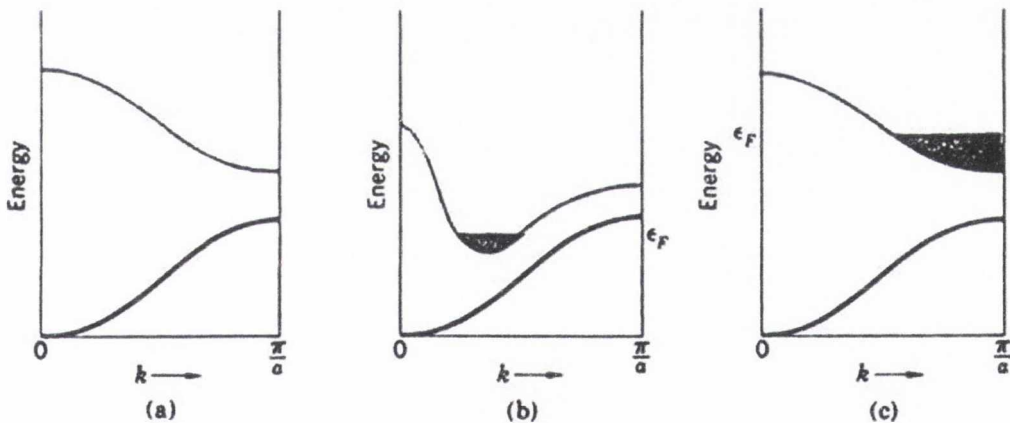


Figure 4.1: Occupied states and band structures, the thicker back line indicates the occupied band or band section. (a) is an insulator, (b) a metal or semi-metal due to band overlap and (c) a metal due to the electron concentration.

The alkali and noble metals have only one valence electron per primitive cell, so they are clearly metals with half filled conduction bands. The alkaline earth metals have two valence electrons per primitive cell, so they could be insulators, expect that the energy

bands overlap, similar to part (b) of figure 4.1, and so they are metals but not very good metals. Diamond, silicon and germanium each have eight valence electrons per primitive cell and the energy bands do not overlap, the pure crystals are insulators at absolute zero.

AlO_x and MgO insulators

The insulators AlO_x and MgO were used in these experiments as they are widely used insulators in research and have proved to be the most successful tunnel junction materials. In 1995 Moodera [3] and Miyazaki [4] independently reported significant tunnel magnetoresistance (TMR), > 10 % at room temperature, ratios that had previously been reported using magnetic tunnel junctions (MTJ), which had been fabricated using amorphous Al₂O₃ as the tunnel barrier and it was these initial results which sparked such a tremendous interest in magnetic tunnel junctions.

Since 2000, when the papers with the theoretical calculations on magnetic tunnel junctions of perfectly orientated Fe (001) / MgO (001) / Fe (001) predicted TMR ratios of hundreds of percent [5] - [7], there has been a huge effort to fabricate crystalline tunnel barriers, particularly MgO. It took until 2004 for the experiments to catch up with the theoretical predictions [8] & [9].

Figure 4.2 illustrates very nicely the TMR ratios associated with different barrier materials and how they have improved over recent years. It clearly shows AlO_x and MgO as giving the best ratios. Our group has also successfully fabricated MTJs using both AlO_x and MgO as tunnel barriers in the past [10] - [12] and for all these reasons these are the tunnel barriers of choice in this thesis.

through the barrier rendering it useless. Once the tunnel barriers were deposited in Chamber B the substrates were moved to Chamber A of the sputtering system, without breaking vacuum, where the 20 nm $\text{Co}_{90}\text{Fe}_{10}$ film was deposited and capped with a 5 nm Ta layer. Both films were deposited in an Ar pressure of 4×10^{-3} Torr. The Si substrates were etched for three minutes using hydrofluoric acid to remove a thermally grown 25 nm SiO_2 layer immediately prior to loading into the Shamrock sputtering system. The junctions were patterned into two different sizes, $50 \times 50 \mu\text{m}$ using UV lithography in order to have a well defined active area, and circular junctions of approximately 100 nm in diameter using e-beam lithography to see if the electrical transport depends on junction size. Both these lithographic methods were outlined in Chapter 2. A Cu or Au top contact was sputtered in Chamber A after top contact patterning using UV lithography for both junction sizes. The top contact was sputtered again in an Ar pressure of 4×10^{-3} Torr. Ohmic indium back contacts were soldered onto the back of the silicon substrates at 450 °C for one minute.

For consistency, the carrier concentration of the silicon substrate was once again determined by room temperature Hall effect and resistance measurements as outlined in Chapter 2. The result yielded a carrier concentration of $1.6 \times 10^{15} \text{ cm}^{-3}$ with $\rho = 2.3 \Omega\text{cm}$, which is in good agreement with previous measurements on similar substrates, Chapter 3. Using the barrier height, ϕ_B , obtained in Chapter 3 the depletion width of the Si(001) substrates is approximated¹ as $0.71 \mu\text{m}$ wide using,

$$x_d = \sqrt{\frac{2\varepsilon_0\varepsilon_r\phi_B}{qN_d}} \quad (4.1)$$

where ε_r is the relative static permittivity of the semiconductor and the value used for this was 11.9 [13]. ε_0 is the permittivity of free space, N_d is the carrier concentration of the semiconductor per m^3 and q is the magnitude of the charge on an electron. The Si

¹See Appendix A for more information on the depletion region approximation

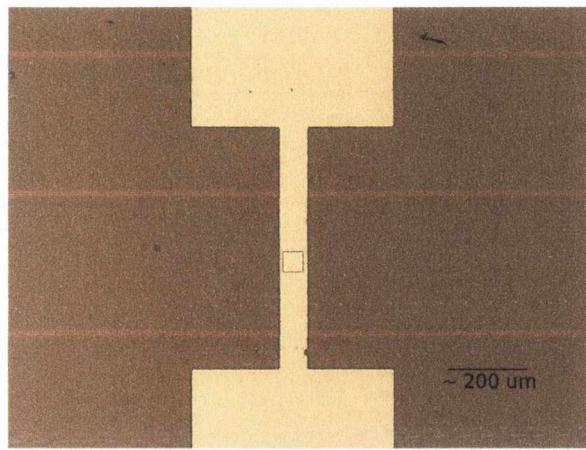
substrates were Phosphorous doped to make them n-type.

The transport measurements were performed as a function of temperature and barrier thickness. For the $50 \times 50 \mu\text{m}$ sized junctions the AlO_x barrier thickness was varied from 0 nm to 6 nm and the MgO thickness went from 0 nm to 4 nm in 1 nm steps. For the 100 nm sized junctions the barrier thickness varied from 0 nm to 4 nm for both barrier materials also in 1 nm steps. All transport measurements were performed using the cryohead part of the resistivity rig, as outlined in Chapter 2.

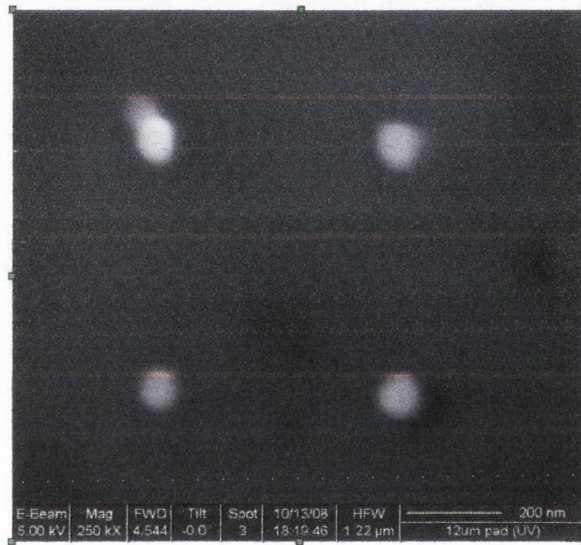
The pictures in figure 4.3 are of (a) one of the $50 \times 50 \mu\text{m}$ junctions. This picture was taken with a camera attached to a normal optical microscope. This junction has a patterned top contact. The actual junction is the small square in the middle of the Au contact “track”. Part (b) is of four junctions made using e-beam lithography. It can be seen that the diameters of the junctions are 90 – 100 nm and are in close proximity to each other. This picture was taken with an SEM, the same SEM used to pattern them but at a much lower accelerating voltage, 5 kV instead of 30 kV. In order to help with alignment of the contacts many of these junctions are patterned in close proximity to each other over a particular area of the substrate at specified locations. It is also very difficult to find a lone dot of 100 nm for imaging purposes, whereas these large areas can be seen almost immediately. Figure 4.4, part (a) is a zoomed out picture of part of one of these large areas for aligning and imaging. Part (b) of the figure is a schematic of how the junctions are patterned onto the substrate, including top contacts. Note that there is more than one junction patterned on each substrate so multiple junctions can be measured to confirm results across a substrate.

4.2.2 Film structures on Si substrates

One of the advantages of using MgO as a tunnel barrier is that it also acts as a spin filter, allowing only one spin orientation to pass through [14] & [15]. This is what enables such high TMR ratios using MgO and why AlO_x will never compete with it. However in order



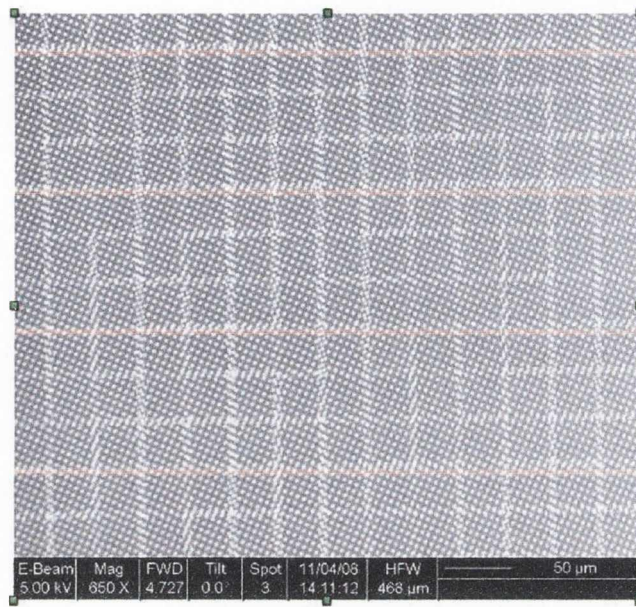
(a)



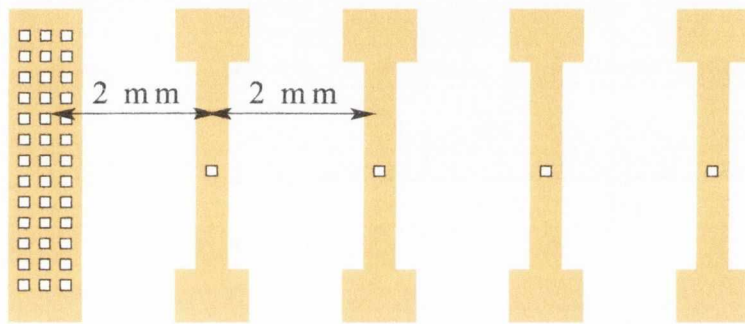
(b)

Figure 4.3: Picture of (a) one of the $50 \times 50 \mu\text{m}$ junctions with a Au top contact. This was taken with by a camera attached to a normal optical microscope. (b) is a picture of four 100 nm sized junctions in close proximity taken by an SEM microscope.

for MgO to act as a spin filter it must be crystalline. One of the challenges of this work was to grow crystalline MgO directly onto the silicon substrate. The slower the MgO deposition rate the more likely crystalline growth will take place, so the MgO is grown in as a low a pressure and power as possible to maintain a stable and reproducible plasma. The optimum Ar pressure and sputtering power were determined and they were used to grow MgO films on both Si(111) and Si(001) oriented substrates. The results can be seen



(a)



(b)

Figure 4.4: (a) is a picture of the alignment and imaging area of the substrate in the fabrication of the nano sized junctions. (b) is a schematic of how they are patterned to look on the substrate, including top contact patterning.

in figure 4.5.

Under these conditions it can be seen that crystalline MgO can be grown on the Si (001) substrate, part (a) figure 4.5, but not on Si(111), part (b) figure 4.5. A number of adjustments to the growth conditions were carried out in an attempt to obtain crystalline MgO growth on the Si(111) substrate but unfortunately the lattice mismatch between the two is just too great for it to be successful. Efforts were then concentrated on using the Si(001) substrates to fabricate the structures.

A rocking curve of the (002) MgO peak in figure 4.5, part (a) is shown in figure 4.6. The Gaussian fit to the curve in figure 4.6 gives a full width half maximum (FWHM) of approximately 6° . This is a measure of how well orientated a crystal is. The narrower the FWHM value is the better. Stress on the crystalline film can distort the orientation, giving it a wider FWHM value. This quite a broad rocking curve but still within an acceptable width, less than 8° .

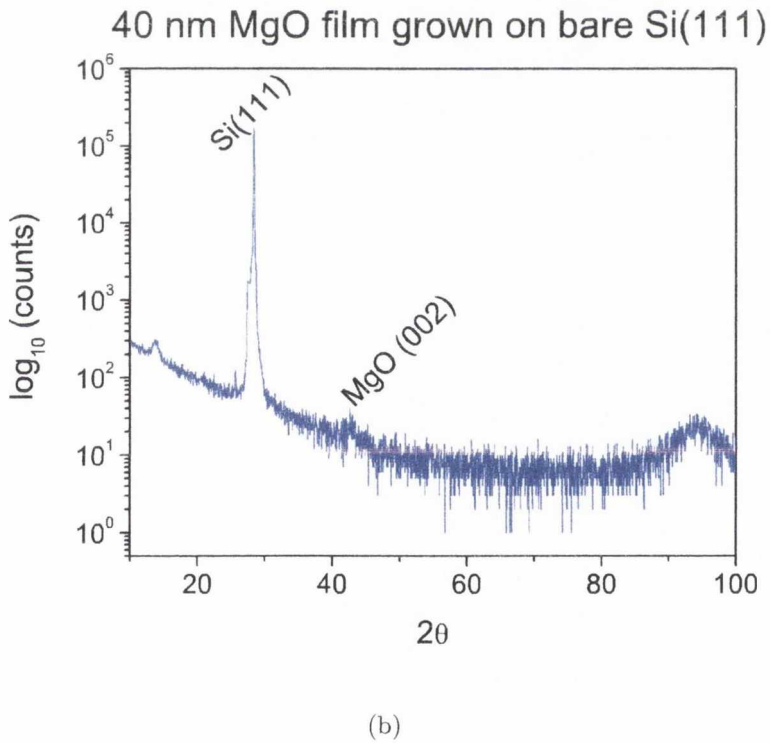
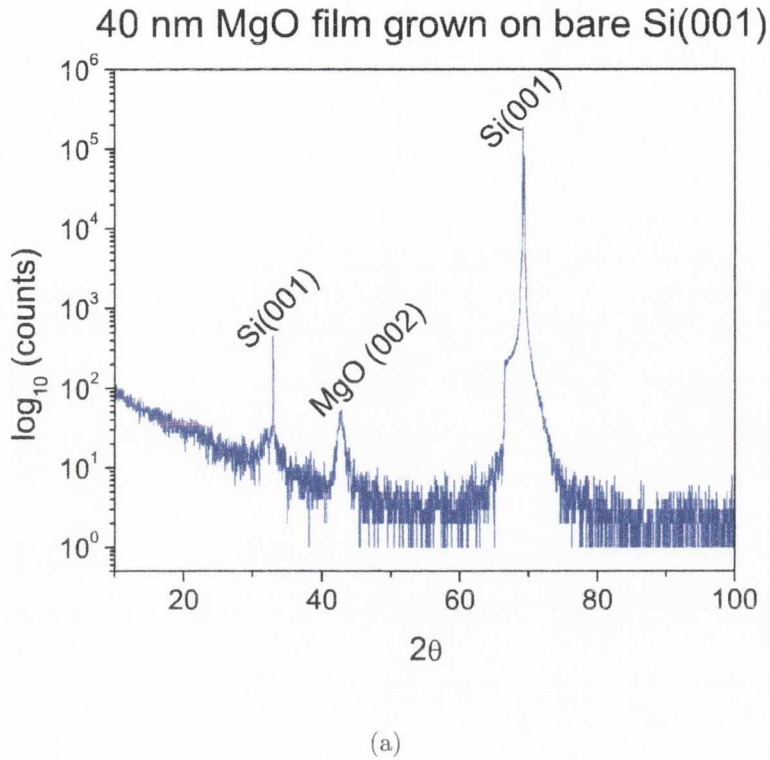


Figure 4.5: X-ray diffraction scans of 40 nm MgO films grown on (a) Si(001) substrate and (b) Si(111) substrate. The (002) MgO peak can clearly be seen in the film grown on the Si(001) substrate.

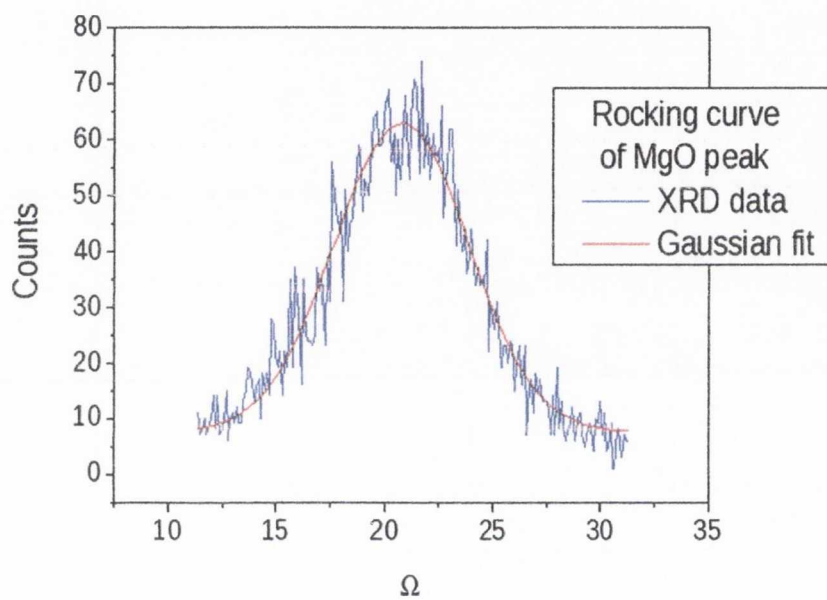


Figure 4.6: Rocking curve of the MgO(002) peak of MgO grown on Si(001). The blue line is the XRD data and the red line is the Gaussian fit to the curve, giving a FWHM of $\approx 6^\circ$.

4.2.3 Magnetic properties of the $\text{Co}_{90}\text{Fe}_{10}$ films

Figure 4.7 shows the magnetization curve for a 20 nm thick film of $\text{Co}_{90}\text{Fe}_{10}$ at both 300 K and 4 K. At 4 K the films exhibit a coercive field of about 45 mT. At room temperature it has a saturation magnetization of $4.8 \times 10^5 \text{ Am}^{-1}$, which increases to $6.8 \times 10^5 \text{ Am}^{-1}$ at 4 K for these films. This is lower than the expected value for $\text{Co}_{90}\text{Fe}_{10}$, which is 1.4×10^6 but literature has shown that the saturation magnetization for $\text{Co}_{90}\text{Fe}_{10}$ films is very much dependant on film thickness [16].

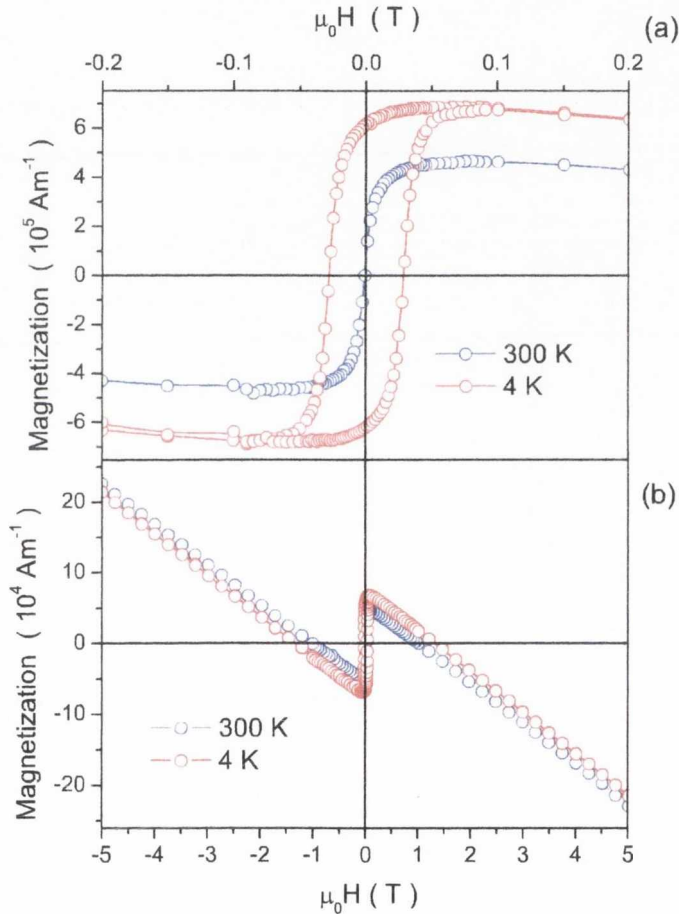


Figure 4.7: Magnetization curve of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on a Si(001) substrate at 300 K, blue line, and at 4 K, red line. (a) is a display of the data between -200 mT and 200 mT and (b) is all the data between -5 T and 5 T. The diagonal slope is due to the diamagnetic signal of the semiconductor. The data presented here is courtesy of M. Venkatesan.

4.2.4 Electrical Transport, $50 \times 50 \mu\text{m}$ sized Junctions

Figures 4.8 to 4.11 and 4.12 to 4.15 show the $I - V$ measurements for $\text{Co}_{90}\text{Fe}_{10}$ on Si with 0 to 3 nm of AlO_x and MgO tunnel barriers between the $\text{Co}_{90}\text{Fe}_{10}$ and Si respectively. The data is in 25 K intervals between 50 K and 300 K. Despite the presence of a tunnel barrier the curves still display an asymmetric, rectifying current-voltage characteristic within defined temperature regions, much the same as discussed in Chapter 3.

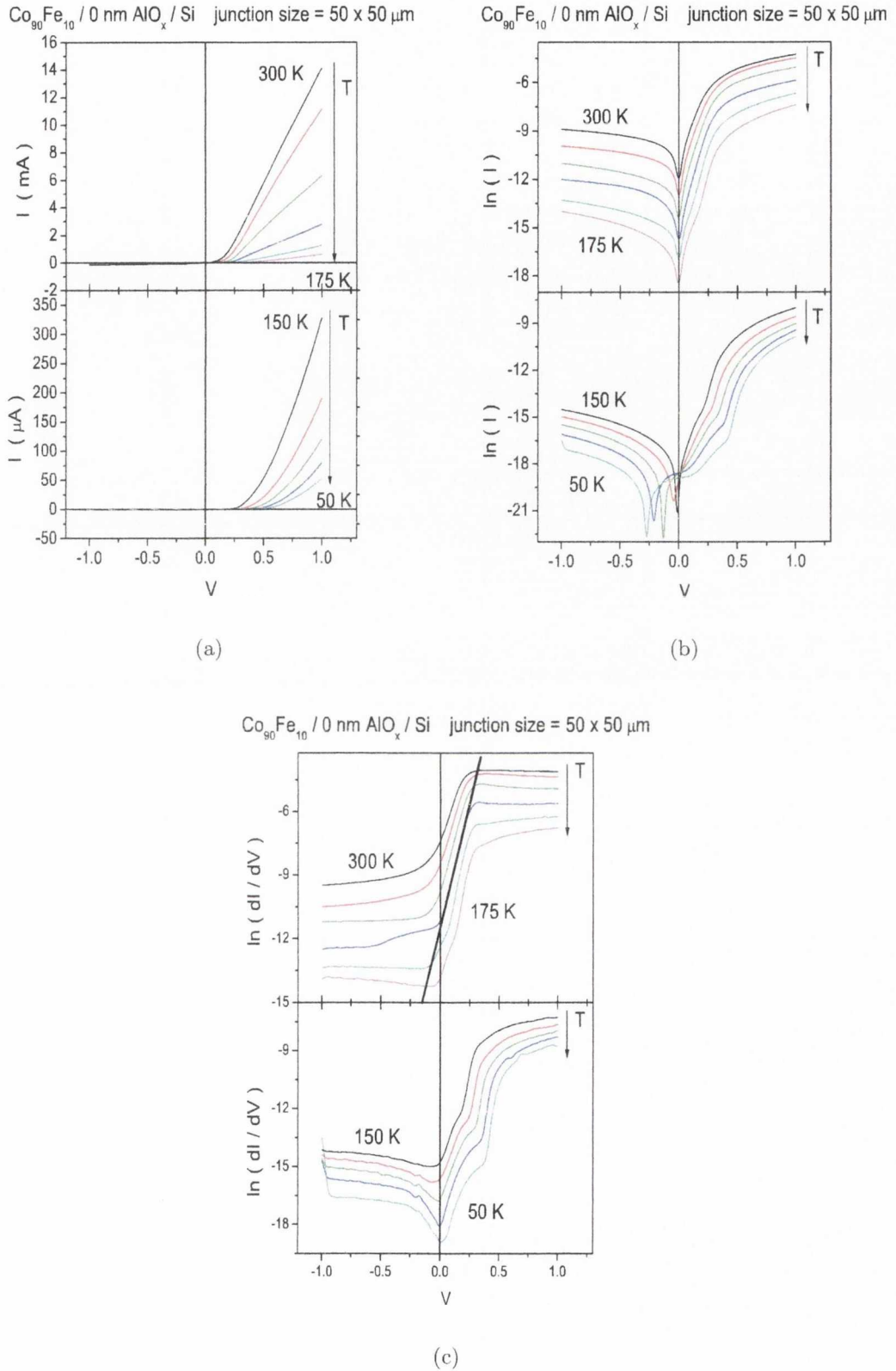


Figure 4.8: $I - V$ measurements as a function of temperature for 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 0 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V and (c) $\ln(dI/dV)$ vs. V , the black line here is the fit used to extract the ideality factor, n , and the barrier height, ϕ_B .

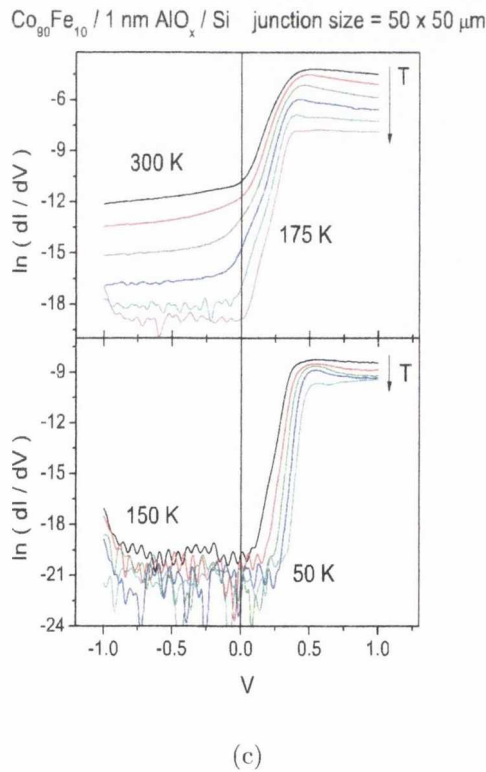
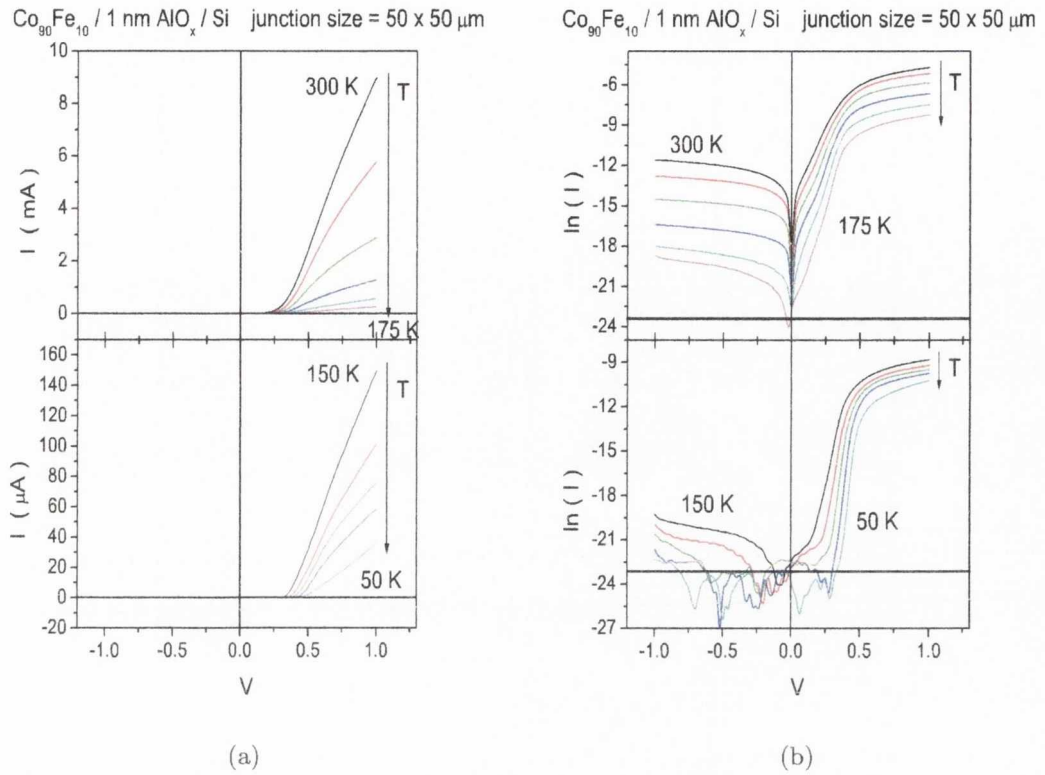


Figure 4.9: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on Si (001) with 1 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

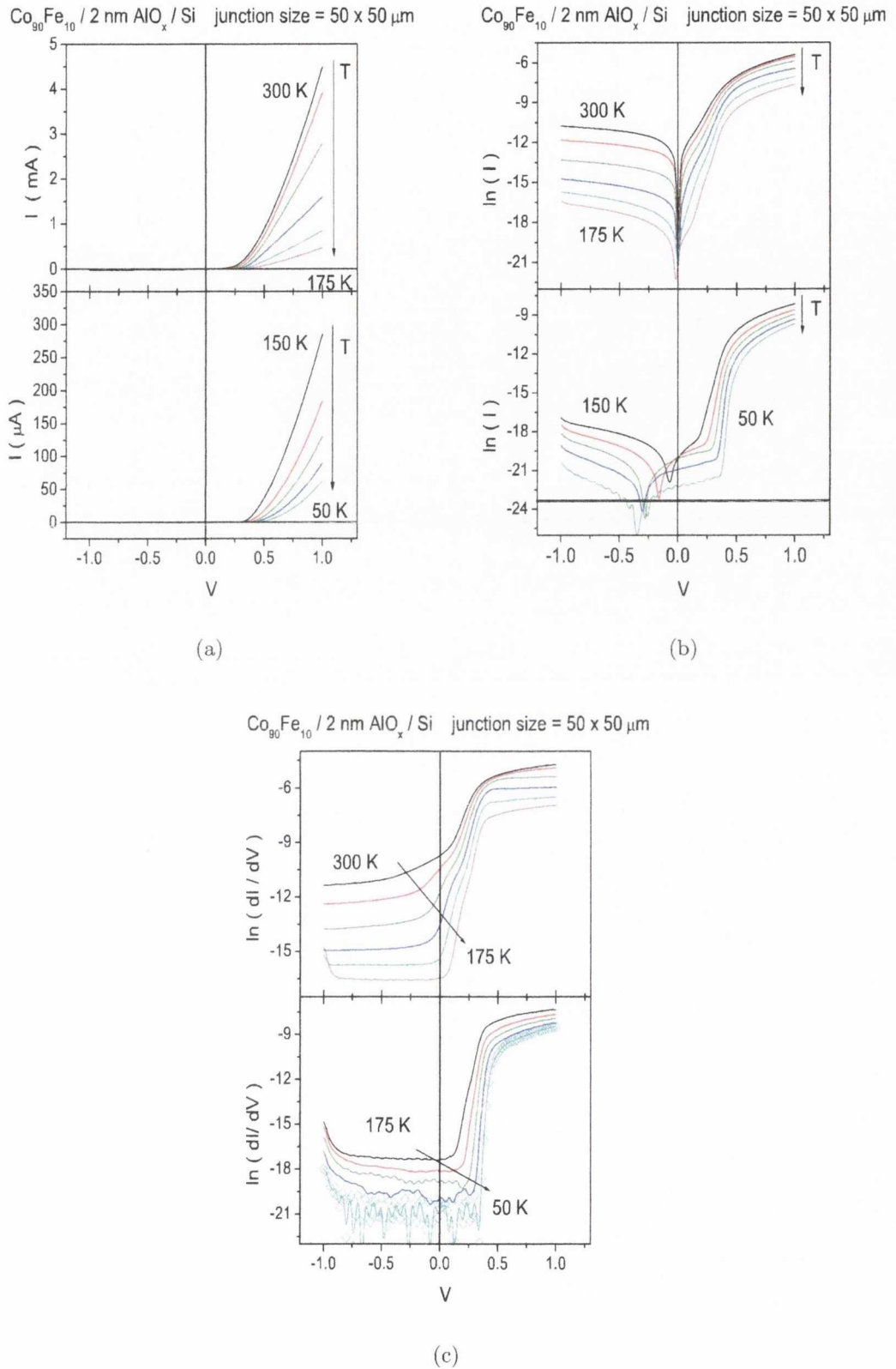


Figure 4.10: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 2 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1 \text{ nA}$), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V

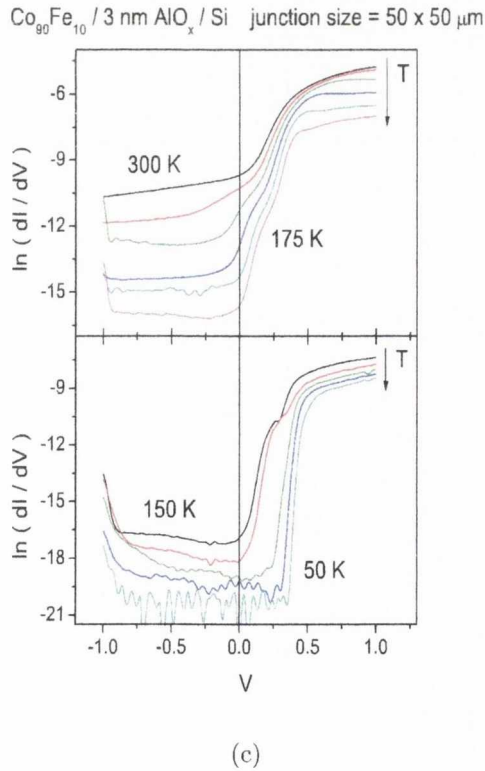
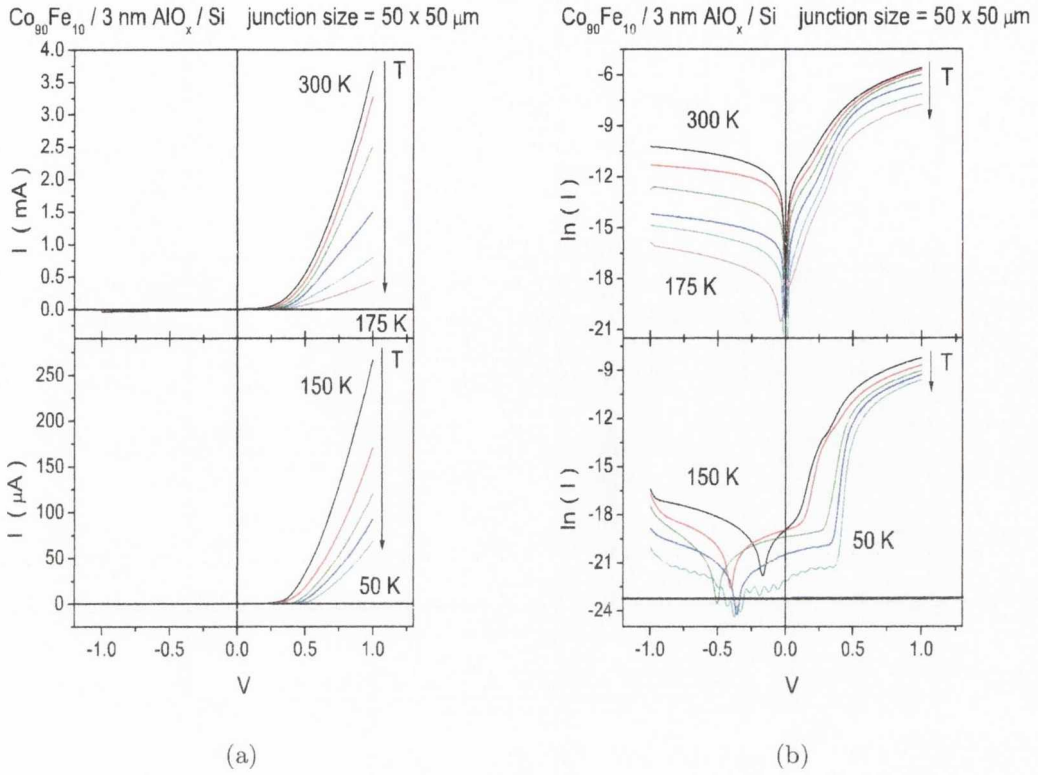


Figure 4.11: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 3 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1 \text{ nA}$), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

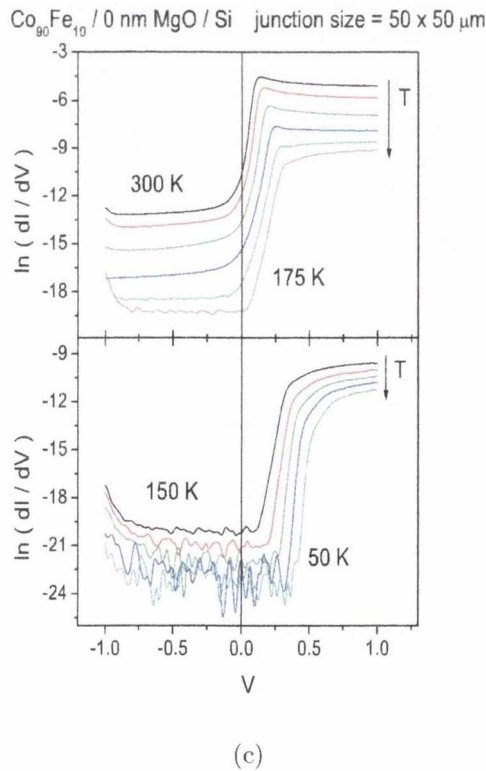
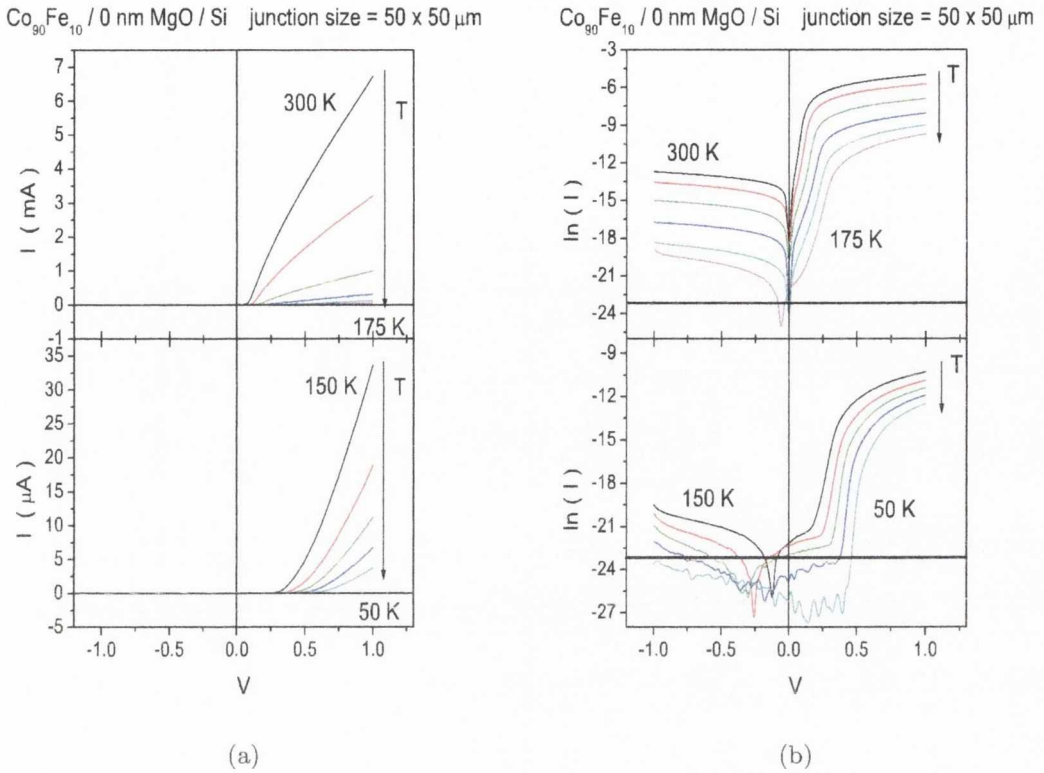


Figure 4.12: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 0 nm of the tunnel barrier MgO between them. (a) Graph of I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V

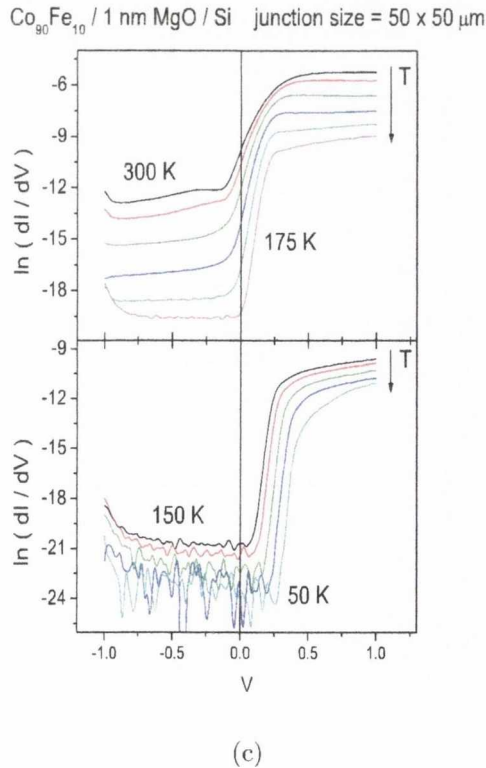
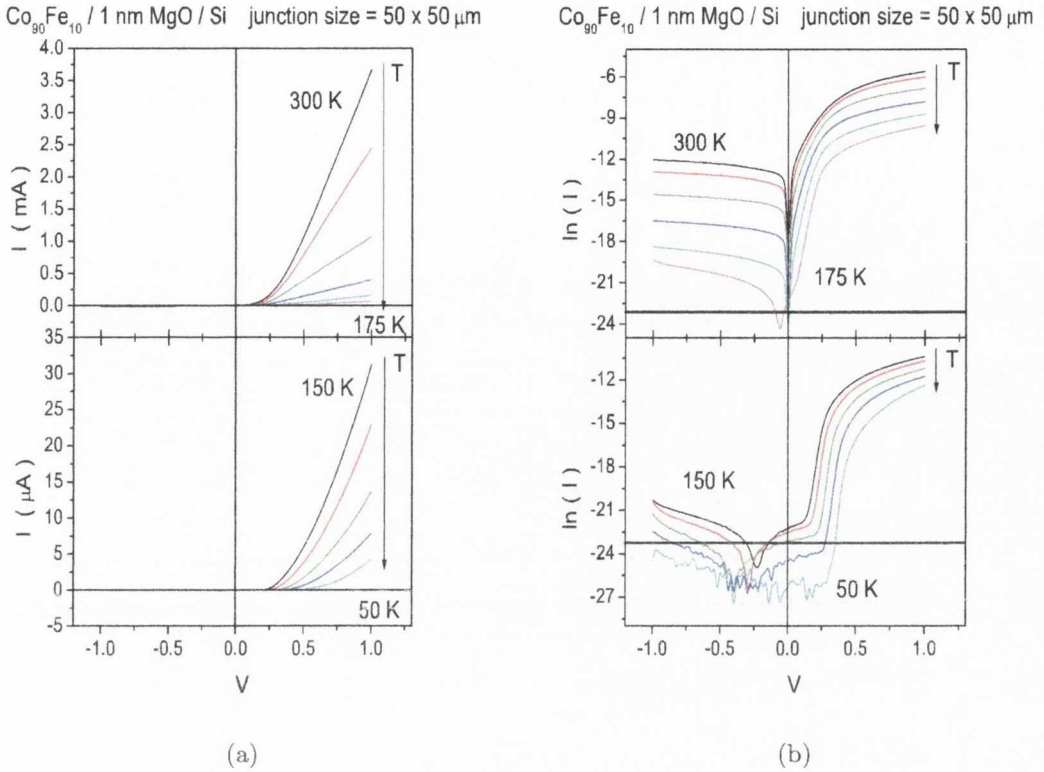


Figure 4.13: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on Si (001) with 1 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

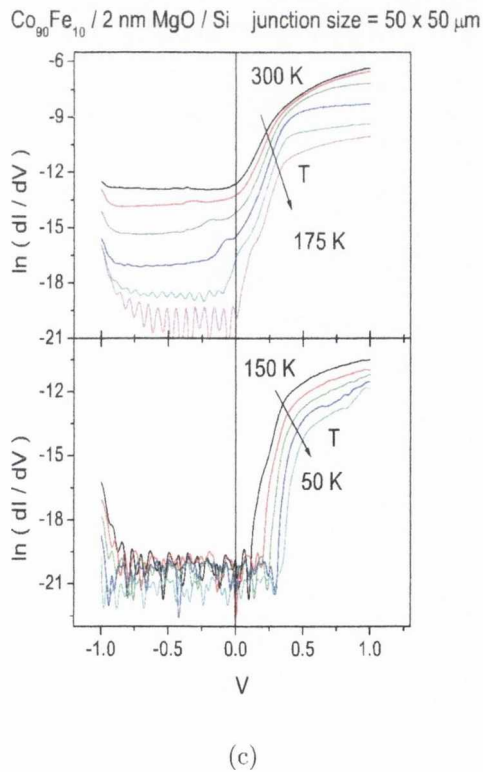
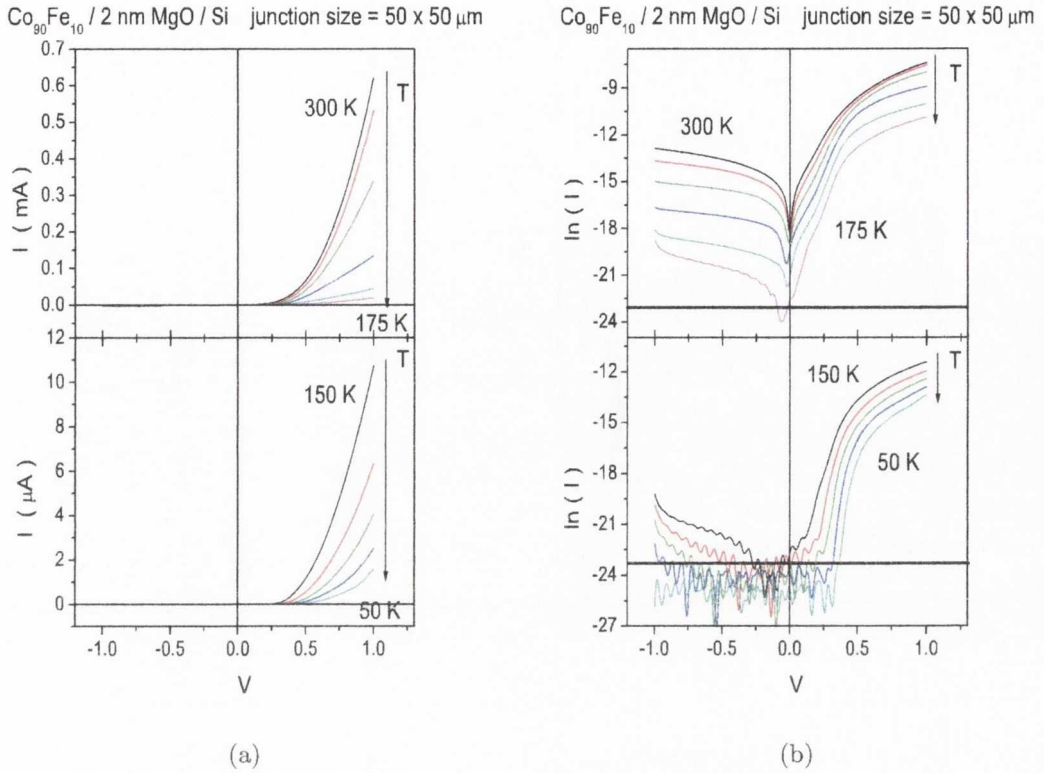


Figure 4.14: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on Si (001) with 2 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

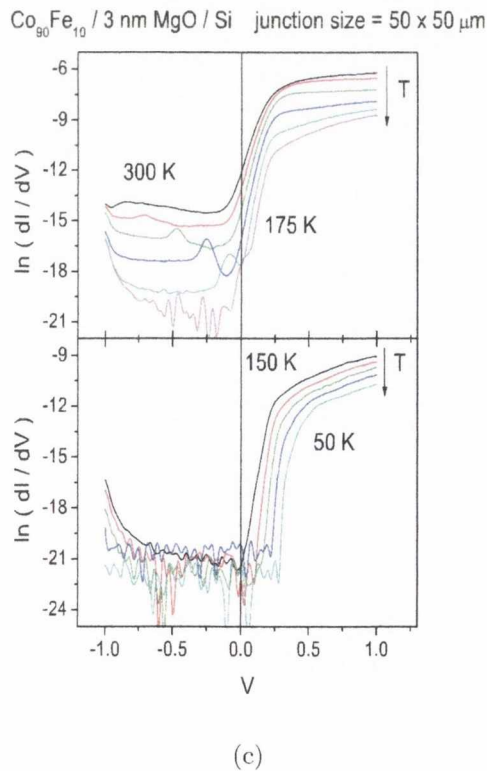
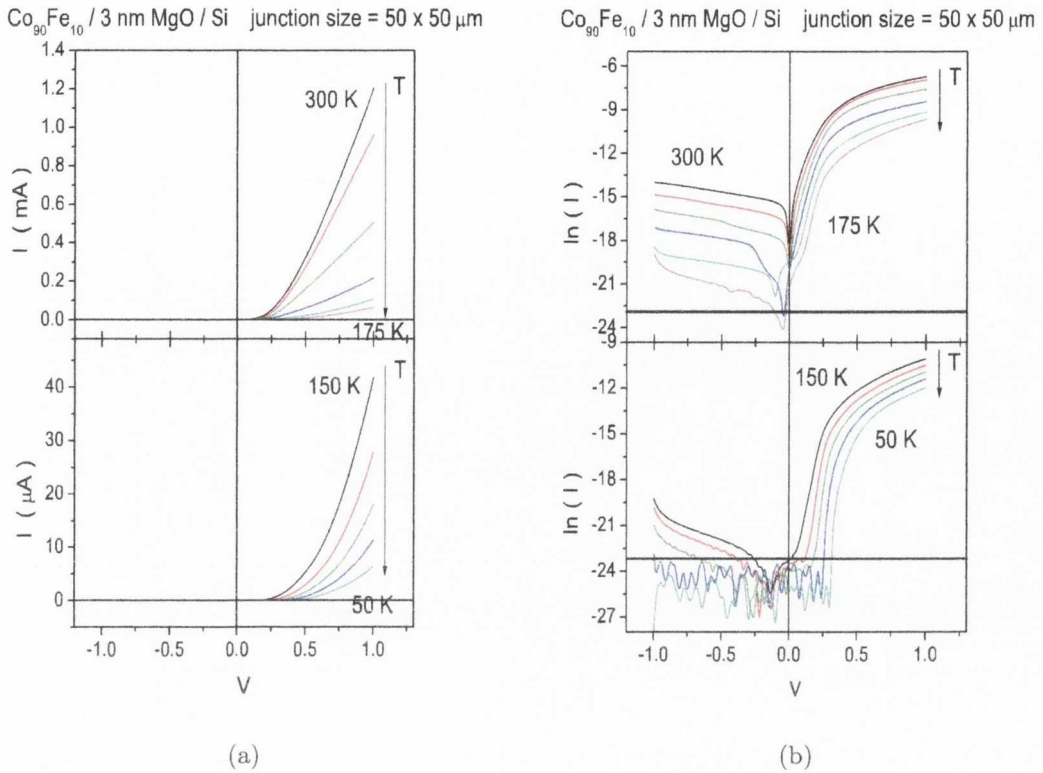


Figure 4.15: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 3 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

Three distinct temperature regimes can be identified, at low temperatures the curves become fully symmetric at low bias ($T \leq 150$ K), this is demonstrated in figure 4.16, which is a zoom in of the low bias region at low temperatures of $\ln(I)$ vs. V for the first junction shown, figure 4.8. part (b). At intermediate temperatures the curves are

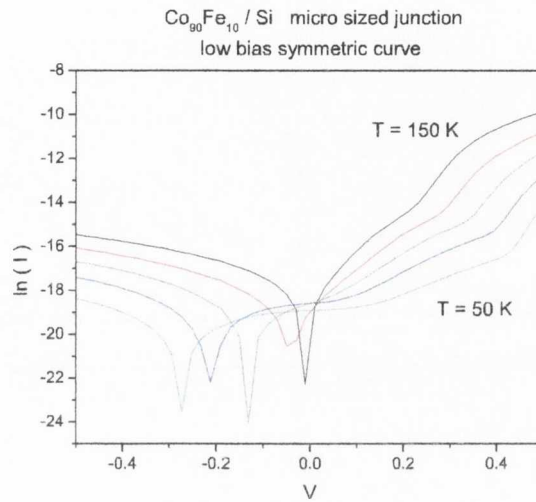


Figure 4.16: This graph shows the low bias region of the $\ln(I)$ vs. V curve of part (b) in figure 4.8 at low temperatures. The symmetric regions can be seen more clearly here.

asymmetric ($175 \text{ K} \leq T \leq 250$), which can be difficult to see due to the noise from the lower temperature data, and at higher temperatures the asymmetry between forward and reverse bias is reduced ($T \geq 275$) due to the series resistance. In the low temperature regimes the bias range over which the curves are symmetric increases as the tunnel barrier thickness increases, indicating tunneling as the dominant mode of electrical transport across the interfaces. This is to be expected due to the tunnel barrier. What is surprising is how asymmetric the data remains at higher temperatures. This remains true for all thicknesses of the tunnel barrier but as the thickness of the barrier increases a distortion can be observed in the forward bias, which becomes more apparent in the $I - V$ plots as the temperature decreases. There is also a zero bias offset that starts to appear at lower temperatures, generally for $T \leq 150$ K. These are seen in the plots of $\ln(I)$ vs. V .

This offset may be to some charge build up at the interface. Graphs of $\ln(I)$ vs. V for all thicknesses of AlO_x at 300 K, 200 K and 100 K are shown in figure 4.17, in which this distortion can be clearly seen as a function of AlO_x thickness, particularly in the plots at 100 K.

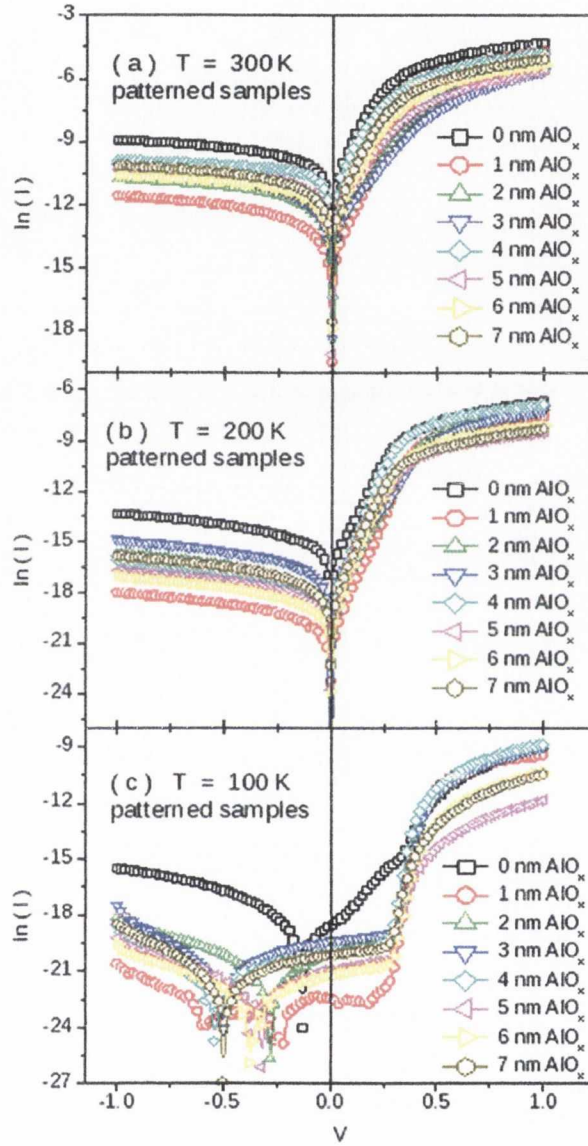


Figure 4.17: Plots of $\ln(I)$ vs. V for all thicknesses of AlO_x at (a) 300 K, (b) 200 K and (c) 100 K. Junction size is $50 \times 50 \mu\text{m}$.

Since the data displays such asymmetric behaviour, which is characteristic of thermionic

emission / diffusion across a Schottky barrier, it was fitted using this model [2] & [17]. To recap on the thermionic emission / diffusion model, which has been previously outlined in Chapter 3, the current dependence on bias voltage is given as,

$$I = I_S \left(e^{\frac{qV}{nkT}} - 1 \right) \quad (4.2)$$

where,

$$I_S = A_e A^{**} T^2 e^{\frac{q\phi_B}{kT}} \quad (4.3)$$

A_e is the active area, A^{**} is the effective Richardson constant, ϕ_B is the Schottky barrier height and n is the ideality factor. The theory behind equation 4.2 has been discussed in detail in the first chapter. Differentiating and taking the natural logarithm of equation 4.2 results in,

$$\ln \left(\frac{dI}{dV} \right) = \ln \left(\frac{I_S q}{nkT} \right) + \frac{q}{nkT} V \quad (4.4)$$

And so a fit of the slope of the data plotted as $\ln(dI/dV)$ vs. V , part (c) in figures 4.8 to 4.15, in the small forward bias region will give the ideality factor, n . The intercept of the line can be used to calculate the barrier height, an example is shown by the black fit line in part (c) of 4.8.

To determine the barrier heights, ϕ_B , the total area of the sample is used, which has been patterned to be $2.5 \times 10^{-3} \text{ mm}^2$ and an effective Richardson constant, A^{**} , of $110 \text{ Acm}^{-2}\text{K}^{-2}$. The barrier heights and ideality factors for all junctions, where possible to fit are outlined in table 4.1 along with the temperature the used. Unfortunately, as can be seen in table 4.1 all of the ideality factors are very high in these junctions. It is understandable that the ideality factors should be high once a tunnel barrier is introduced but even in the junctions where there is no tunnel barrier, the 0 nm junctions, n is still

Material	Thickness in nm	ϕ_B in eV	n	T in K
	0	0.42	2.2	250
		0.39	2.3	200
AlO _x	1	0.41	1.9	250
		0.37	2.3	200
AlO _x	2	0.28	2.3	250
		0.34	2.6	200
AlO _x	3	0.35	3.6	250
		0.32	3.3	200
AlO _x	4	0.62	2.4	250
		0.58	1.8	200
AlO _x	5	0.64	3.1	250
		0.60	1.7	200
AlO _x	6	0.46	2.4	250
		0.45	1.7	200
	0	0.51	0.97	250
		0.48	1.39	225
MgO	1	0.42	2.16	250
		0.42	1.84	225
MgO	2	0.46	2.82	225
MgO	3	0.48	1.58	250

Table 4.1: The barrier heights, ϕ_B , and ideality factors, n , for all junctions fabricated in the μm size on Si.

high except where there was no MgO barrier present. It is a problem that decreasing the junction size leads to high ideality factors. This has been a feature in discussions with other people working on Schottky barriers and using the same thermionic emission / diffusion model. They have also observed high ideality factors when fabricating small devices. One very interesting aspect of the data is that with the initial introduction of a tunnel barrier the Schottky barrier height appears to decrease, reaching its lowest level when there is 2 nm of AlO_x in the Co₉₀Fe₁₀ / AlO_x / Si system. Figures 4.18 and 4.19 are plots of $\ln(I)$ versus the barrier thickness for the AlO_x and MgO systems respectively

at three different temperatures showing how the current is affected with the introduction the tunnel barriers.

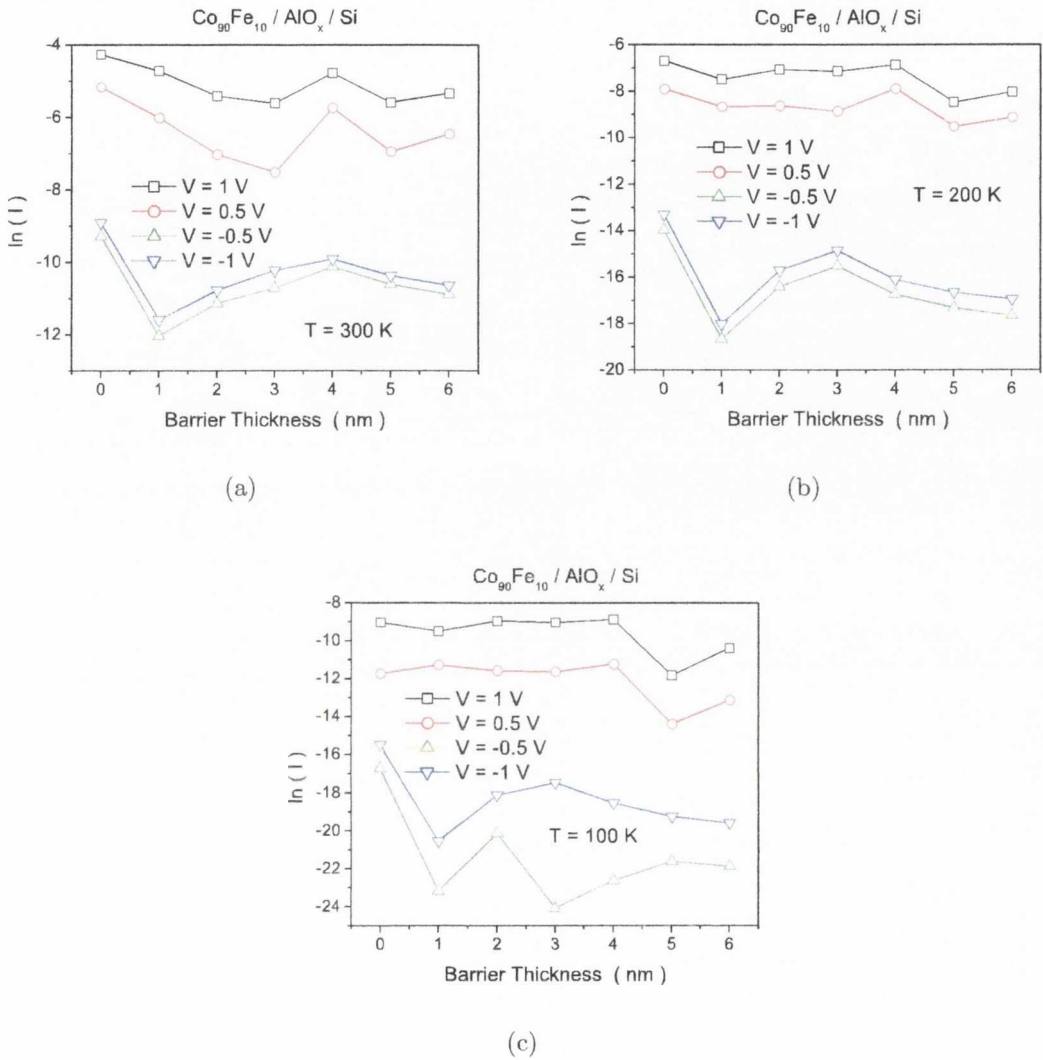


Figure 4.18: Plots of $\ln(I)$ vs. AlO_x barrier thickness on Si substrates at (a) 300 K, (b) 200 K and (c) 100 K. The current values are taken for voltages that are -1 V, -0.5 V, 0.5 V and 1 V. Junction size is $50 \times 50\ \mu\text{m}$.

At 300 K the forward bias current starts to decrease slightly and steadily with the introduction of an AlO_x tunnel barrier, part (a) of figure 4.18, until the barrier is 4 nm thick, then the current picks up again but never reaches the value it was at 0 nm. The reverse bias current takes an initial decrease with the introduction of 1 nm of AlO_x but

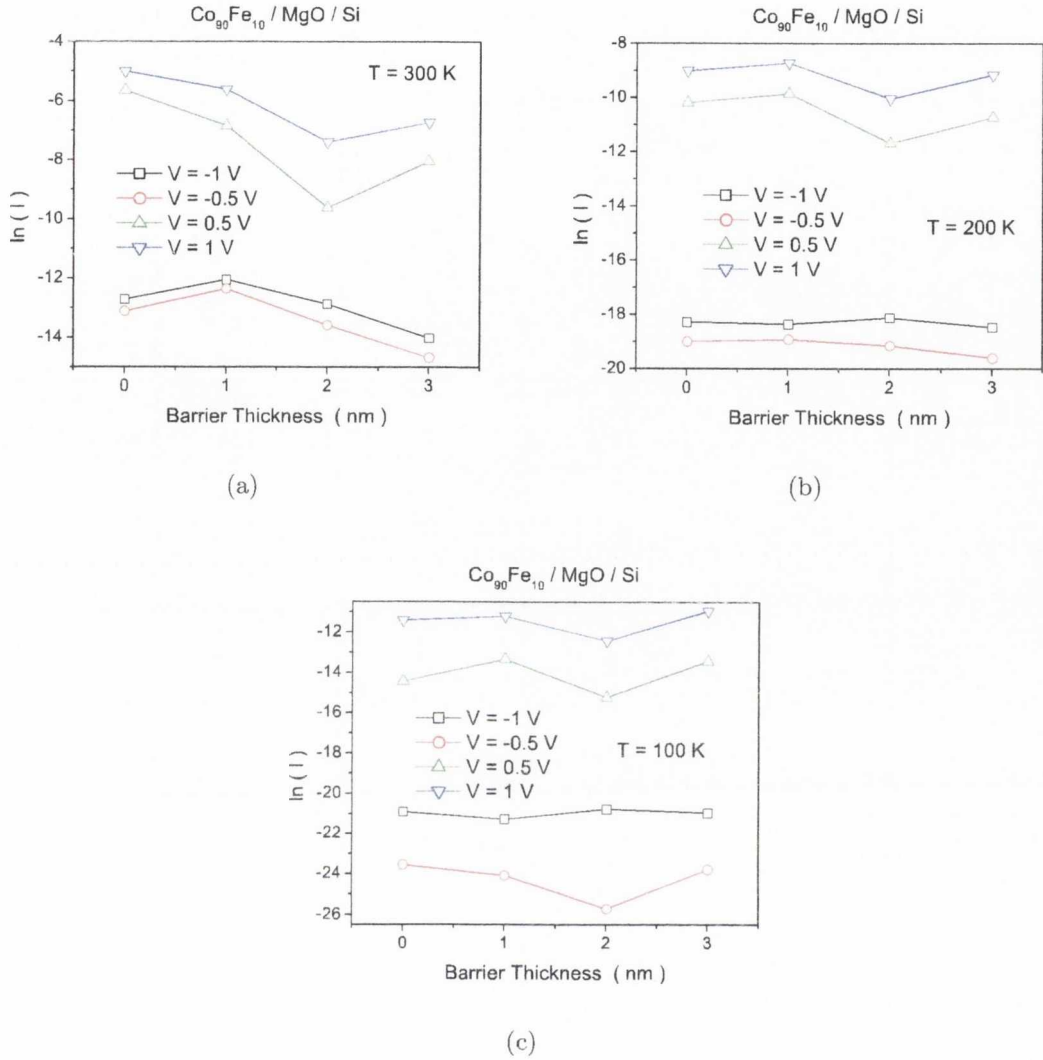


Figure 4.19: Plots of $\ln(I)$ vs. MgO barrier thickness on Si substrates at (a) 300 K, (b) 200 K and (c) 100 K. The current values are taken for voltages that are -1 V, -0.5 V, 0.5 V and 1 V. Junction size is $50 \times 50 \mu\text{m}$.

then starts to increase from this point, but again without reaching the 0 nm value. This trend in the data is generally true across the other temperatures. In the MgO system there is a slight increase in the reverse bias current at 300 K, part (a) of figure 4.19, with the introduction of 1 nm of MgO. The current drops as the barrier thickness increases from this point. With decreasing temperature this increase seems to shift from 1 nm of MgO to 2 nm and can also be observed in the forward bias. The observation of an increase

in reverse bias, however slight is quite exciting as it is the current flowing in the reverse direction in which the injection of polarized spins into the semiconductor takes place.

Having such high ideality factors means that the data is unsuitable to be fitted using an activation energy plot. In the extrapolation of a barrier height from such a plot the ideality factor is assumed to be 1. When it is close to 1, as it was for all junctions studied in Chapter 3, it is fine to use this method but here they are just too high.

4.2.5 Electronic Transport, 100 nm Junctions

Figures 4.20 to 4.23 and 4.24 to 4.27 show the $I - V$ measurements for $\text{Co}_{90}\text{Fe}_{10}$ on Si with 0 to 3 nm of AlO_x and MgO tunnel barriers between the $\text{Co}_{90}\text{Fe}_{10}$ and Si respectively. Again the data is in 25 K intervals between 50 K and 300 K. It is important to note that the transport through these nano junctions is again rectifying, with a small reverse bias current.

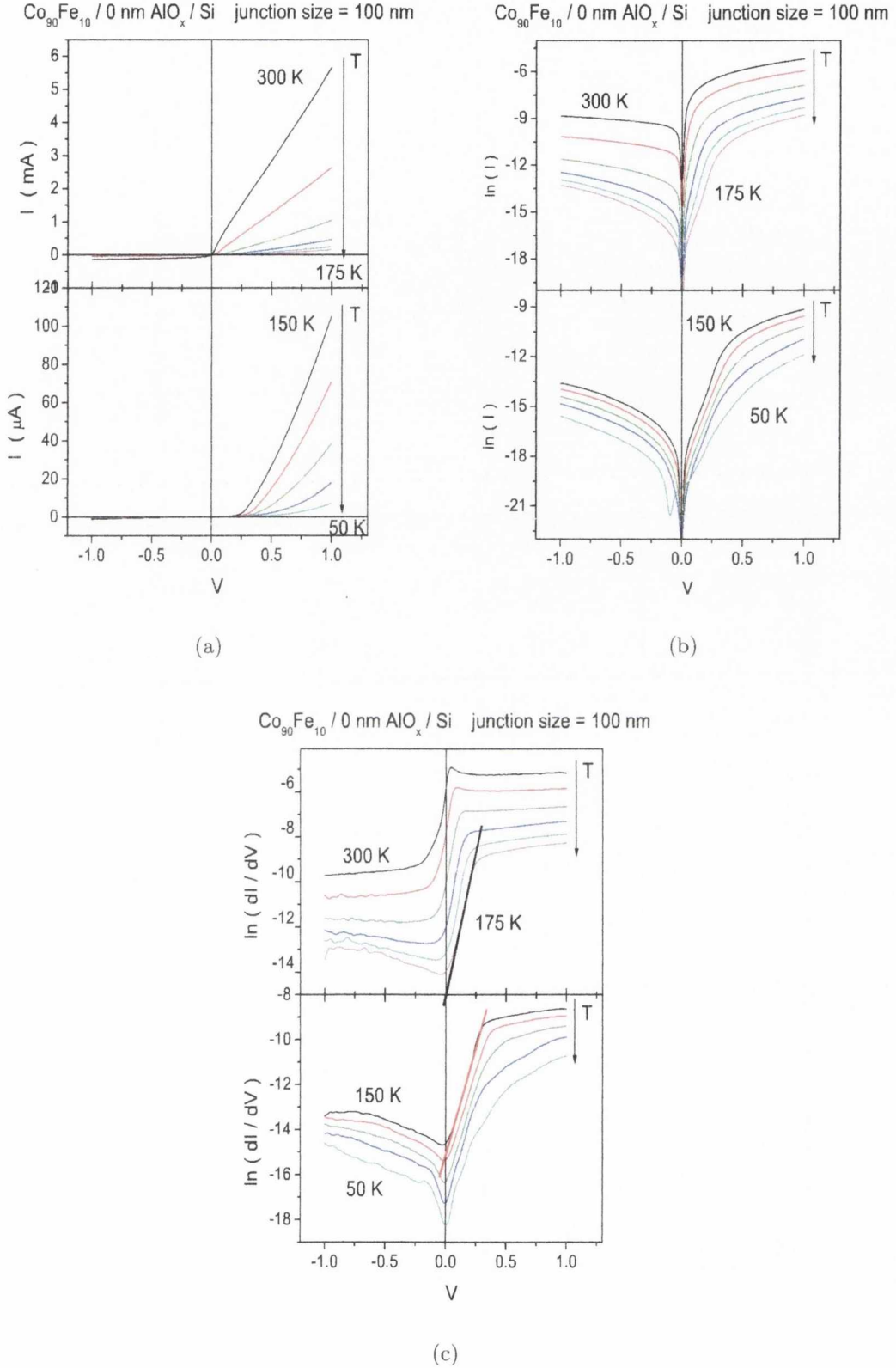


Figure 4.20: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 0 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V and (c) $\ln(dI/dV)$ vs. V , the back and red lines are the fits in order to determine the barrier height, ϕ_B , and the ideality factor, n .

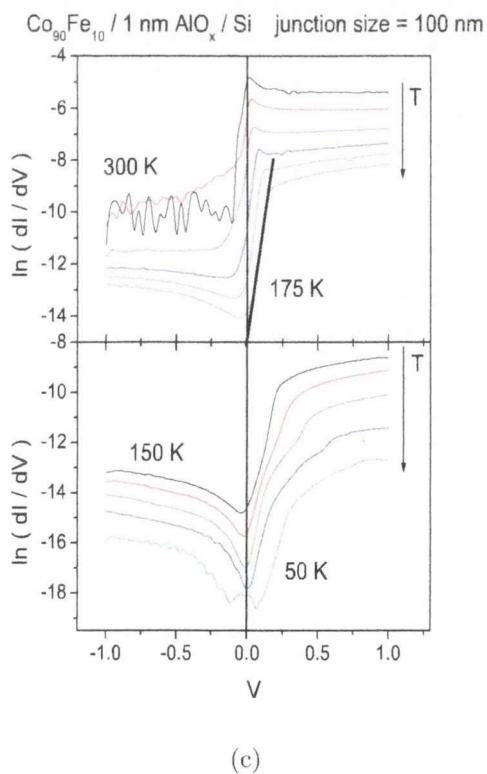
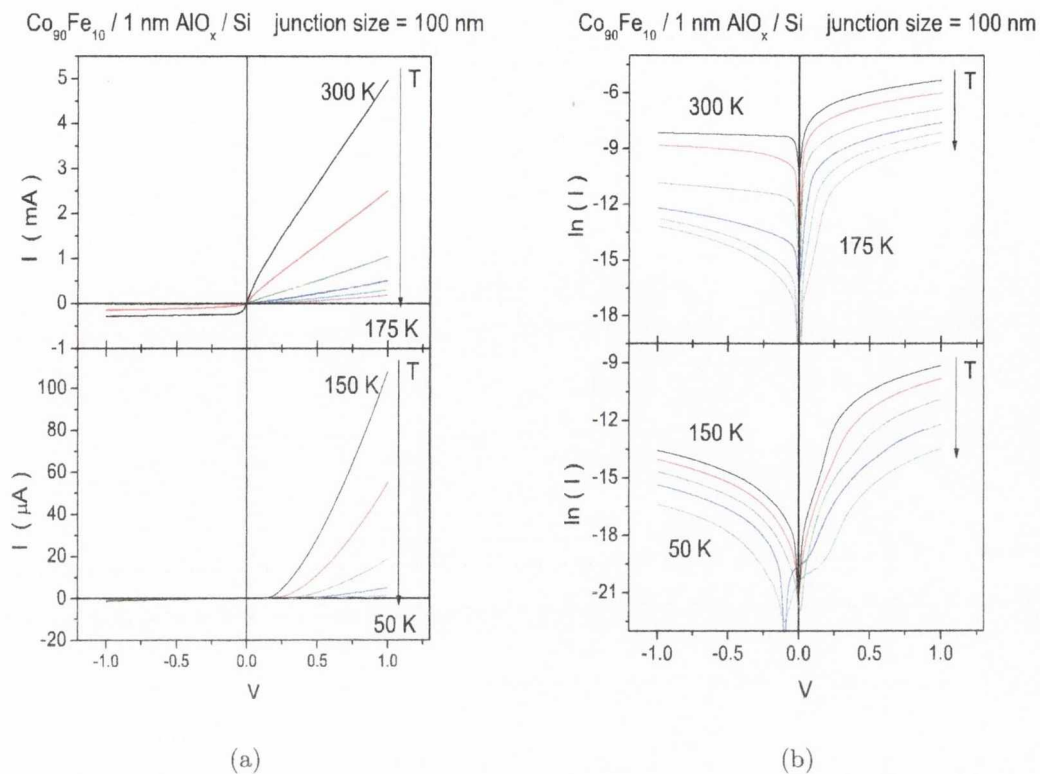


Figure 4.21: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 1 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V and (c) $\ln(dI/dV)$ vs. V .

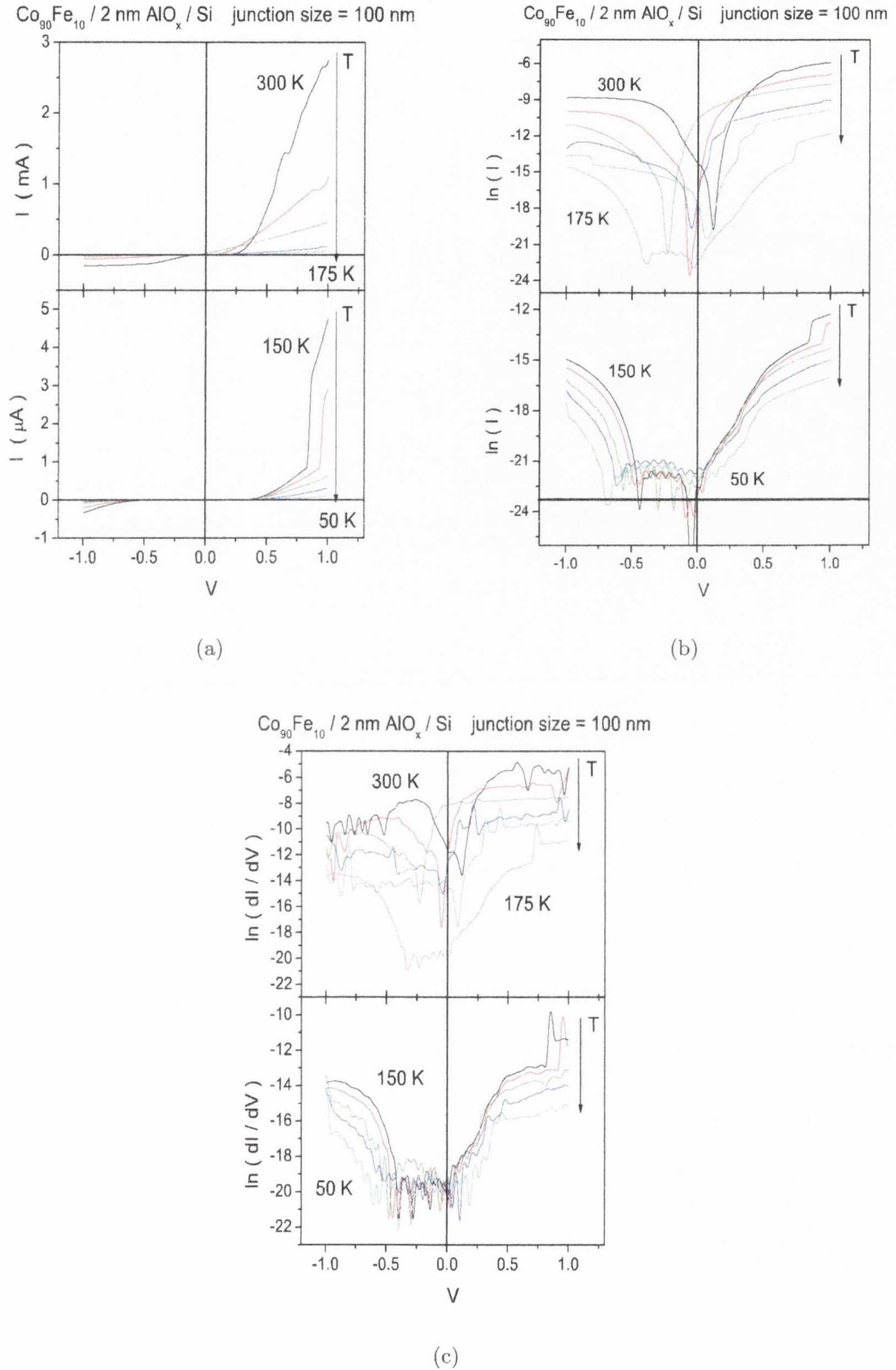


Figure 4.22: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 2 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

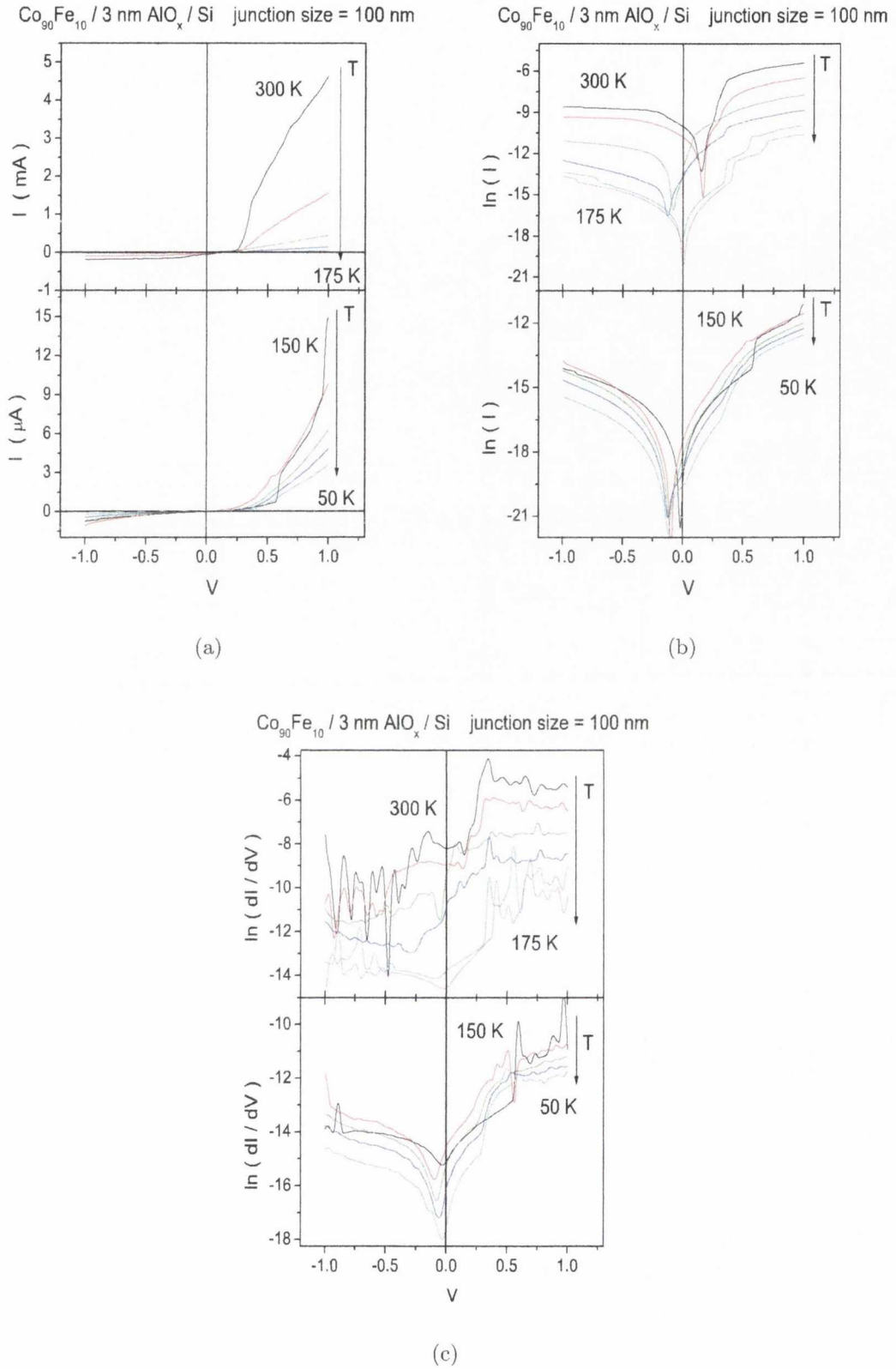


Figure 4.23: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 3 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V and (c) $\ln(dI/dV)$ vs. V .

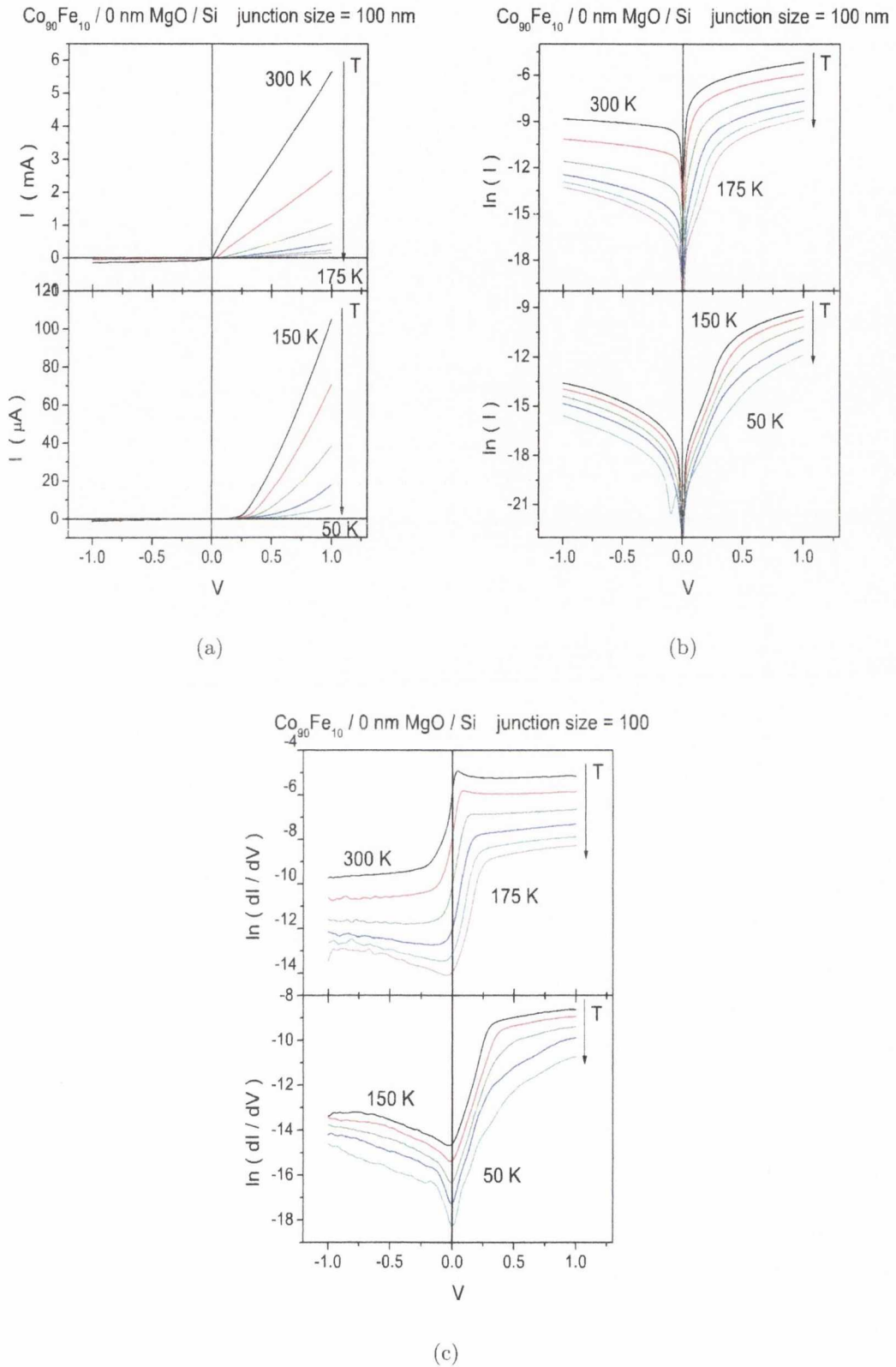


Figure 4.24: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on Si (001) with 0 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V and (c) $\ln(dI/dV)$ vs. V .

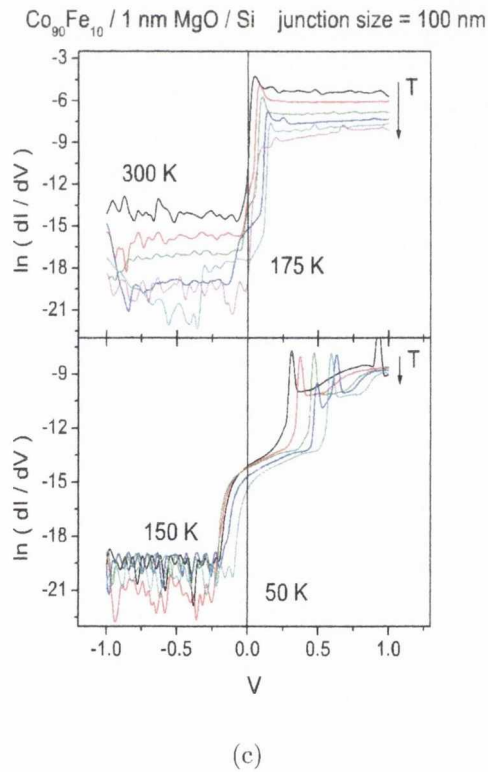
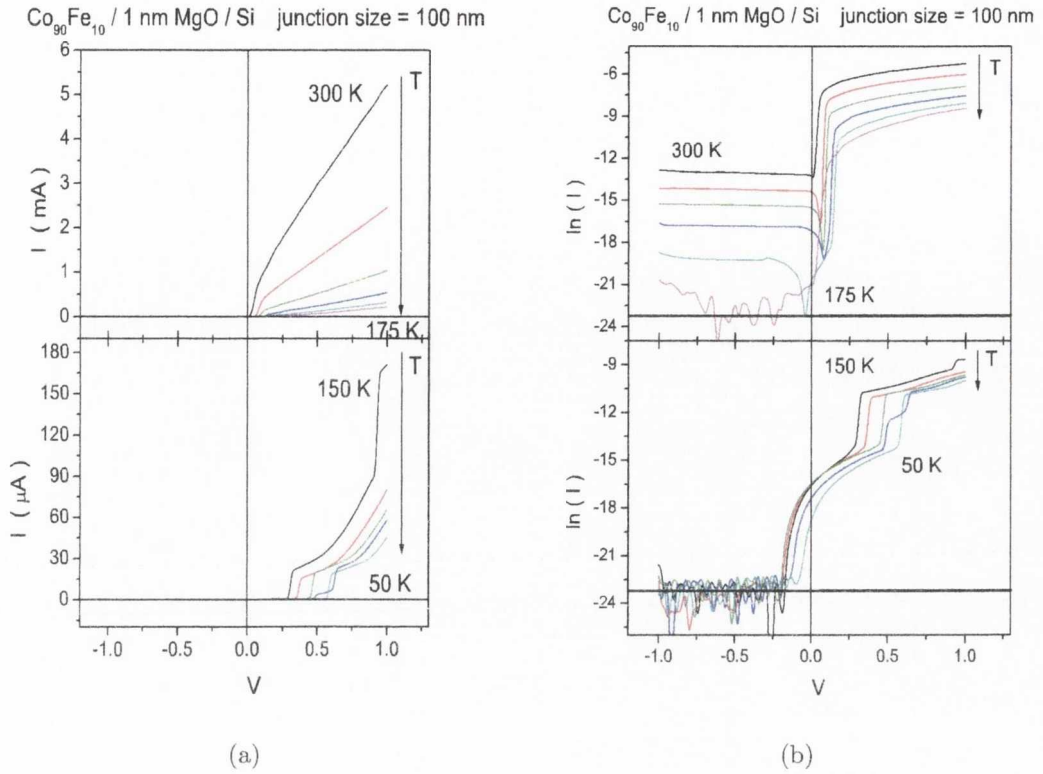


Figure 4.25: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on $\text{Si}(001)$ with 1 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

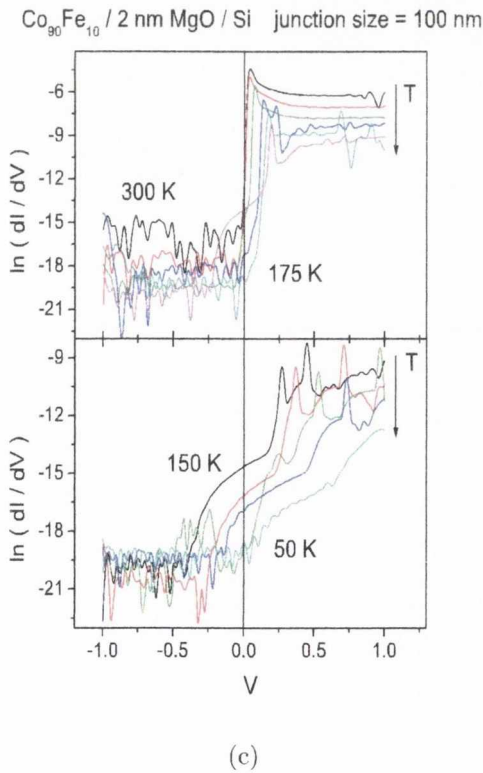
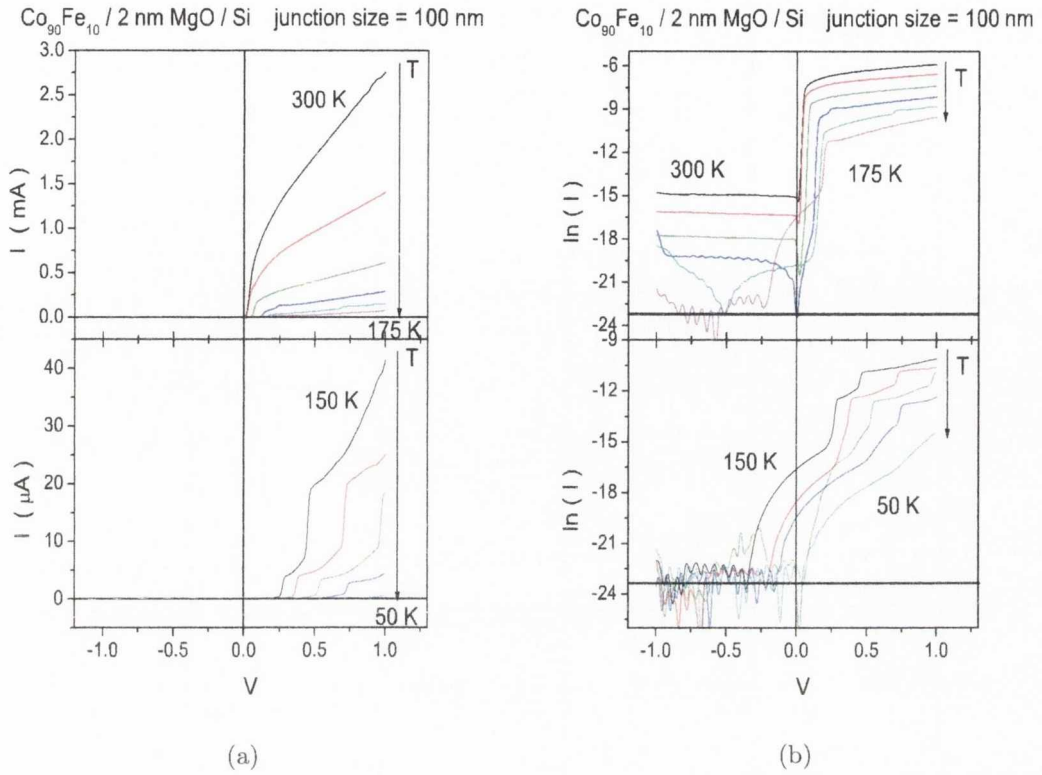


Figure 4.26: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on $\text{Si}(001)$ with 2 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1 \text{ nA}$), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

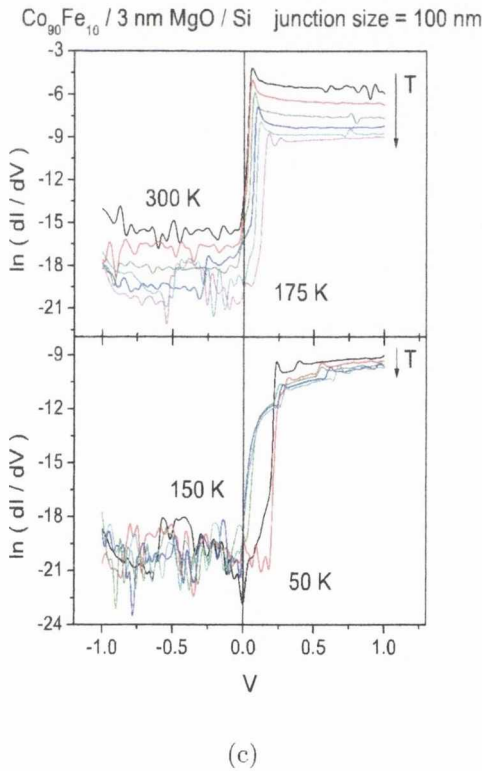
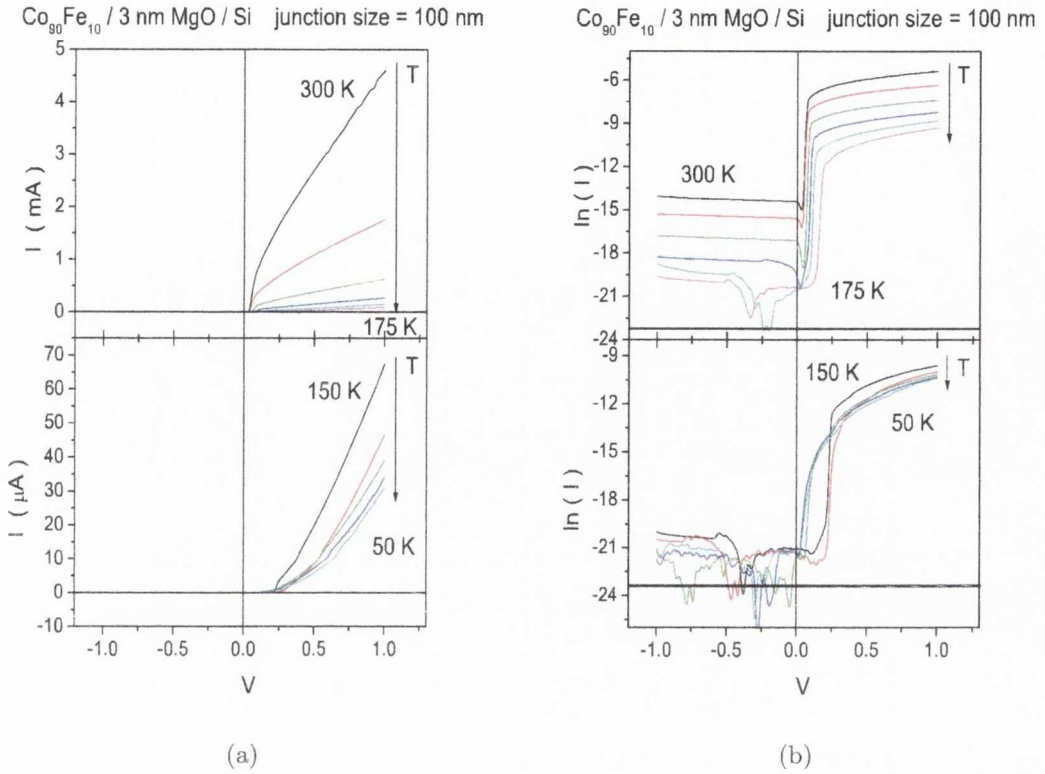


Figure 4.27: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on $\text{Si}(001)$ with 3 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

Looking first at the current through the nano sized junctions where there is an AlO_x tunnel barrier inserted between the $\text{Co}_{90}\text{Fe}_{10}$ and Si. The current through these junctions when there is no tunnel barrier is remarkably high given that these junctions are of the order of 10^6 times smaller in area than the junctions in figures 4.8 to 4.15. There is not much of a change in the forward bias current when 1 nm of AlO_x is introduced but the current in the reverse bias seems to increase slightly, parts (b) of figures 4.20 and 4.21. The current also stays asymmetric in both junctions as the temperature decreases to $T \leq 75$ K and then at low bias the data becomes symmetric. At higher temperatures, $T \geq 265$ K in both the junction without a tunnel barrier and with 1 nm of AlO_x , the asymmetry of the curve is reduced. When the AlO_x thickness is increased to 2 nm and 3 nm the shape of the curves changes drastically. It is still rectifying in so much as the current under forward bias is greater than the current under reverse bias but, as is obvious from parts (b) and (c) in figures 4.22 and 4.23, there is no possibility of trying to extract the barrier height from this data. Tunneling plays a much more dominant role in the current in these nano sized junctions than it did in the micro sized ones. The magnitude of the current, while reduced at these thicknesses of AlO_x is still quite high considering the size of the junction and the fact that the transport through junctions is dominated by the tunnel barrier.

When MgO is used as a tunnel barrier in the nanoscale junctions it immediately dominates the transport through the junction but without affecting much of a change in the magnitude of the forward bias current. However it lowers the current flow under negative bias, parts (b) figures 4.25, 4.26 and 4.27. To clearly see how the current is affected by barrier thickness plots of $\ln(I)$ vs barrier thickness are shown in figures 4.28 and 4.29 for the AlO_x and MgO tunnel barriers respectively.

These figures confirm the current increase under reverse bias when 1 nm of AlO_x is introduced between the $\text{Co}_{90}\text{Fe}_{10}$ and Si. They also confirm that for all other thicknesses of AlO_x and all thicknesses of MgO, the current decreases with increasing barrier thickness

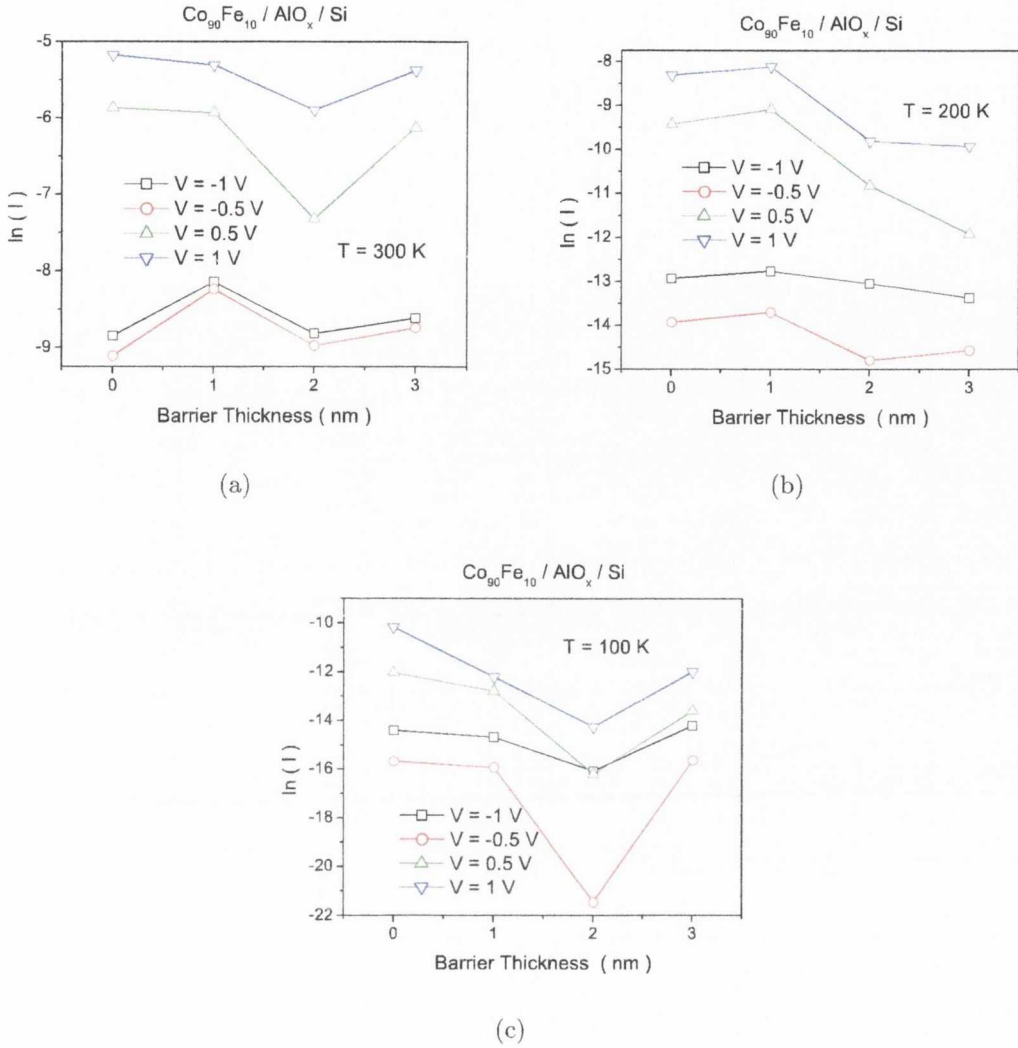


Figure 4.28: Plots of $\ln(I)$ vs. AlO_x barrier thickness on Si substrates at (a) 300 K, (b) 200 K and (c) 100 K for the 100 nm sized junctions. The current values are taken for voltages that are -1 V, -0.5 V, 0.5 V and 1 V. Junction size is 100 nm.

under reverse bias. Under forward bias the current decreases in general with barrier thickness but where the barrier is MgO the change under forward bias is marginal.

In the junctions with no tunnel barrier the current dependence on forward bias for $V > \frac{3kT}{q}$ was fitted to the thermionic emission / diffusion model given by equations 4.2 and 4.4. The slope of the small forward bias part of the curves in (c) of figures 4.20 and 4.24 gives the ideality factor. The intercept is used to calculate the barrier height. A fit

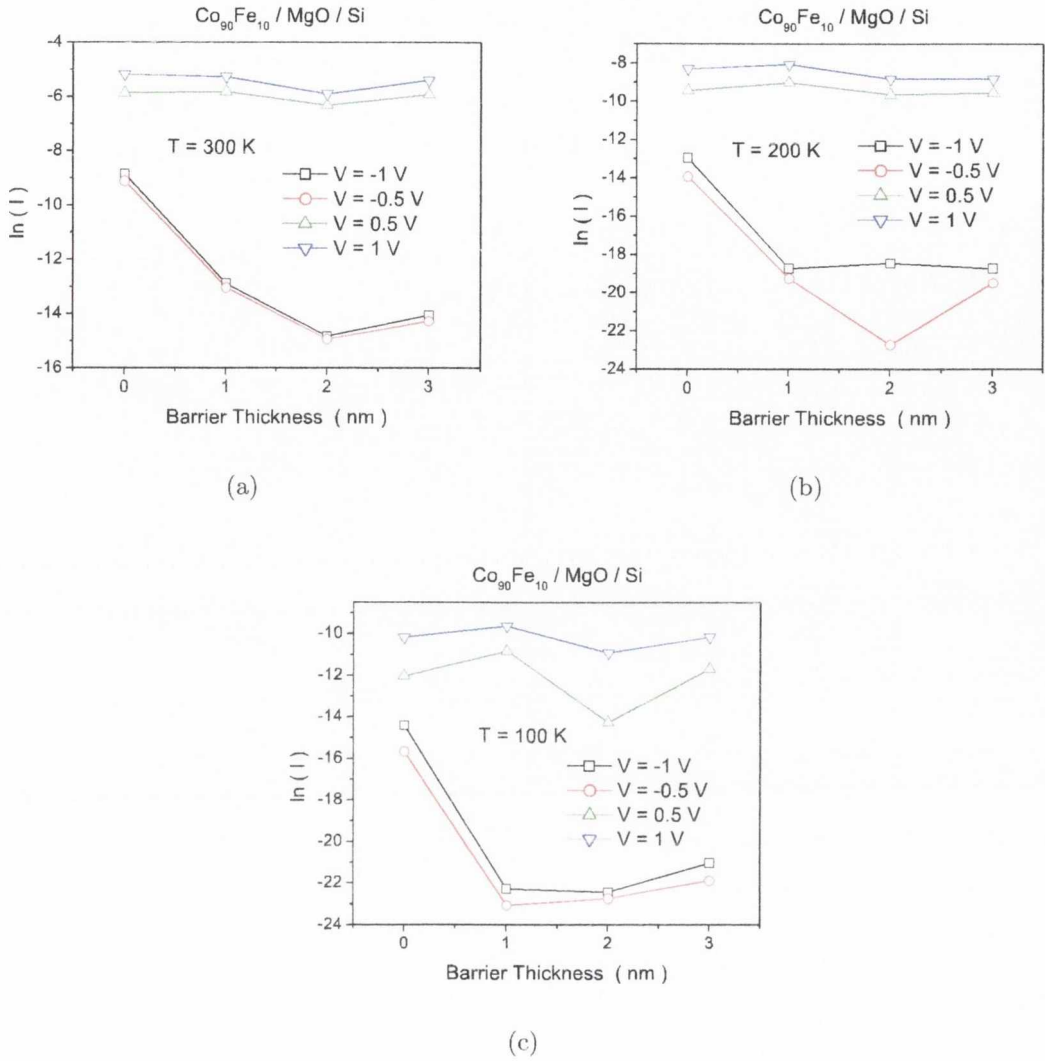


Figure 4.29: Plots of $\ln(I)$ vs. MgO barrier thickness on Si substrates at (a) 300 K, (b) 200 K and (c) 100 K for the 100 nm sized junctions. The current values are taken for voltages that are -1 V, -0.5 V, 0.5 V and 1 V. Junction size is 100 nm.

line is shown in part (c) of figure 4.20. Using $A_e = 7.85 \times 10^{-11}$, calculated using πr^2 where $r = 50$ nm, as the junctions are circular in shape with a diameter of 100 nm, and $A^{**} = 110 \text{ Acm}^{-2}\text{K}^{-2}$ a barrier height, ϕ_B , of 0.12 eV with an ideality factor, n , of 2.75 is obtained in the temperature range of $225 \text{ K} \leq T \leq 125 \text{ K}$. The junction with 1 nm of AlO_x was also fitted and a ϕ_B of 0.10 eV with an n of 1.93 was determined. It was not possible to fit the other junctions.

Steps start to appear in the $I - V$ curves once the tunnel barrier is introduced. These steps can be clearly seen in parts (c) of figures 4.22 and 4.23 and figures 4.25 to 4.27.

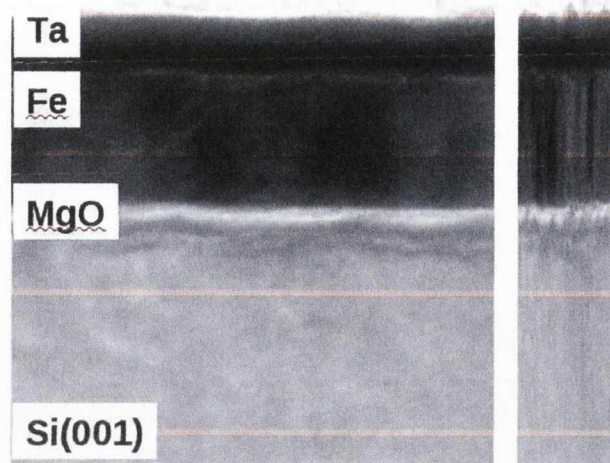
4.2.6 Interface Properties

Figure 4.30, part (a) shows a low magnification tunneling electron microscopy (TEM) image and part (b) shows a high resolution tunneling electron microscopy (HRTEM) image on an Fe / MgO / Si structure. These images were taken by Ana M. Sánchez in Departamento de Ciencia de los Materiales e IM y QI, Universidad de Cádiz, Spain. The panel on the right of part (a) of figure 4.30 is a digitally compressed image. The lateral dimension is scaled by a factor of 10 for a better illustration of film roughness. This image clearly reveals a relatively large MgO barrier roughness when grown on a Si (001) substrate. The thickness of a nominally 4 nm thick MgO layer varies between 3.4 nm and 4.6 nm. Unfortunately the HRTEM images indicate that despite obtaining an MgO (002) peak for a 40 nm film grown on a Si (001) substrate, figure 4.5, part (a), a thin MgO tunnel barrier film on Si (001) is amorphous. However, there is no evidence of any unwanted interfacial layers forming between either the Si / MgO interface or the MgO / $\text{Co}_{90}\text{Fe}_{10}$ interface.

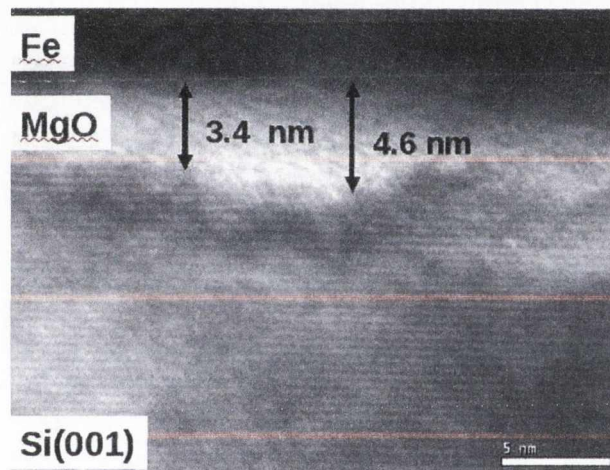
4.3 $\text{Co}_{90}\text{Fe}_{10}$ on n-type Gallium Arsenide substrates

4.3.1 Introduction

As seen from Chapter 3 it was the mid n-type GaAs semiconductor substrate which gave the best example of rectifying electrical transport and so this was the substrate used in these experiments. The AlO_x and MgO films were once again deposited onto the GaAs substrates orientated in the (001) direction using Chamber B of the Shamrock sputtering system. The growth parameters used here are the same as was used in the previous section to ensure as similar barriers as possible for the different substrates. They were



(a)



(b)

Figure 4.30: (a) TEM and (b) HRTEM images of 10 nm Ta / 20 nm Fe / 4 nm MgO / Si(001). The panel in the right of part (a) is digitally modified image with a reduced lateral dimension.

grown from two very high purity targets arranged in a target facing target configuration, which were sputtered using an RF power supply in Ar pressures of 4.3×10^{-3} Torr and 3.9×10^{-3} Torr for AlO_x and MgO respectively. Once the tunnel barriers were deposited the substrates were moved to Chamber A of the sputtering system for the 20 nm $\text{Co}_{90}\text{Fe}_{10}$ film deposition and 5 nm Ta layer capping layer. Both films were again deposited in an Ar pressure of 4×10^{-3} Torr to ensure similar films to the ones used in the previous

section. The bare GaAs substrates were packed in an inert atmosphere and once opened were placed directly into the vacuum chamber, eliminating the need for etching. These junctions were also patterned into two different sizes, $50 \times 50 \mu\text{m}$ using UV lithography and circular junctions of approximately 100 nm in diameter, keeping them the same as the junction sizes used in the Si junction systems. A Au top contact was sputtered after top contact patterning using UV lithography for both junction sizes in Chamber A and again in an Ar pressure of 4×10^{-3} Torr. AuGe back contacts were thermally evaporated onto the back of the GaAs substrates and annealed in air at 300 °C for about a minute after film stack deposition but before lithographic patterning.

Again the carrier concentration of the substrate was confirmed using room temperature Hall effect and resistance measurements as outlined in Chapter 2. The result yielded a carrier concentration of $6.3 \times 10^{17} \text{ cm}^{-3}$ and a resistivity, ρ , of $1.2 \times 10^{-2} \Omega\text{cm}$, which is, again, in good agreement with previous measurements on similar substrates used in Chapter 3. The substrates were doped with Si and the depletion region width was approximated as 37.1 nm wide using equation 4.1. The value used for ϵ_r was 13.1 [13]. The depletion region for this semiconductor substrate is much narrower than the Si depletion region due to the higher carrier concentration.

The transport measurements were performed as a function of temperature and barrier thickness. For the $50 \times 50 \mu\text{m}$ sized junctions the barrier thickness went from 0 nm to 6 nm in 1 nm steps. For the 100 nm sized junctions the barrier thickness varied from 0 nm to 4 nm in 1 nm steps. All transport measurements were performed using the cryostat part of the resistivity rig outlined in Chapter 2.

4.3.2 Film Structure

Figure 4.31 shows an x-ray diffraction scan of only 3 nm of MgO sandwiched between a GaAs (001) substrate and 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ capped with 5 nm of Ta. Note the presence of a small MgO (002) peak despite how thin the MgO layer is, only 3 nm, and is under 25

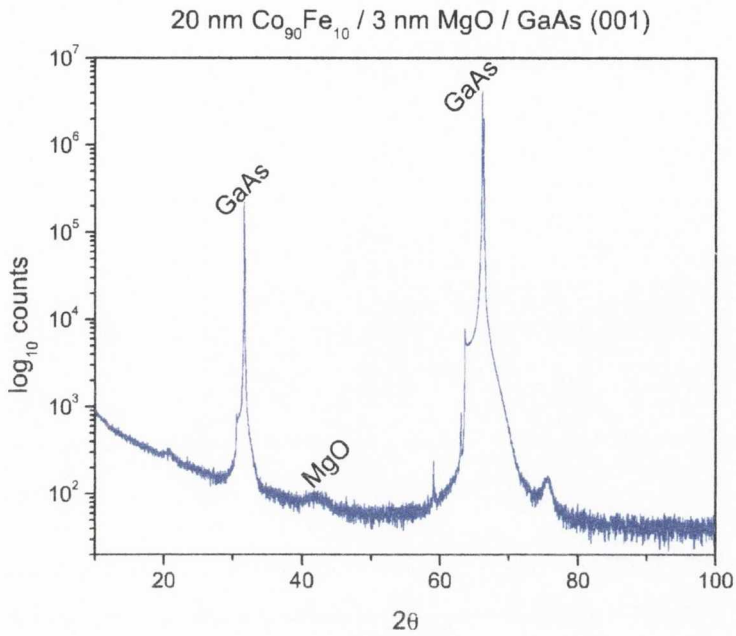


Figure 4.31: X-ray diffraction graph of 5 nm Ta / 20 nm $\text{Co}_{90}\text{Fe}_{10}$ / 3 nm MgO / GaAs (001). Even though the MgO layer is extremely thin, only 3 nm, the MgO (002) peak can still be made out.

nm of metal. The presence of this peak indicates that exceptionally well orientated MgO films are grown on the GaAs (001) substrates, much better than those grown on either Si substrate. As mentioned earlier well orientated MgO acts as a spin filter, allowing one type of spin through. The high quality MgO growth here may form “channels” that aid the transport of one spin type through the barrier. This presents very exciting possibilities for the use of these systems in spintronic devices.

4.3.3 Electrical Transport, $50 \times 50 \mu\text{m}$ sized Junctions

Figures 4.32 to 4.35 and 4.36 to 4.39 show the $I - V$ measurements for $\text{Co}_{90}\text{Fe}_{10}$ on GaAs with 0 to 3 nm of AlO_x and MgO tunnel barriers between the $\text{Co}_{90}\text{Fe}_{10}$ and GaAs respectively. The data is in 25 K intervals between 50 K and 300 K. And once again despite the presence of a tunnel barrier the curves still display an asymmetric voltage

dependence similar to the results seen in the $\text{Co}_{90}\text{Fe}_{10}$ / insulator / Si systems and much the same as discussed in Chapter 3.

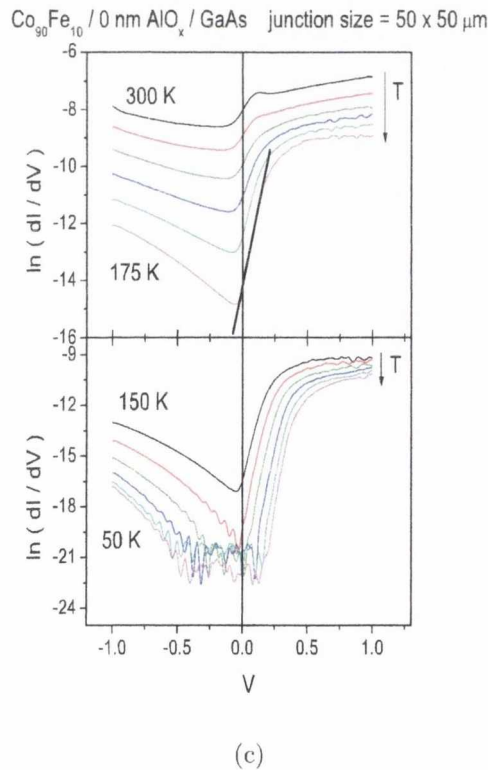
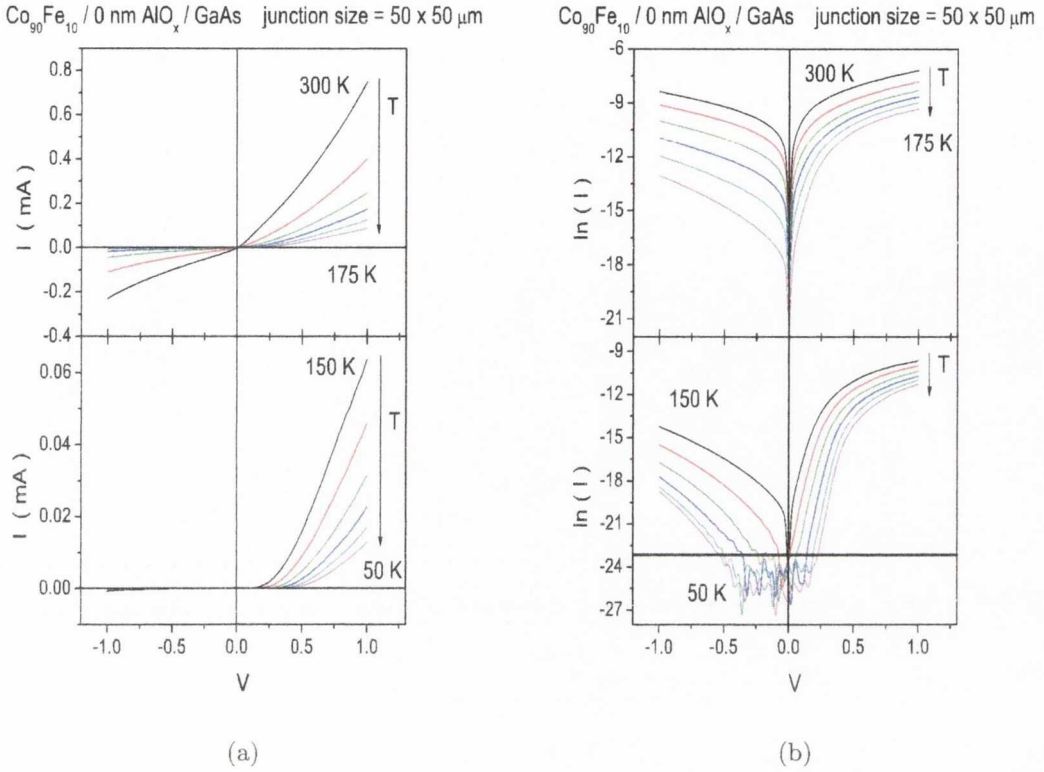


Figure 4.32: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs (001) with 0 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

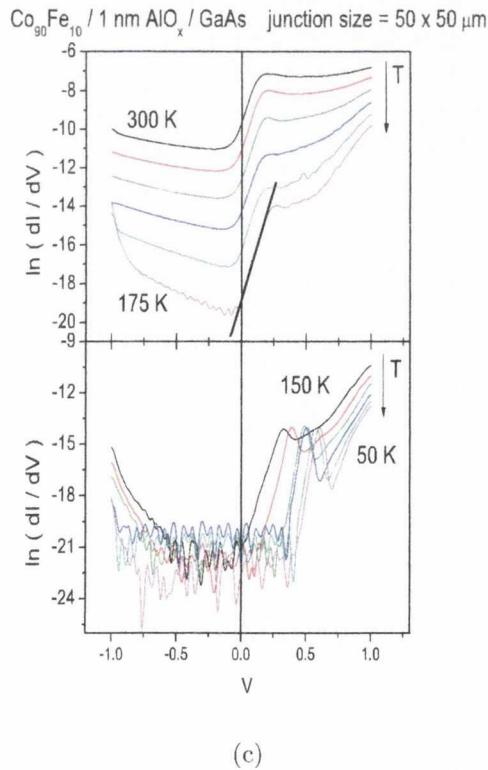
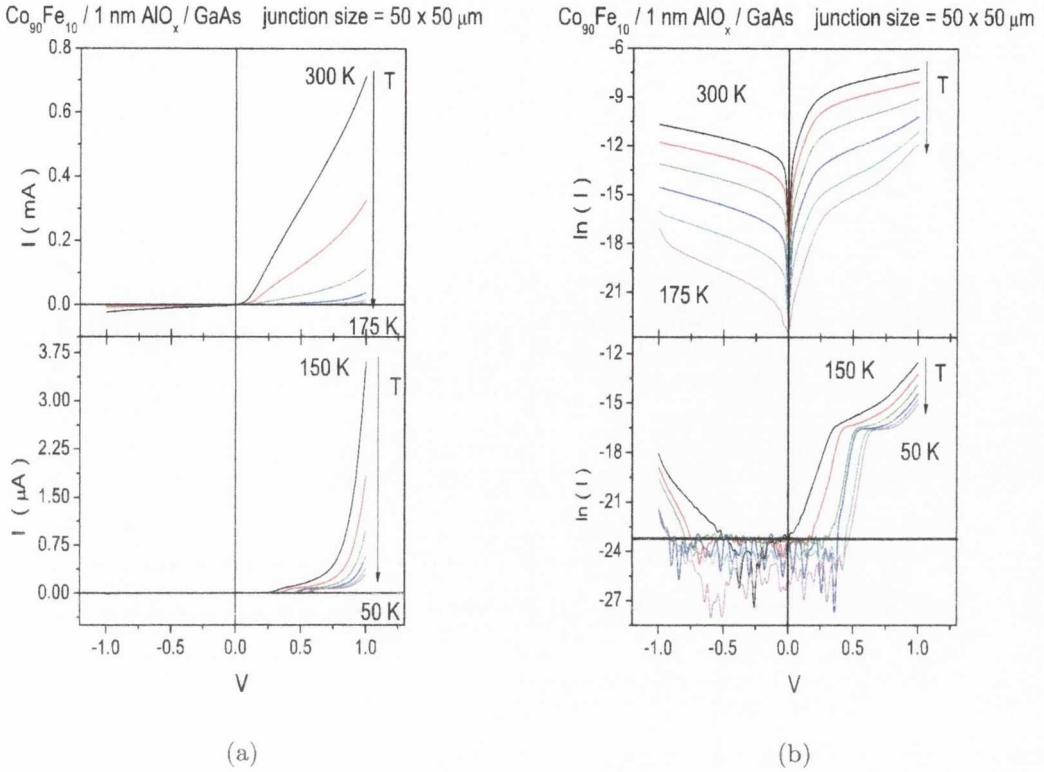


Figure 4.33: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on GaAs (001) with 1 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1 \text{ nA}$), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

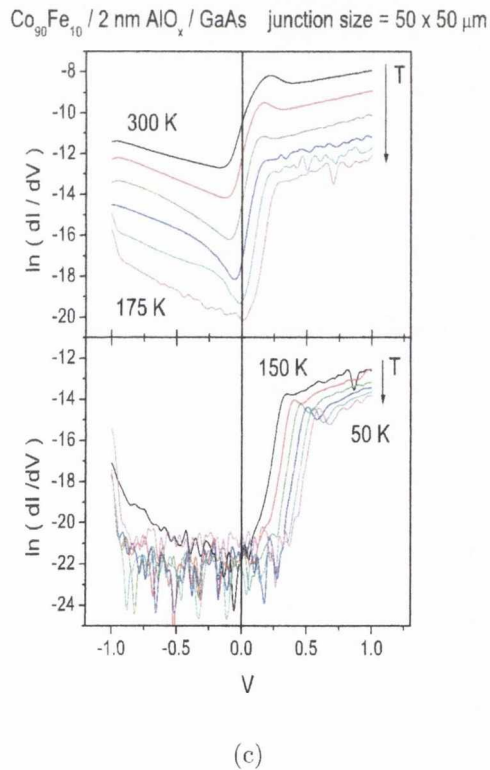
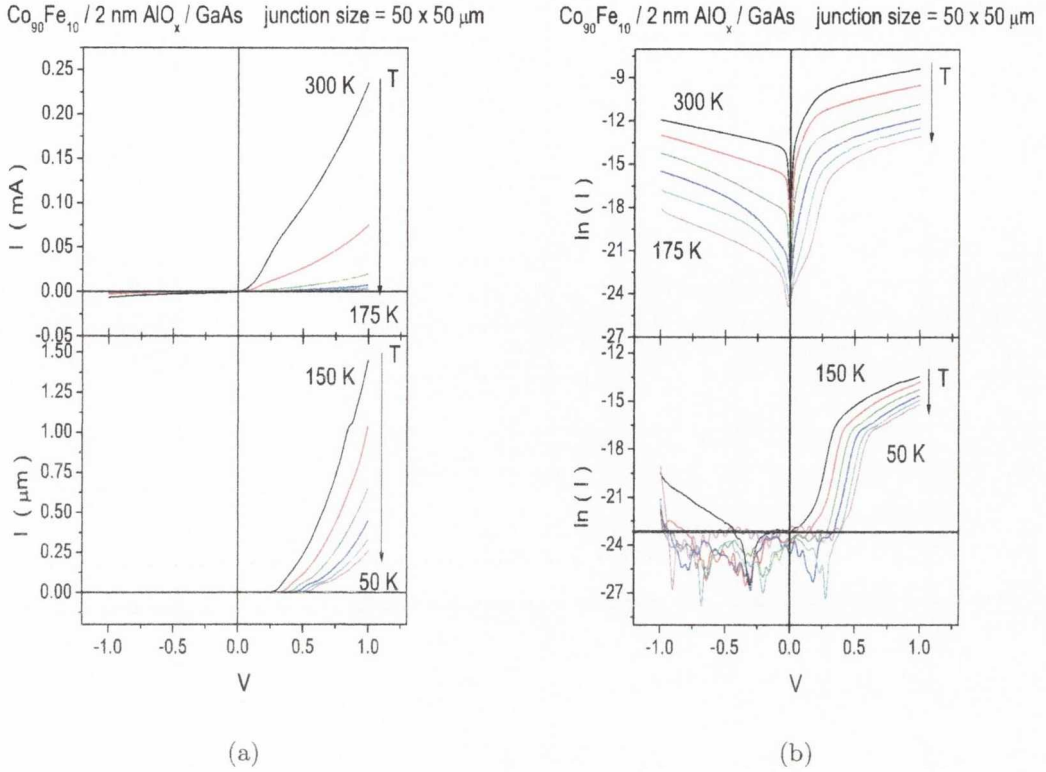
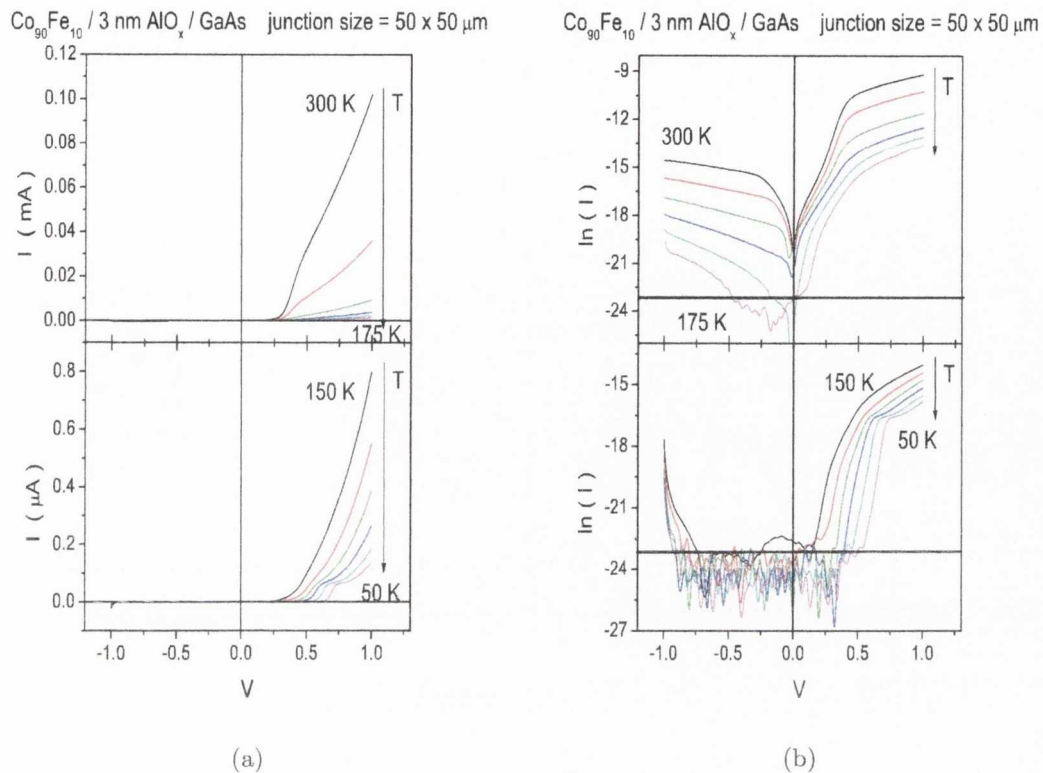


Figure 4.34: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on GaAs (001) with 2 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1 \text{ nA}$), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .



$\text{Co}_{90}\text{Fe}_{10} / 3 \text{ nm AlO}_x / \text{GaAs}$ junction size = $50 \times 50 \mu\text{m}$

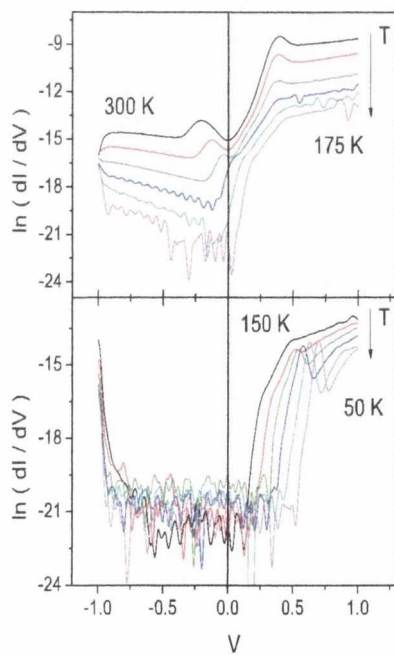


Figure 4.35: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on GaAs (001) with 3 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1 \text{ nA}$), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

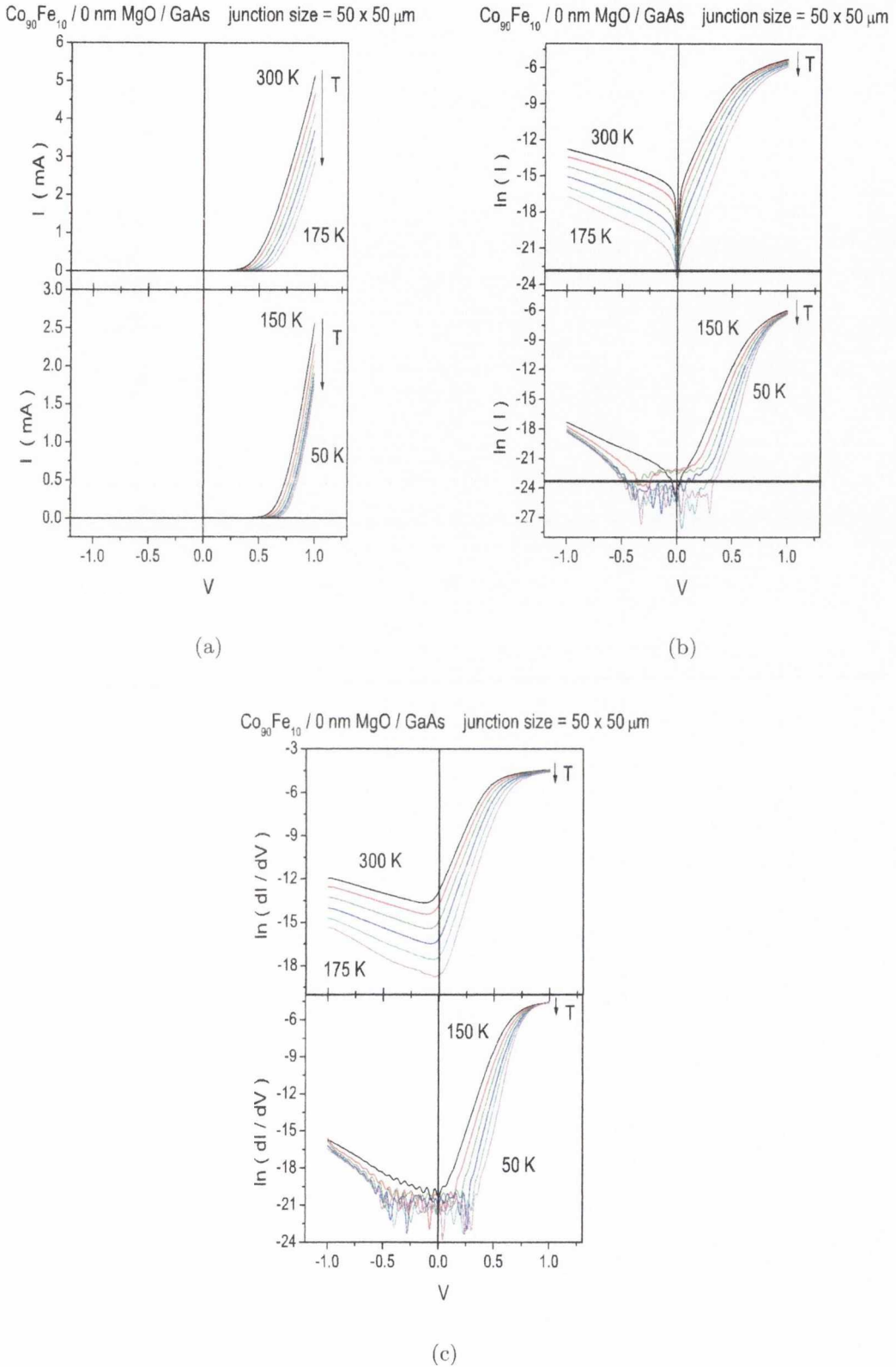


Figure 4.36: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs (001) with 0 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

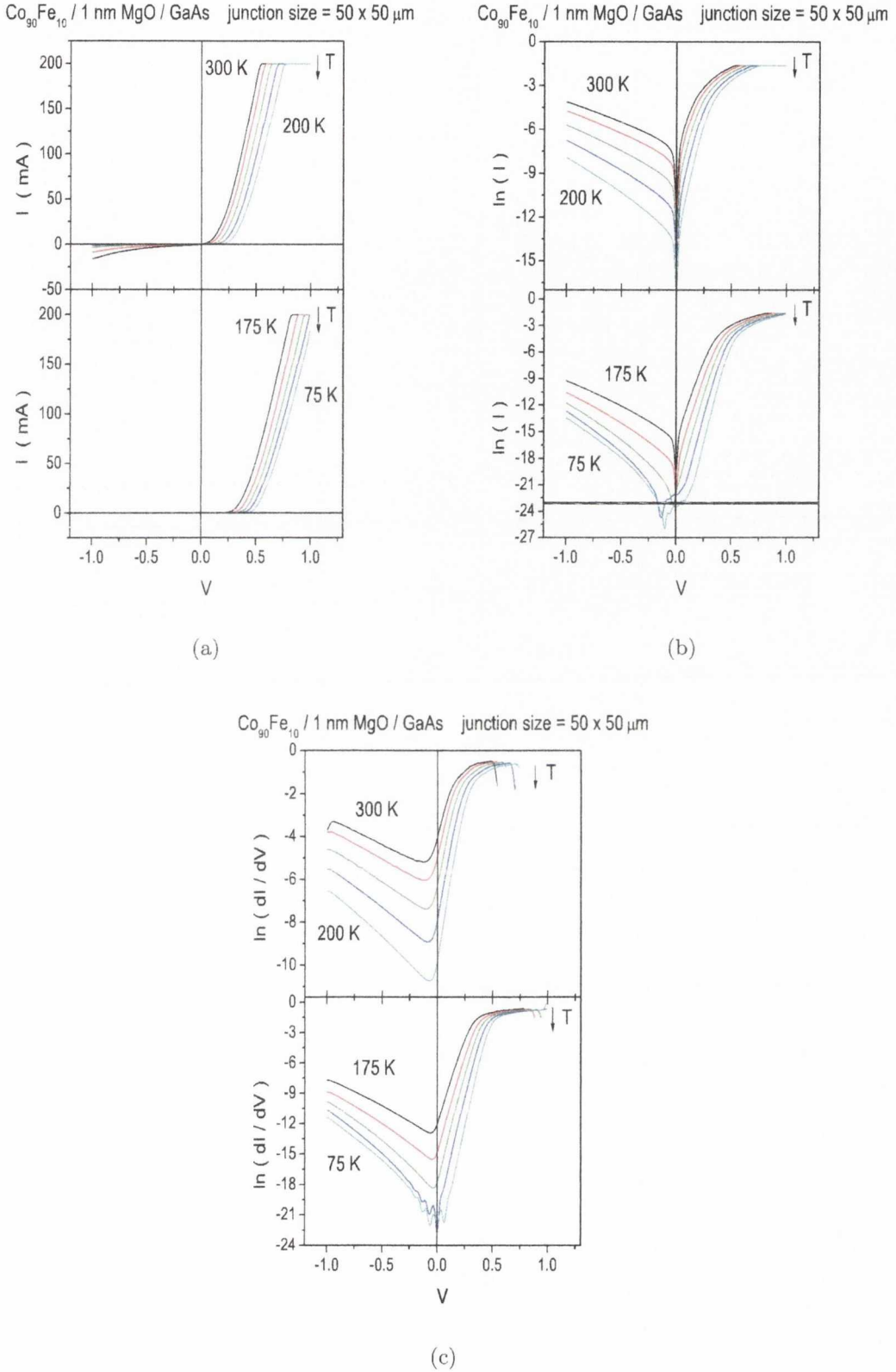
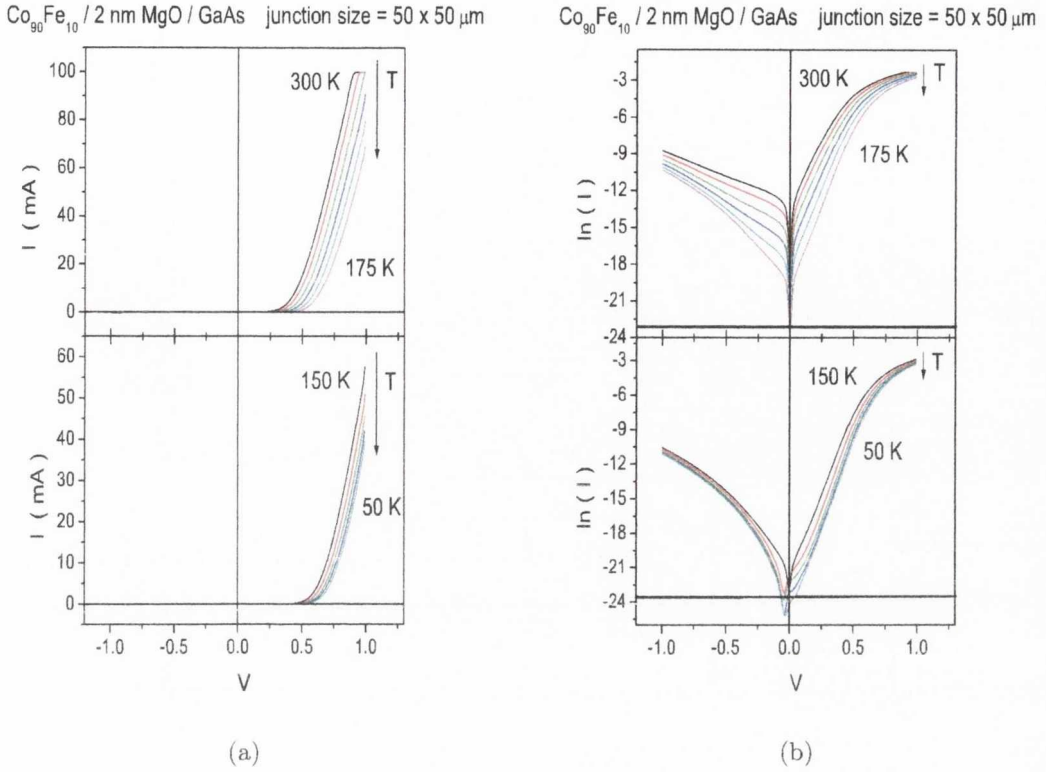


Figure 4.37: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs (001) with 1 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .



Co₉₀Fe₁₀ / 2 nm MgO / GaAs junction size = 50 x 50 μm

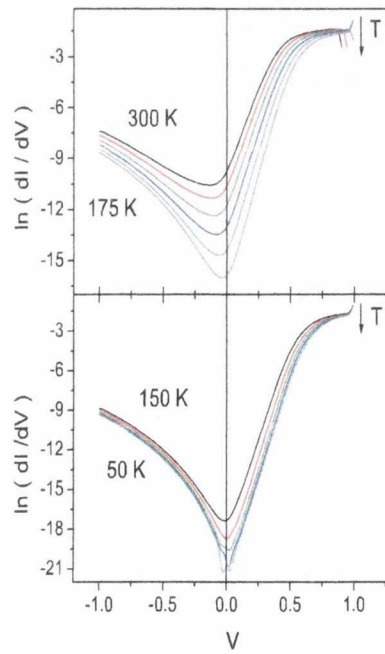


Figure 4.38: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs(001) with 2 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

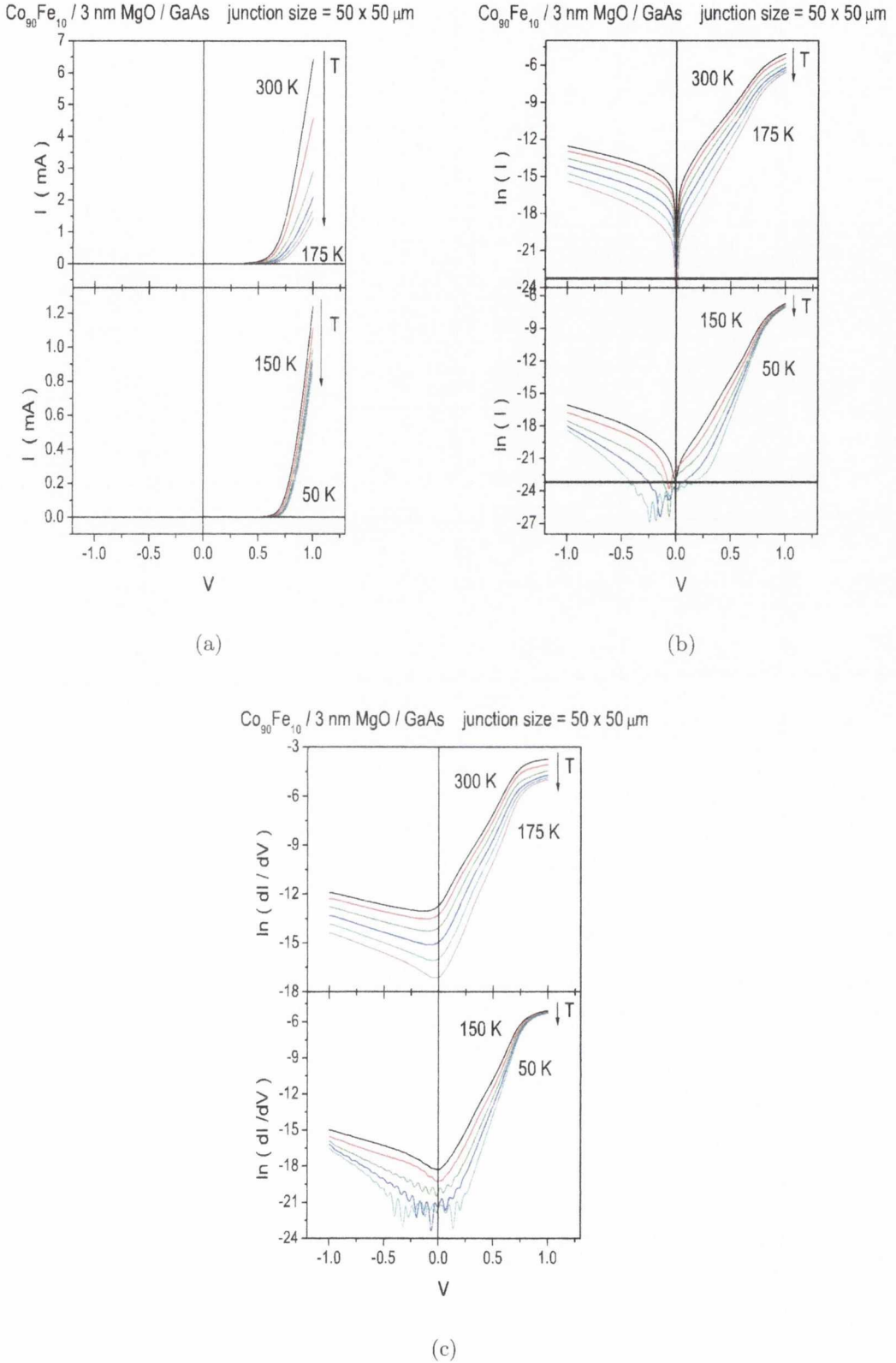


Figure 4.39: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs(001) with 3 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

The three distinct temperature regimes which were identified in all previous junctions are changed somewhat for the GaAs systems. For the $\text{Co}_{90}\text{Fe}_{10} / \text{AlO}_x / \text{GaAs}$ they are still clearly there although somewhat shifted. The low temperature regime, where the curves become fully symmetric at low bias, is now from $T \leq 100$ K for the $\text{Co}_{90}\text{Fe}_{10} / \text{GaAs}$ junction and from $T \leq 150$ K once the AlO_x tunnel barrier has been introduced. The intermediate temperature range where the curves are asymmetric is now from $125 \text{ K} \leq T \leq 200 \text{ K}$ where there is no AlO_x in the junction and rises to $175 \text{ K} \leq T \leq 250 \text{ K}$ for the junctions with an AlO_x barrier present. At higher temperatures the reduced asymmetry between forward and reverse bias is more obvious here in the GaAs substrate systems than it was for the Si system junctions, $T \geq 225 \text{ K}$ and $T \geq 275 \text{ K}$ for the junctions with no tunnel barrier and with a tunnel barrier respectively. Again in the low temperature regimes the bias range over which the curves are symmetric increases as the tunnel barrier thickness increases, indicating tunneling as the dominant mode of electrical transport across the interfaces. For the junctions where MgO is the tunnel barrier the temperature regimes are much more difficult to identify. The junction where there is no MgO is the same as the junction with no AlO_x .

On the introduction of an MgO tunnel barrier something remarkable happens, there is a huge increase in current through the junction. It is so large when 1 nm of MgO is introduced that it hit the compliance current limit on the Keithly 2400 used to supply the voltage and measure the current. This is a limit that can be set and is usually set to 100 mA to prevent damage to the junction in case of a current spike. It was increased to 200 mA when measuring these junctions but even then the current reached the limit. This is the flat bit at the end of the forward bias curve in part (a), figure 4.37. Such a high current continues until $T \leq 75 \text{ K}$. Even though there is an increase in the reverse bias current, there is no low temperature region where the data is symmetric, no matter how low a bias is focused on. When the MgO thickness is increased to 2 nm the current is reduced from the level it reached when it was 1 nm thick but it is still much higher

than having no barrier. Strangely the low temperature region, being defined as the region where the curves have symmetry at low bias, is much increased as the reverse bias current does not decrease with decreasing temperature to the same extent as the forward bias current does. This region is now from $T \leq 175$ K. In fact, while at higher temperatures the reverse bias current is greater for the 1 nm MgO junction than it is for the 2 nm MgO junction, as the temperature decreases this changes. From $T \leq 150$ K the 2 nm reverse bias current is significantly larger than the reverse bias current in the 1 nm junction, parts (b) in figures 4.37 and 4.38. When the barrier is increased to 3 nm the current in both directions is again reduced and continues to reduce as the temperature decreases. But again there is no obvious low temperature regime to be seen in the curves, figure 4.39.

Figures 4.40 and 4.41 are plots of the $\ln(I)$ versus the barrier thickness so that the effect on current of incorporating a tunnel barrier can be observed directly. From these figures it can be seen that as soon as an AlO_x tunnel barrier is introduced the current starts to decrease, in both the forward and reverse bias directions. On the other hand when MgO is introduced there is a massive increase in both the forward and reverse directions. The increase in the reverse bias current is larger than the increase in the forward bias current.

In figure 4.41 oscillations in the data can be seen as the MgO barrier thickness increases. The origin of these oscillations is unclear but it is thought that they might be due to quantum confinement in the tunnel barrier at the semiconductor interface. The oscillations are not seen in any other system containing MgO studied.

The distortion in the shape of a typical rectifying curve when a thin tunnel barrier is placed between the metal and semiconductor is best seen in the $\text{Co}_{90}\text{Fe}_{10} / \text{AlO}_x / \text{GaAs}$ plots, figures 4.33 to 4.35 and is particularly exaggerated at lower temperatures. Since rectifying behaviour has been observed for the junctions in this section they were fitted in the forward bias region to the thermionic emission/ diffusion model once again to determine the Schottky barrier height of each junction. An active area, A_e of 2.5×10^{-9}

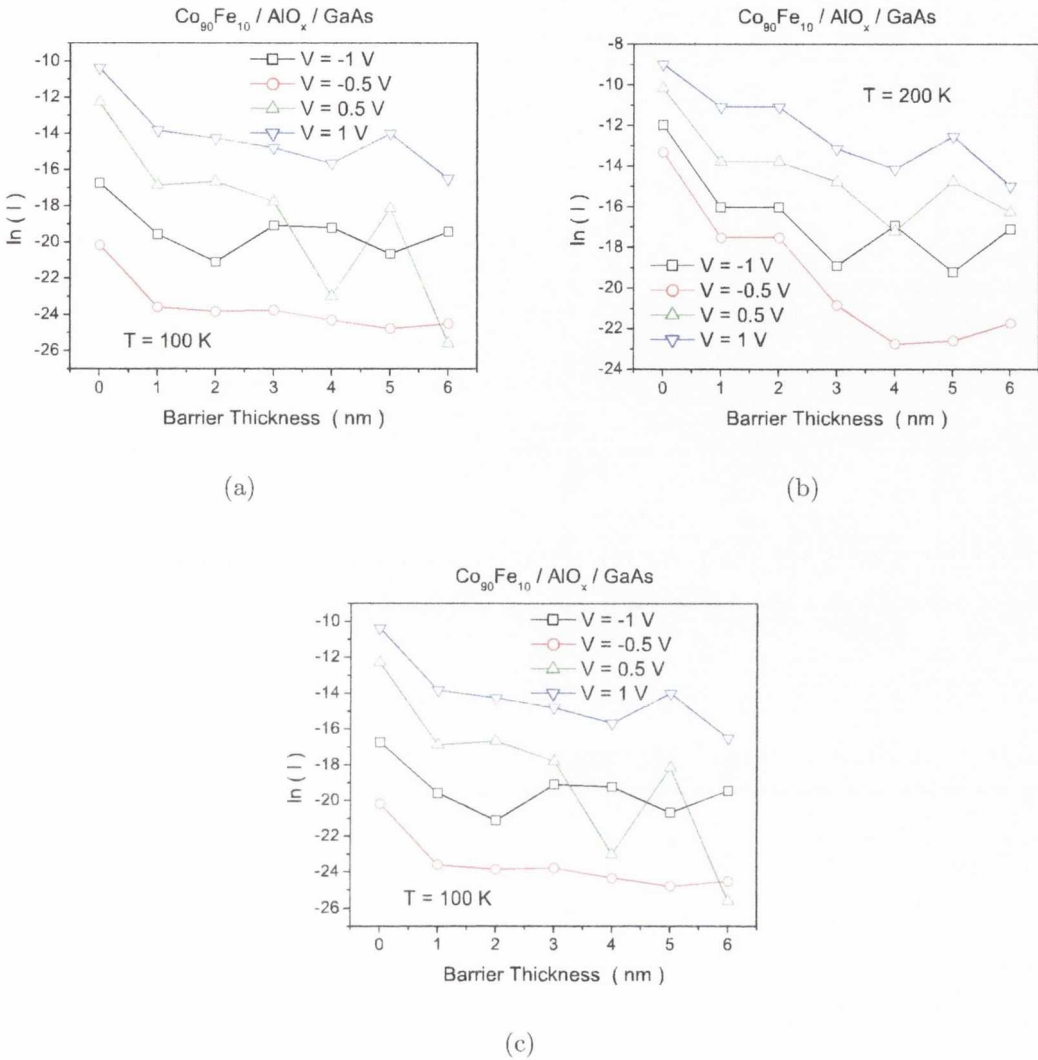


Figure 4.40: Plots of $\ln(I)$ vs. AlO_x barrier thickness on GaAs substrates at (a) 300 K, (b) 200 K and (c) 100 K. The current values are taken for voltages that are -1 V, -0.5 V, 0.5 V and 1 V. Junction size is $50 \times 50 \mu\text{m}$.

m^2 , which every junction has been patterned to be, and an effective Richardson constant, A^{**} , of $8.2 \text{ Acm}^{-2}\text{K}^{-2}$ [2] are used. The results are shown in table 4.2.

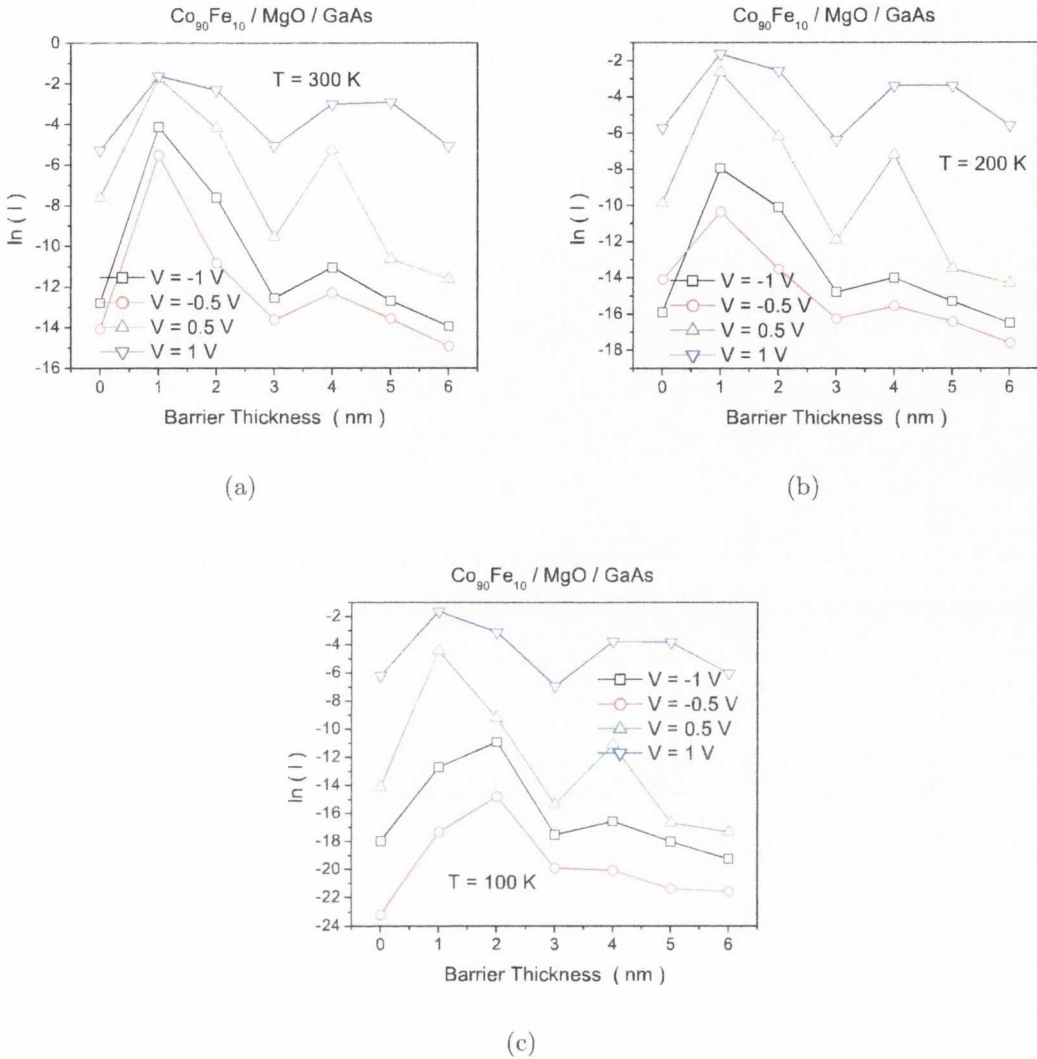


Figure 4.41: Plots of $\ln(I)$ vs. MgO barrier thickness on GaAs substrates at (a) 300 K, (b) 200 K and (c) 100 K. The current values are taken for voltages that are -1 V, -0.5 V, 0.5 V and 1 V. Junction size is $50 \times 50 \mu\text{m}$.

4.3.4 Electronic Transport, 100 nm Junctions

Figures 4.42 to 4.45 and 4.24 to 4.27 show the $I - V$ measurements for $\text{Co}_{90}\text{Fe}_{10}$ on GaAs with 0 to 3 nm of AlO_x and MgO tunnel barriers between the $\text{Co}_{90}\text{Fe}_{10}$ and Si respectively. The data is in 25 K intervals between 50 K and 300 K.

Material	Thickness in nm	ϕ_B in eV	n	T in K
	0	0.28	2.92	175
		0.27	2.95	150
AlO _x	1	0.37	2.70	200
		0.39	2.26	250
AlO _x	2	0.43	1.88	250
AlO _x	3	0.47	3.15	250
	0	0.40	2.52	200
MgO	1	0.26	1.86	225
MgO	2	0.36	2.24	225
MgO	3	0.41	3.66	225
MgO	4	0.39	2.12	225
MgO	5	0.54	2.09	225
MgO	6	0.45	4.11	225

Table 4.2: The barrier heights, ϕ_B , and ideality factors, n , for all junctions fabricated in the μm size on GaAs.

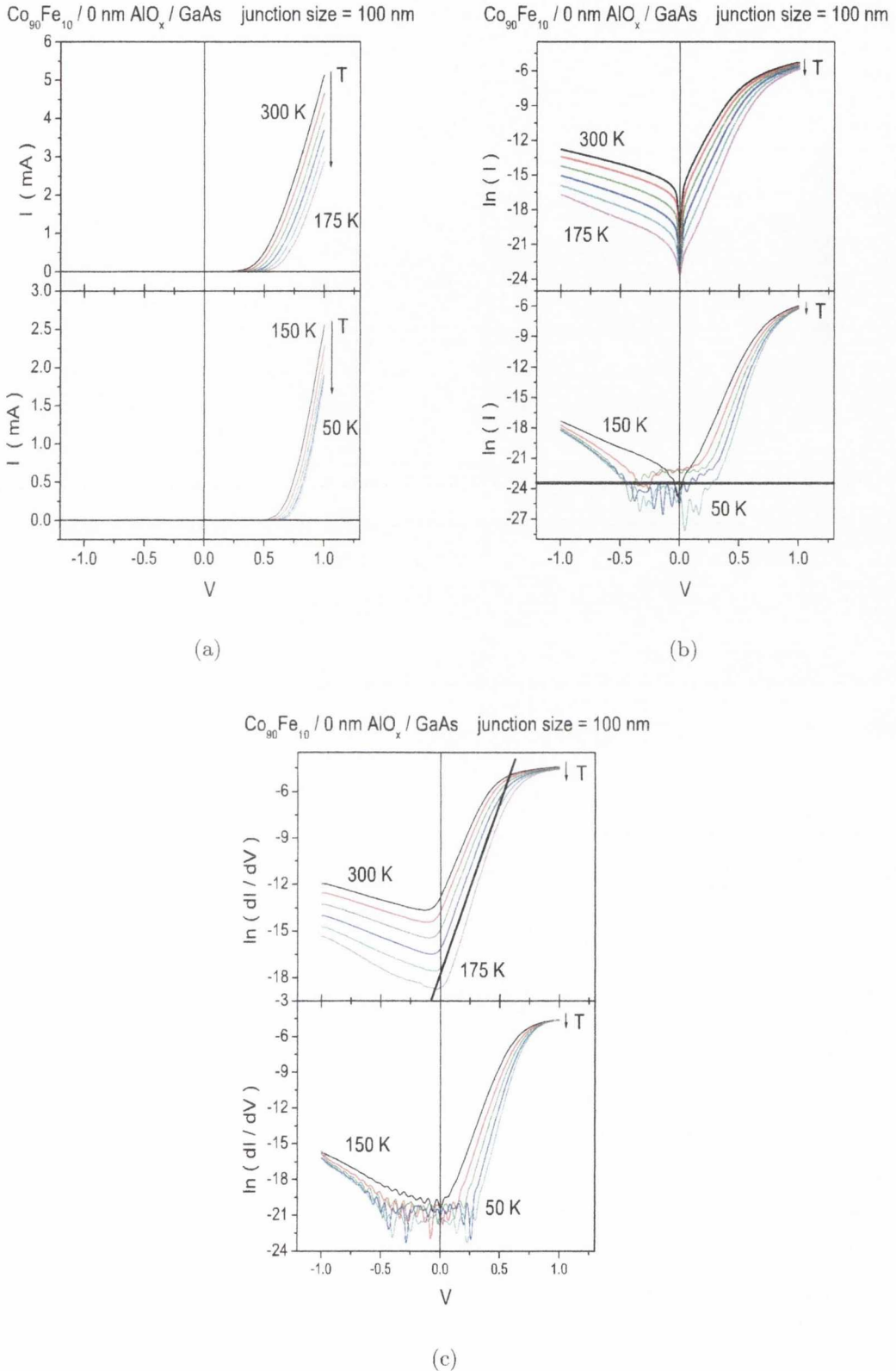


Figure 4.42: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on GaAs (001) with 0 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V , the black line is the fit in order to determine the barrier height, ϕ_B .

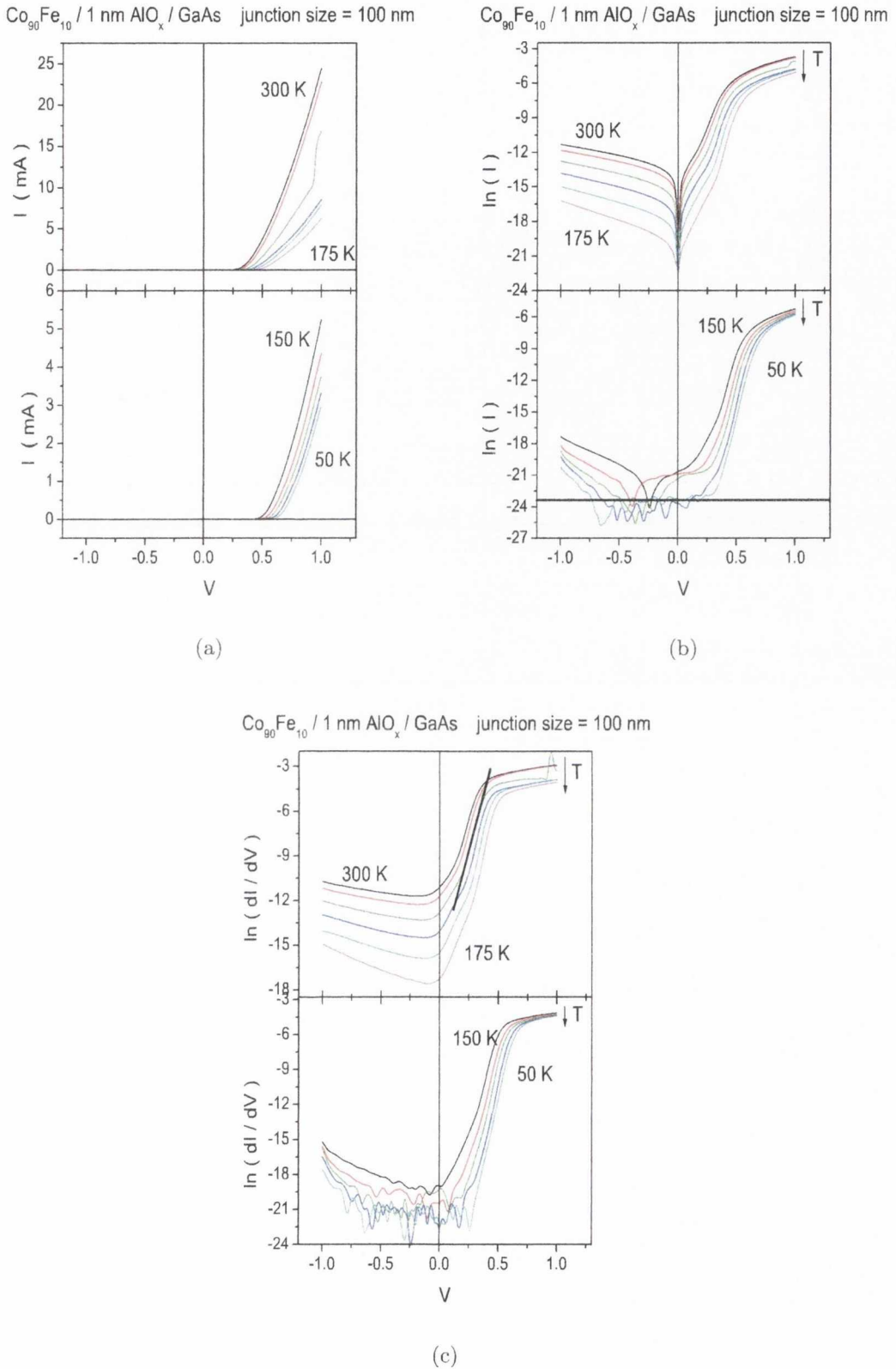


Figure 4.43: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on GaAs (001) with 1 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1 \text{ nA}$), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

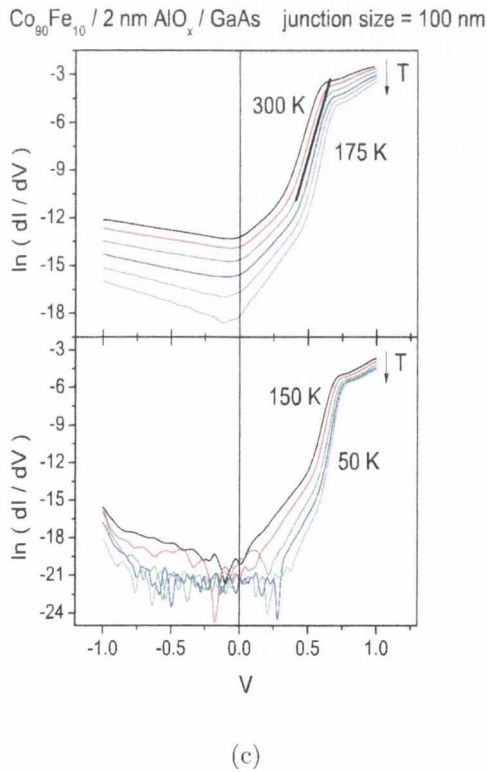
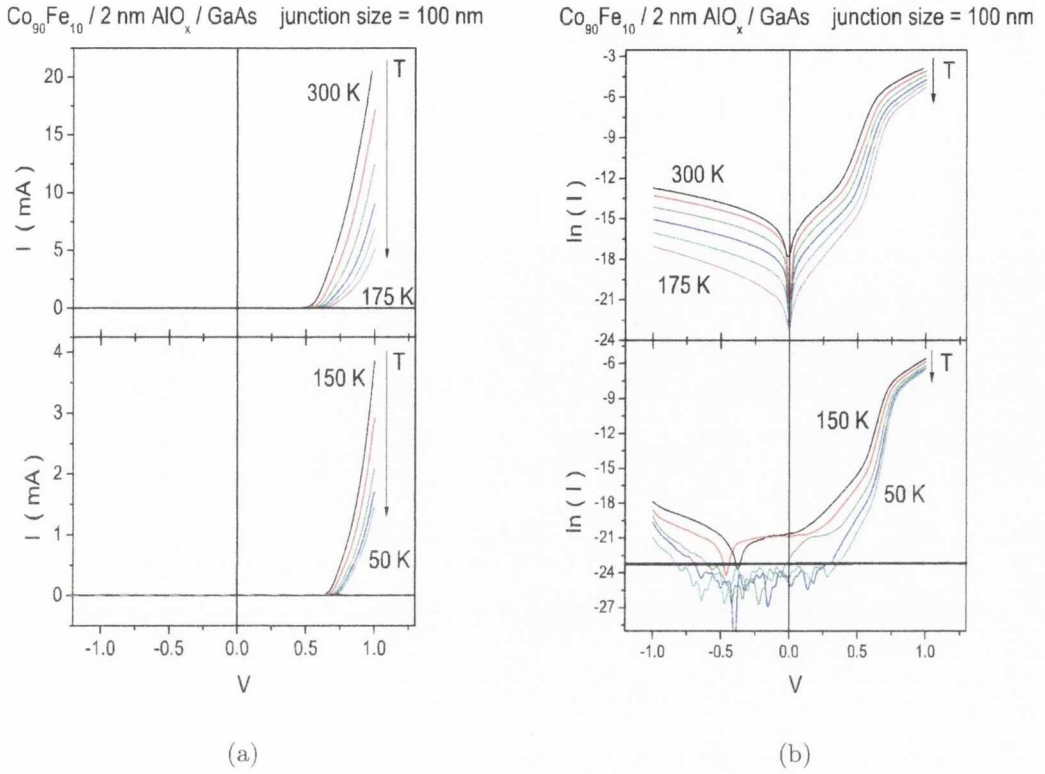


Figure 4.44: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs (001) with 2 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

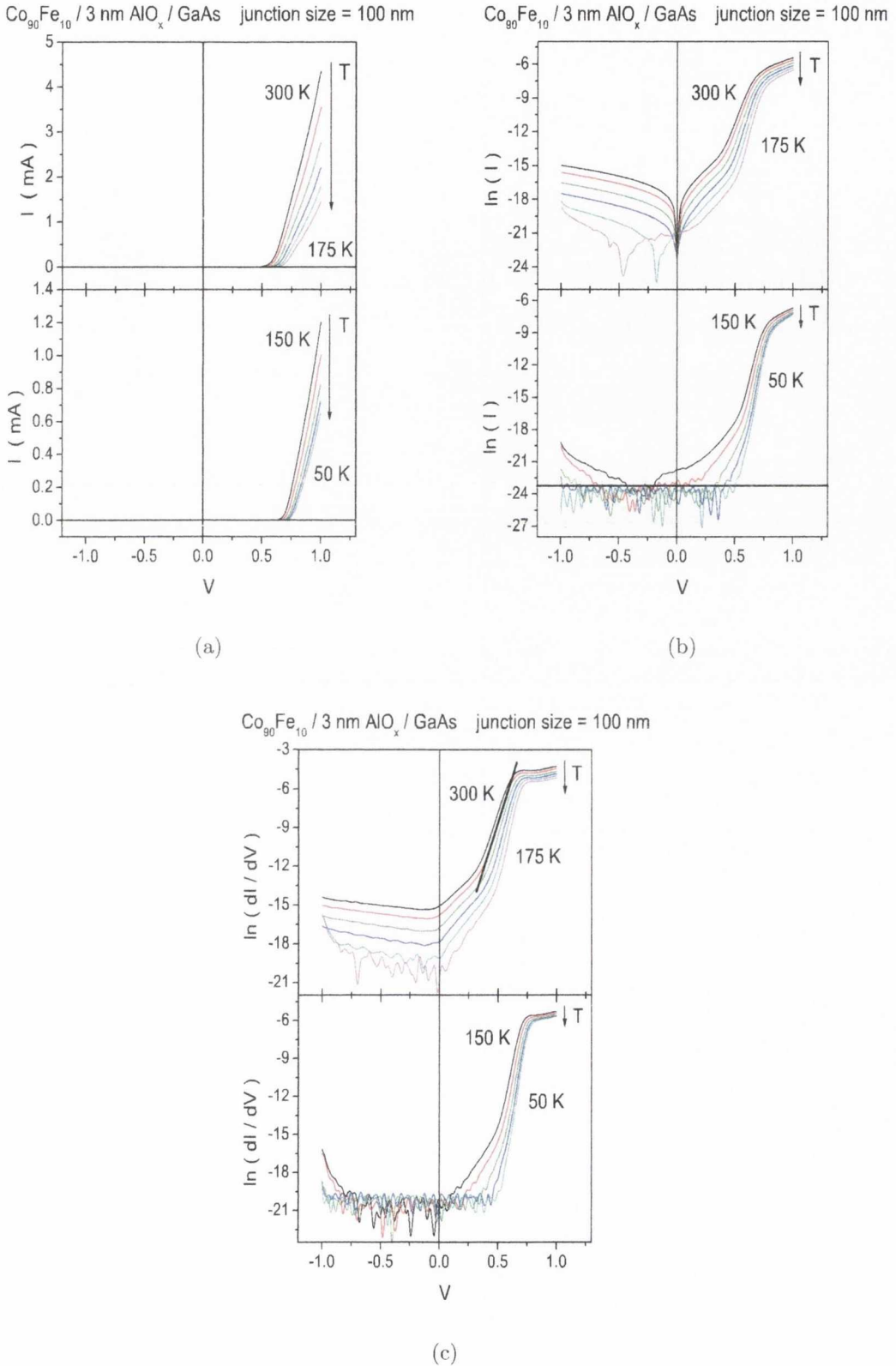


Figure 4.45: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs (001) with 3 nm of the tunnel barrier AlO_x between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current ($I > 0.1$ nA), current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

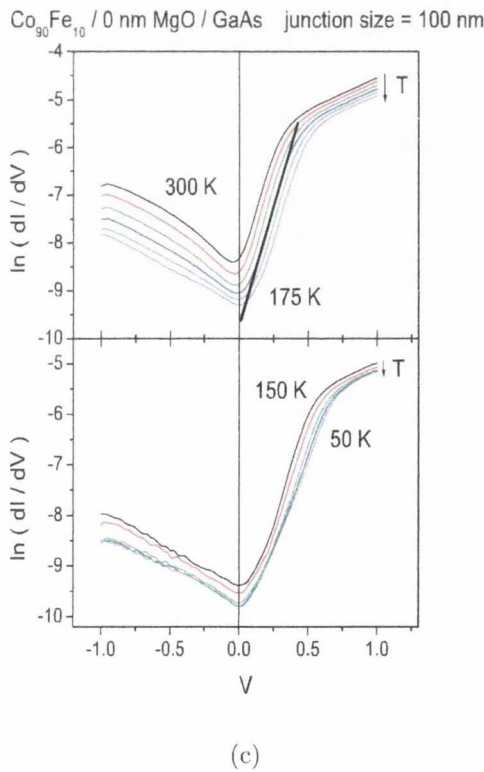
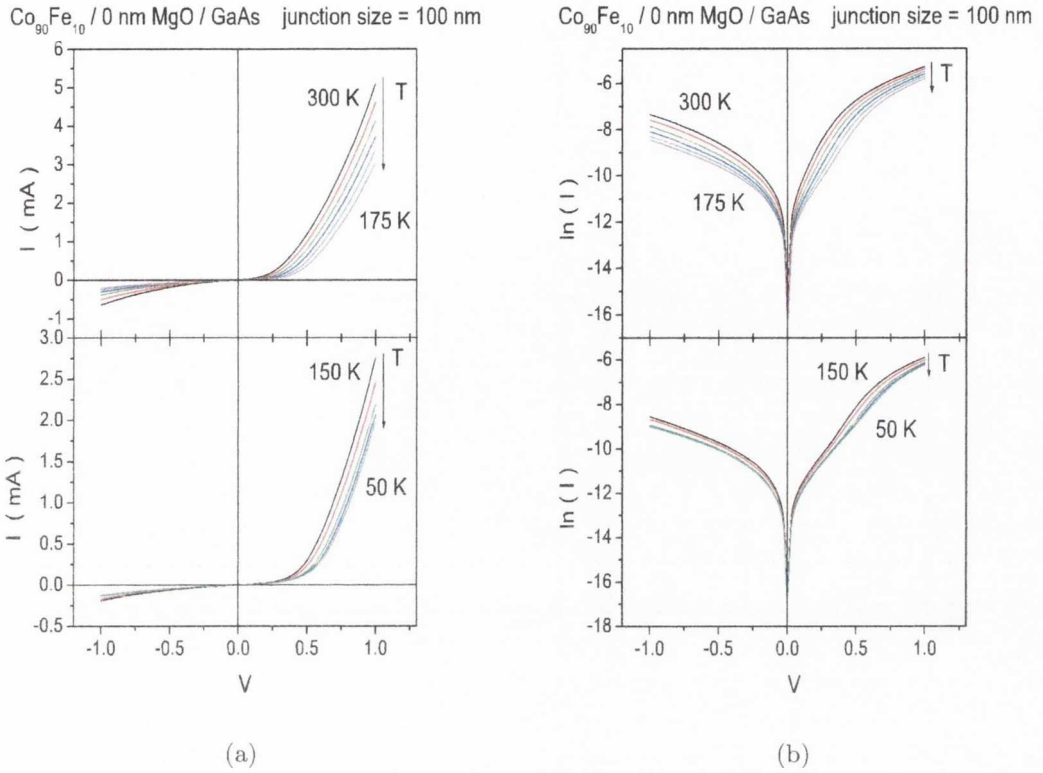


Figure 4.46: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs (001) with 0 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V and (c) $\ln(dI/dV)$ vs. V .

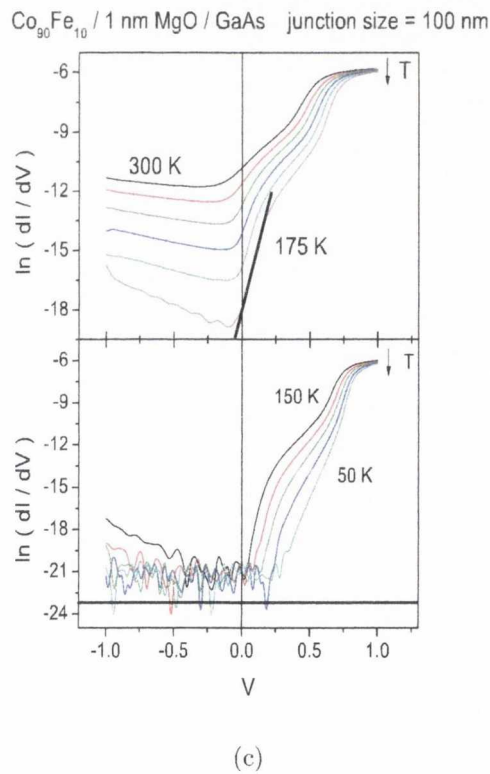
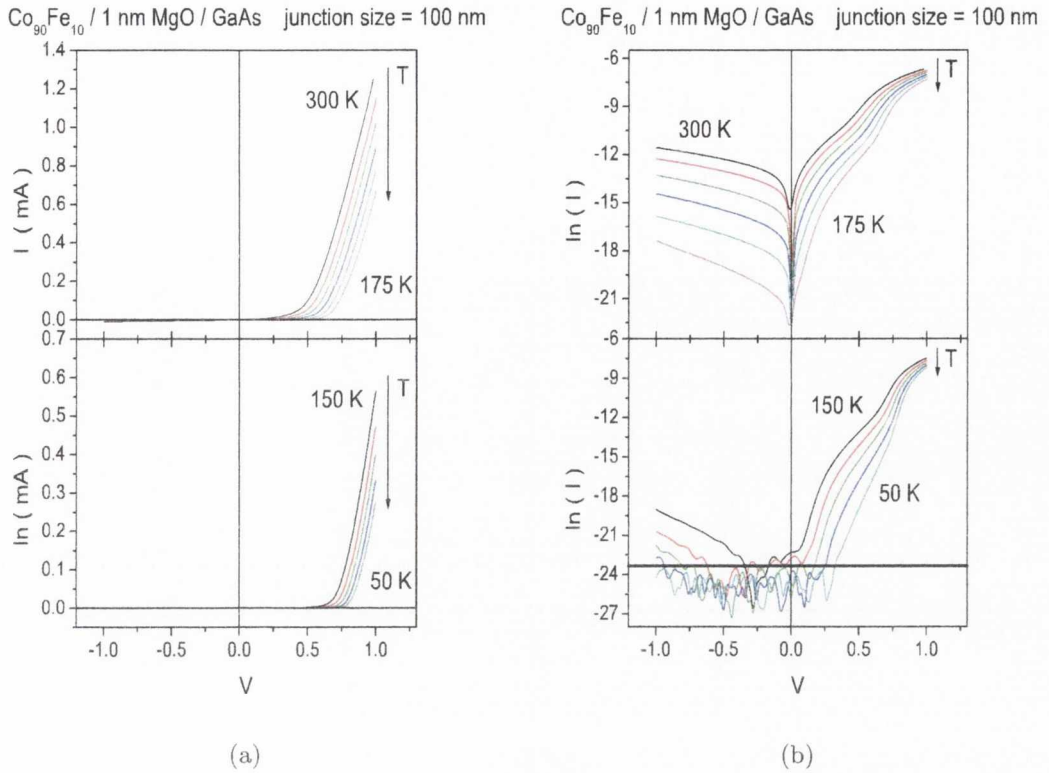


Figure 4.47: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs (001) with 1 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current, current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

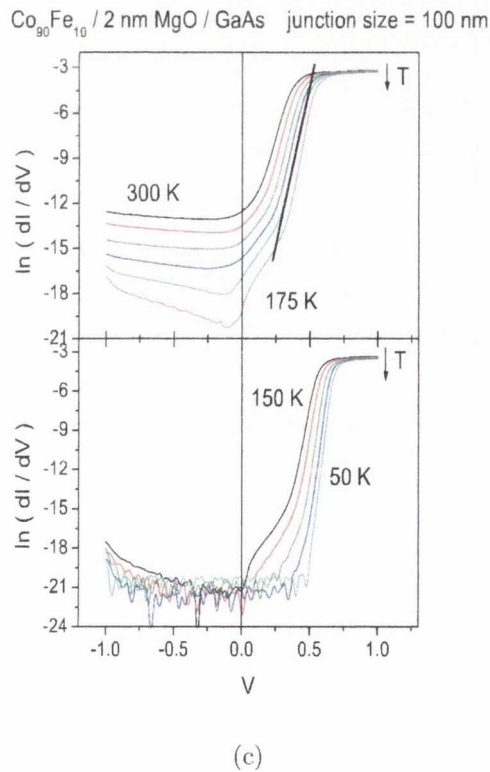
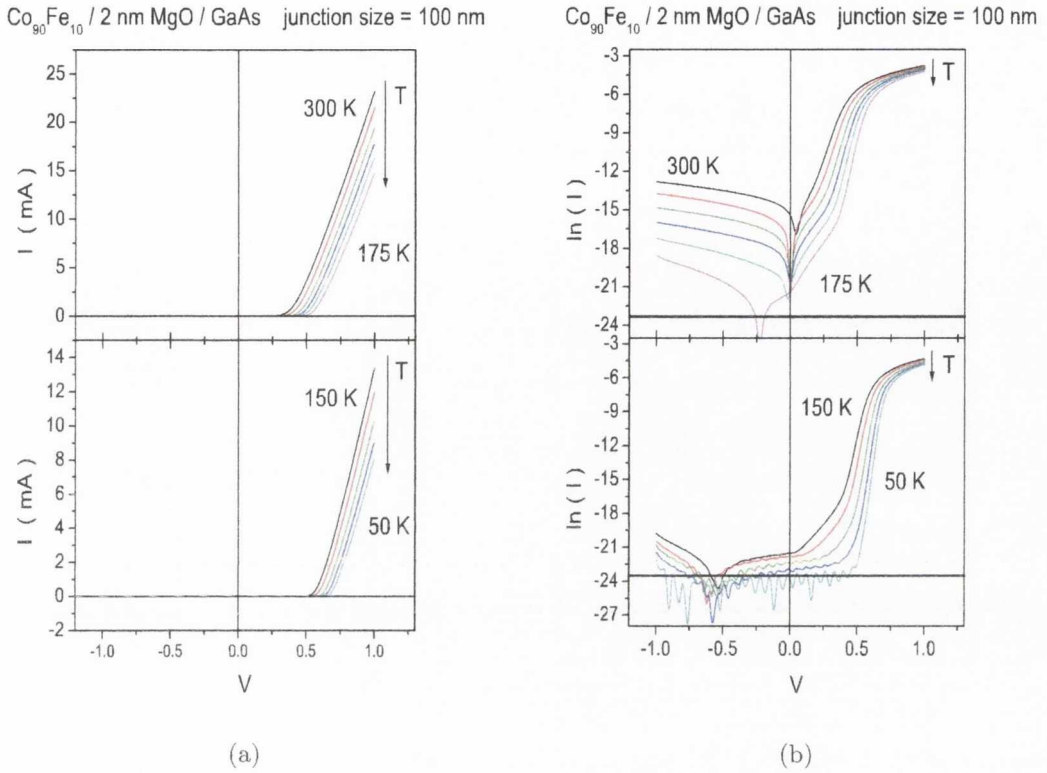


Figure 4.48: $I - V$ measurements of 20 nm of $\text{Co}_{90}\text{Fe}_{10}$ on GaAs (001) with 2 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current, current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

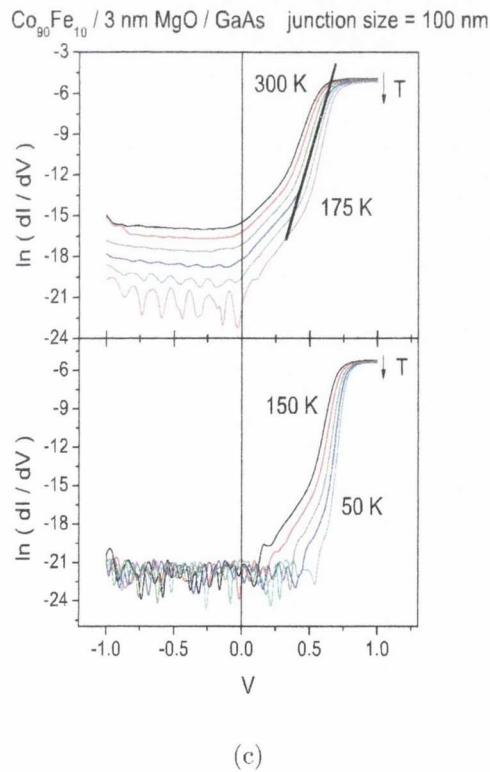
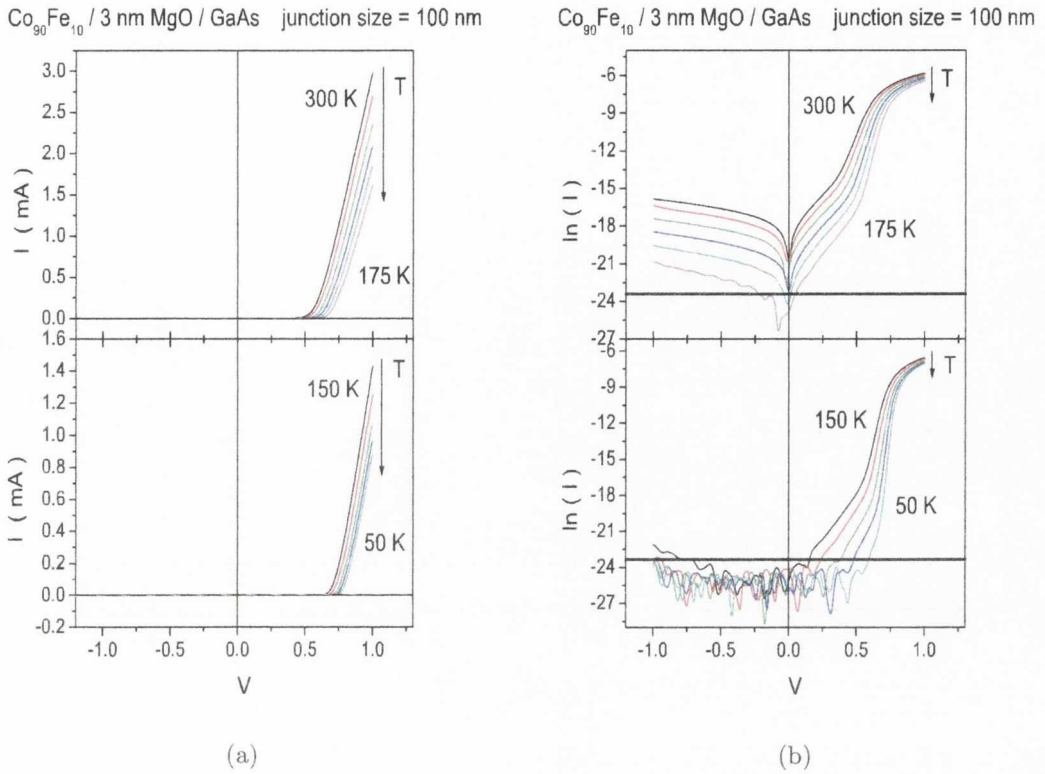


Figure 4.49: $I - V$ measurements of 20 nm of Co₉₀Fe₁₀ on GaAs (001) with 3 nm of the tunnel barrier MgO between them. The data is plotted as (a) I vs. V , (b) $\ln(I)$ vs. V , the black line here indicates the cut-off point for the measurable current, current below this line is in the error margin of the Keithly, and (c) $\ln(dI/dV)$ vs. V .

Where there is no tunnel barrier present, figures 4.42 and 4.46, there is quite a large reverse bias current until $T \leq 200$ K. This is very similar to the situation for the micro scale junctions. Below this temperature the curves are asymmetric and can be fitted to the thermionic emission / diffusion model, equations 4.2 and 4.4. With the introduction of 1 nm of a tunnel barrier the high temperature curves become asymmetric. However there is a slight distortion in the small forward bias region of the curve due to the tunnel barrier, and again regardless of tunnel barrier material, which extends in bias as the temperature decreases. part (b), figure 4.43.

For the AlO_x junctions it is the area immediately after that which is fitted with the model, as it is free from the tunneling effect, the fit line in part (c) figures 4.43 to 4.45. As the AlO_x thickness increases this distortion increases. Also with the inclusion of a tunnel barrier there is a huge increase in the current under forward bias, which is affected only marginally by the decrease in temperature. The current increase decreases when the barrier is 3 nm thick but it is still larger than the forward bias current when there is no barrier. It is more difficult to tell from these graphs what the effect on the reverse current is and so once again a plot of the current versus the barrier thickness is included, figure 4.50. These graphs confirm the increase in current under forward bias when 1 nm of AlO_x is included in the system but it is not maintained as the thickness increases. In reverse bias the current mainly decreases when the barrier is introduced and continues decreasing as thickness increases.

For the forward bias current when 1 nm of MgO is introduced the current increases only slightly but when the thickness is 2 nm a much bigger current increase is observed. The current decreases again when the barrier thickness is 3 nm but it is still larger than the current for the junction with no barrier. Only a plot of $\ln(I)$ against barrier thickness will reveal with any certainty what is happening with the reverse bias current. This plot is shown in figure 4.51. Unfortunately these plots show only a decrease in reverse bias current when an MgO tunnel barrier is included.

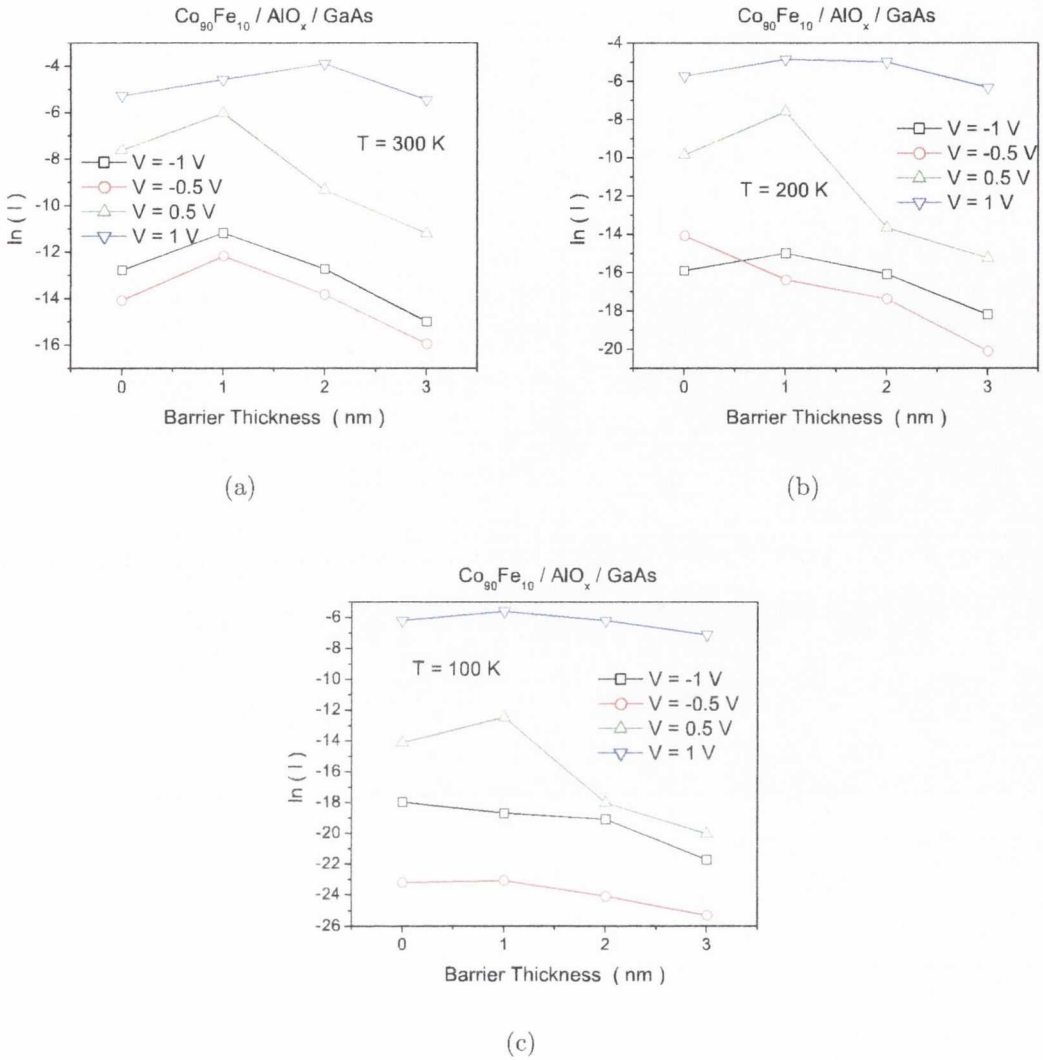


Figure 4.50: Plots of $\ln(I)$ vs. AlO_x barrier thickness on GaAs substrates at (a) 300 K, (b) 200 K and (c) 100 K. The current values are taken for voltages that are -1 V, -0.5 V, 0.5 V and 1 V. Junction size is 100 nm.

The junctions in this section were all fitted to the thermionic emission / diffusion model, part (c) of figures 4.46 to 4.49. For junctions with 2 nm and 3 nm of MgO the fit was again done on the area of curve after the tunneling distortion. When the MgO thickness is only 1 nm is harder to distinguish where this distortion starts and ends, part (c) of figure 4.47, and so it fitted in the usual area, the very low forward bias region. The results for all the junctions fitted are outlined in table 4.3.

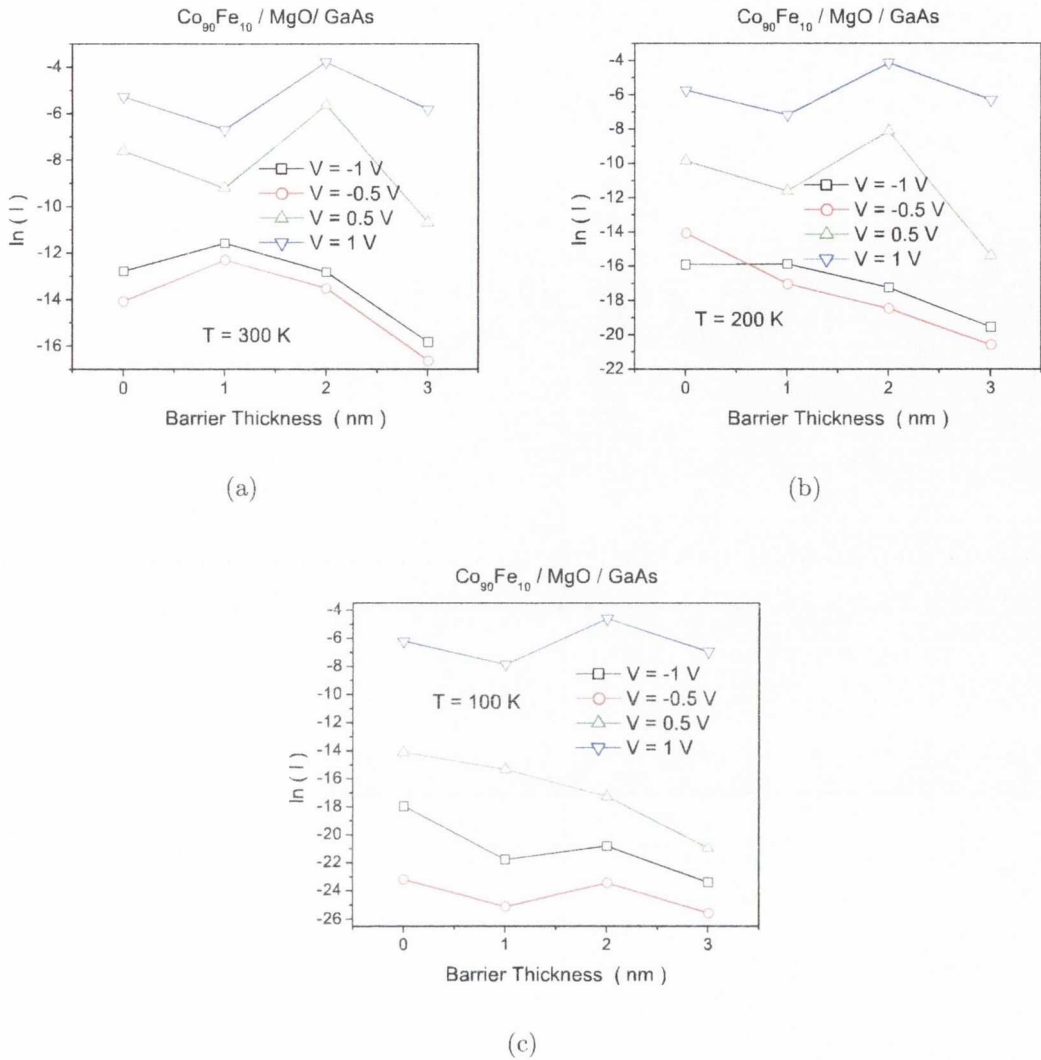


Figure 4.51: Plots of $\ln(I)$ vs. MgO barrier thickness on GaAs substrates at (a) 300 K, (b) 200 K and (c) 100 K. The current values are taken for voltages that are -1 V, -0.5 V, 0.5 V and 1 V. Junction size is 100 nm.

4.4 Resistance

It is important to show that it is the Schottky barrier that is dominating the resistance of the junctions, particularly given the results in the nano sized junctions. In order to do this each element of the junction that could contribute significantly to the junction resistance must be looked at on it's own. The first place to start is by looking at the

Material	Thickness in nm	ϕ_B in eV	n	T in K
	0	0.11	2.60	150
AlO _x	1	0.20	1.57	250
AlO _x	2	0.35	1.56	250
AlO _x	3	0.39	1.50	250
	0	0.12	2.51	125
MgO	1	0.14	2.60	200
MgO	2	0.31	1.38	200
MgO	3	0.43	1.42	225

Table 4.3: The barrier heights, ϕ_B , and ideality factors, n , for all junctions fabricated in the nm size on GaAs.

resistance of the semiconductors as a function of temperature.

4.4.1 Semiconductor Resistance

The inset in figure 4.52 is a graph of the resistance of the GaAs substrate used in the junctions as a function of temperature. The main plot in this figure is just the natural log of the conductivity of the semiconductor versus $1000/T$. As can be seen from the inset the resistance of this substrate is in $m\Omega$ at both room temperature and at 50 K and so can safely be neglected as having an impact on the behaviour of the $I - V$ curves. The graph was plotted as $\ln(\sigma)$ vs. $1000/T$ in order to extract the activation energy, E_a , of the semiconductor (higher temperature fit) and of the charge carriers (lower temperature fit). E_a is determined using the Arrhenius model given by,

$$\sigma = \sigma_0 \exp\left(\frac{E_a}{kT}\right) \quad (4.5)$$

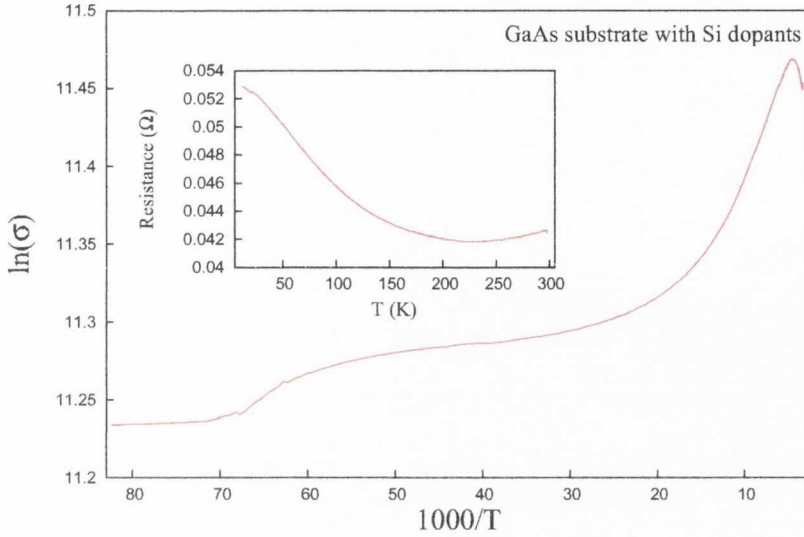


Figure 4.52: Main graph is of $\ln(\sigma)$ versus $1000/T$ for the mid n-type GaAs substrate in order to determine the activation energy, E_a . The inset is a graph of the resistance, R , versus T .

where σ is the conductivity of the semiconductor. T is the temperature in Kelvin and k is Boltzmann’s constant, equal to $8.6 \times 10^{-5} \text{ eVK}^{-1}$. σ_0 is a constant that is equal to the intercept when the data is plotted as $\ln(\sigma)$ vs. $1000/T$, also known as the conductivity equation, given as [18]

$$\ln(\sigma) = -\frac{E_a}{k} \frac{1}{T} + \ln(\sigma_0) \tag{4.6}$$

The slope of this plot is equal to E_a/k . For the GaAs at higher temperatures E_a was determined to be $1.31 \times 10^{-6} \text{ eV}$ and at lower temperatures E_a of the carriers is $1.93 \times 10^{-8} \text{ eV}$.

Figure 4.53 is again a graph of the natural log of the conductivity of the Si(001) substrate used in the fabrication of the junctions versus $1000/T$. The inset shows a graph of the resistance as a function of temperature so the resistance values can be seen directly. The resistance of this substrate is higher, which is to be expected given that the resistivity of the silicon is $2.3 \text{ } \Omega\text{cm}$, where as the resistivity of the GaAs substrate is only 1.2×10^{-2}

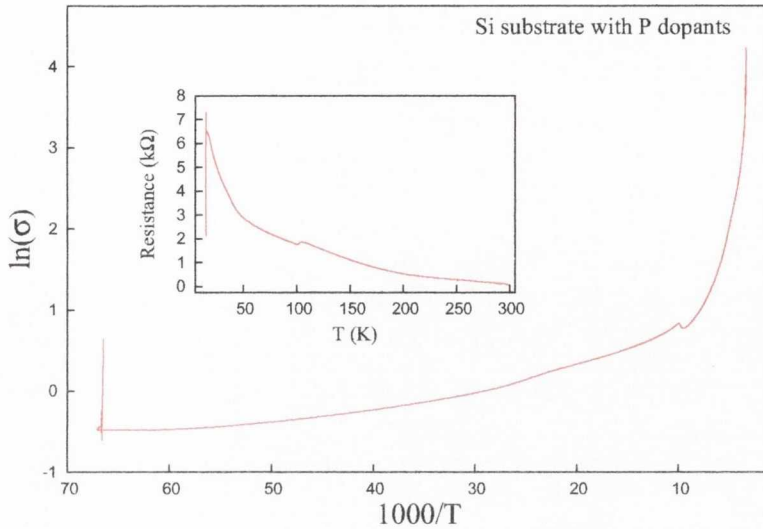


Figure 4.53: Main graph is $\ln(\sigma)$ versus $1000/T$ for the mid n-type Si(001) substrate. Again the inset is a graph of R vs. T .

Ωcm . The rate at which the resistance increases also changes, which again is linked to the difference in resistivity and carrier concentrations, and for silicon reaches $\text{k}\Omega$ at 50 K. However from the $I - V$ graphs shown earlier in the the resistance in forward bias at low temperatures is still greater than the resistance of the semiconductor. The kink in the graph in figure 4.53 that can be seen at around 120 K is due to the current that was initially set on the Keithly. As the resistance increased, the voltage increased and at 120 K it reached the allowed limit. The current had to be reduced, which caused a small break in the data points. Again the activation energy, E_a , was determined by fits of equation 4.6 at higher and lower temperatures. In this case E_a is 1.01×10^{-4} eV for the Si semiconductor (higher temperature fit) and 7.69×10^{-6} eV for the carriers (lower temperature fit).

4.4.2 Contact Resistance

The contacts used to fabricate the junctions also have a contribution to make to the overall resistance of the system. It should not be significant but it is important to get an idea of what it is. The contact resistance can be approximated using the resistivity of the semiconductor and the length of the side of the contact. A schematic is shown in figure 4.54. The contact series resistance can be approximated by the following,

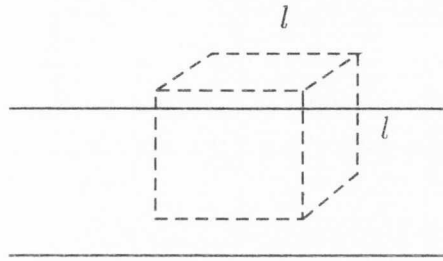


Figure 4.54: Schematic of the approximation of the contact resistance, contact outlined by dashed lines on a semiconductor substrate. l is the length of the contact and here all lengths, l , are equal.

$$R \sim \frac{\rho}{l} \quad (4.7)$$

For both semiconductors the contact length is approximately the size of the junction. For the GaAs substrate with $\rho = 1.2 \times 10^{-2} \Omega\text{cm}$ the resistance is approximately only 6Ω and for the Si substrate with $\rho = 2.3 \Omega\text{cm}$ is approximately 115Ω . Again, due to the higher resistivity, the resistances are larger for the Si substrate but both have a negligible contribution to the overall resistance of the junctions. All junctions were measured in a four point configuration, which helps to reduce the actual series resistance.

4.4.3 Tunnel Barrier Resistance

Next to the Schottky barriers, the tunnel barriers have the biggest effect on the transport characteristics of the device. An effect can be seen in the $I - V$ curves almost as soon as they are introduced in most cases, although it is not always the same for each case. It is important to get a handle on just what the contribution to the junction resistance might be due to the tunnel barriers. In order to show this a plot of the RA (resistance times the area) product of the tunnel barrier versus the thickness of the barrier is shown for MgO in figure 4.55 and for AlO_x in figure 4.56.

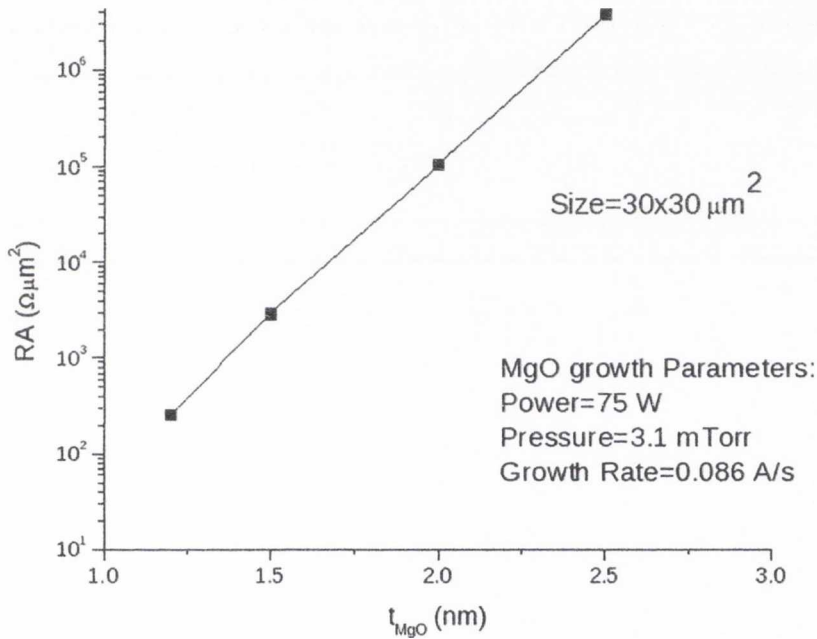


Figure 4.55: Plot of resistance times the area against thickness for an MgO tunnel barrier. This data is courtesy of Gen Feng and Kaan Oguz.

The data shown in figure 4.56 was taken from reference [19] and unfortunately the AlO_x thickness only goes to 1.2 nm. However an idea of the thickness dependence can be obtained from it. As seen from the figure the RA value plateaus as the AlO_x thickness increases. This is generally true and is due to the difficulty in making good quality, thick

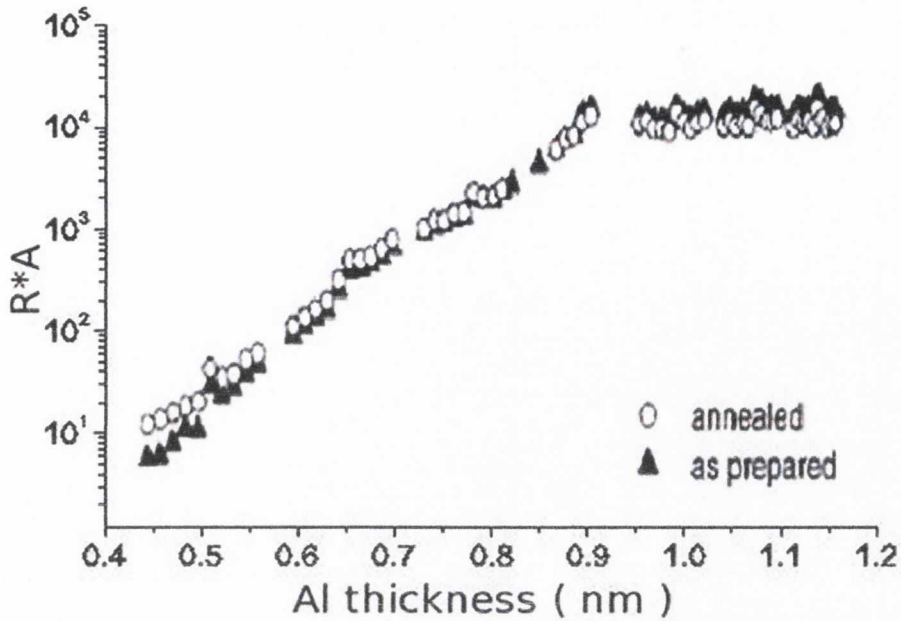


Figure 4.56: Plot of resistance times the area against thickness for an AlO_x tunnel barrier. This data is taken from reference [19].

AlO_x films, particularly when they have been fabricated by oxidising a thin Al film, as was the fabrication method used in this reference.

For an area the size of the micro sized junctions fabricated in this thesis, neither of these tunnel barriers contribute significantly to the overall resistance of the junction. However, as the junction area decreases the resistance contribution from the tunnel barrier, particularly from the MgO barriers, ought to increase significantly. In the nano sized junctions presented here the overall resistance in forward bias is *far less* than the resistance calculated for the tunnel barrier of equal area. This poses an extremely puzzling question, particularly as leakage through the SiO₂ insulating layer can be ruled out, as seen in both Chapter 2 and the next section.

4.5 Conclusions and Summary

In this chapter the electrical transport of four different metal / insulator / semiconductor systems have been studied, $\text{Co}_{90}\text{Fe}_{10} / \text{AlO}_x / \text{Si}$, $\text{Co}_{90}\text{Fe}_{10} / \text{MgO} / \text{Si}$, $\text{Co}_{90}\text{Fe}_{10} / \text{AlO}_x / \text{GaAs}$ and $\text{Co}_{90}\text{Fe}_{10} / \text{MgO} / \text{GaAs}$. The thickness of the barrier was varied in steps of 1 nm to see how transport is affected by barrier thickness. They were also patterned into two very different sizes, squares with side lengths of 50 μm and circular junctions with diameters of 90-100 nm, to determine how transport is affected by junction size. All junctions were given top contacts and electronic transport was measured as a function of temperature using the cryostat part of the resistivity (RT) rig that was described in Chapter 2.

For all junctions of all sizes the transport through the junctions was rectifying, where rectifying is considered to be current flow in only one bias direction, defined as forward bias and the reverse bias is the direction in which no, or very little, current flows. Rectifying behaviour is characteristic of a Schottky barrier present at the interface between a metal and a semiconductor. The barrier height, ϕ_B , and associated ideality factor, n , can easily be extracted by plotting the current as $\ln(dV/dI)$ against the voltage. While all junctions here for all barrier thicknesses and junction sizes show rectifying behaviour, fitting them to the thermionic emission / diffusion model was not always possible. Once the AlO_x thickness became larger than 3 nm in the micro sized $\text{Co}_{90}\text{Fe}_{10} / \text{AlO}_x / \text{GaAs}$ junctions, the distortion in the forward bias part of the curves became so large that it was impossible to fit the data to the model. The Si junctions in the nm range became impossible to fit almost as soon as any tunnel barrier was introduced between the $\text{Co}_{90}\text{Fe}_{10}$ and Si. The only exception was when 1 nm of AlO_x was inserted. Table 4.4 is a summary of all barrier heights, ϕ_B , and ideality factors, n , for all junctions which are able to be fitted to the thermionic emission / diffusion model.

Studying this table reveals a number of interesting things about the data. First looking at the micro sized $\text{Co}_{90}\text{Fe}_{10} / \text{MgO} / \text{GaAs}$ junctions. For a more direct comparison it is

Semiconductor material	Barrier material	Thickness in nm	ϕ_B in eV	n	A_e in m^2
Si		0	0.51	0.97	2.5×10^{-9}
Si		0	0.11	2.75	7.85×10^{-15}
Si	AlO _x	1	0.41	1.9	2.5×10^{-9}
Si	AlO _x	1	0.10	2.10	7.85×10^{-15}
Si	AlO _x	2	0.34	2.6	2.5×10^{-9}
Si	AlO _x	3	0.32	3.3	2.5×10^{-9}
Si	AlO _x	4	0.58	1.8	2.5×10^{-9}
Si	AlO _x	5	0.60	1.7	2.5×10^{-9}
Si	AlO _x	6	0.45	1.7	2.5×10^{-9}
Si	MgO	1	0.42	1.84	2.5×10^{-9}
Si	MgO	2	0.46	2.82	2.5×10^{-9}
Si	MgO	3	0.48	1.58	2.5×10^{-9}
GaAs		0	0.40	2.52	2.5×10^{-9}
GaAs		0	0.12	2.51	7.85×10^{-15}
GaAs	AlO _x	1	0.39	2.26	2.5×10^{-9}
GaAs	AlO _x	1	0.2	1.57	7.85×10^{-15}
GaAs	AlO _x	2	0.43	1.88	2.5×10^{-9}
GaAs	AlO _x	2	0.35	1.56	7.85×10^{-15}
GaAs	AlO _x	3	0.47	3.15	2.5×10^{-9}
GaAs	AlO _x	3	0.39	1.50	7.85×10^{-15}
GaAs	MgO	1	0.26	1.86	2.5×10^{-9}
GaAs	MgO	1	0.14	2.60	7.85×10^{-15}
GaAs	MgO	2	0.36	2.24	2.5×10^{-9}
GaAs	MgO	2	0.31	1.38	7.85×10^{-15}
GaAs	MgO	3	0.41	3.66	2.5×10^{-9}
GaAs	MgO	3	0.43	1.42	7.85×10^{-15}
GaAs	MgO	4	0.39	2.12	2.5×10^{-9}
GaAs	MgO	5	0.54	2.09	2.5×10^{-9}
GaAs	MgO	6	0.45	4.11	2.5×10^{-9}

Table 4.4: All barrier heights, ϕ_B , and ideality factors, n , for all junctions. The active area, A_e , for the nanometer sized junctions was calculated using πr^2 .

easier to refer to table 4.2. When there is no barrier between the Co₉₀Fe₁₀ film and the GaAs substrate, ϕ_B is 0.40 eV. As seen by figure 4.41 when 1 nm of MgO is inserted the

current increases. The explanation for this is given by table 4.2, the barrier height listed here when 1 nm of MgO is brought into the system is reduced to 0.26 eV with an ideality factor of 1.86. When the MgO thickness is increased to 2 nm ϕ_B also increases to 0.36 eV, still lower than no MgO barrier but higher than ϕ_B for 1 nm of a barrier. Increasing to 3 nm brings ϕ_B back to pretty much the same value as having no MgO barrier. This increase and decrease in ϕ_B mirrors the increase and decrease of the $\ln(I)$ with barrier thickness in figure 4.41. So it is concluded here that it is the reduction in ϕ_B when MgO is used as an ultra thin tunnel barrier that enables the increase of current in both forward and reverse bias directions.

Positive voltage is applied to the top side of the junction structure, i.e. the metal side. In these junctions positive bias also corresponds to the forward bias direction. Electrons flow in the opposite direction of current and so electrons travel from the metal into the semiconductor when the bias is in the negative direction, which corresponds to reverse bias here. This means that spin injection from the metal into the semiconductor only occurs under reverse bias and any increase in reverse bias increases spin injection efficiency. As seen in figure 4.41 the increase in the reverse bias current is even larger than the increase in forward bias current. The incorporation of ultra thin MgO tunnel barriers could open up the way for GaAs based spintronic devices and is a very exciting result. More information is needed about the $\text{Co}_{90}\text{Fe}_{10}$ / MgO / GaAs interfaces but the presence of an MgO (002) peak in figure 4.31 is an extremely good sign that the MgO is of good quality and highly orientated, which it probably would not be if there was an amorphous oxide layer between the GaAs and MgO. Similarly any amorphous oxide layer between the MgO and $\text{Co}_{90}\text{Fe}_{10}$ would be more likely to hinder current flow than help it but high resolution TEM analysis would be nice to confirm it.

For the Si junctions in the micro scale the effect of MgO is not nearly as impressive. The barrier height, ϕ_B , does decrease from 0.51 eV to 0.42 eV when 1 nm of MgO is between the $\text{Co}_{90}\text{Fe}_{10}$ and Si but a similar increase in forward bias current is not seen,

figure 4.19. However, in reverse bias at 300 K only a slight increase in the reverse bias current is seen and as mentioned earlier it is under reverse bias in which spin injection takes place and this also is a positive result. It is most likely that thin MgO on Si (001) is amorphous and so is just a tunnel barrier much the same as AlO_x , therefore will not act as a spin filter on Si.

Using AlO_x as the tunnel barrier in both the Si and GaAs systems only results in a decrease in the current in both directions, where any effect is observed, figures 4.18 and 4.40, in the micro sized junctions. However when the junction size is reduced to the nm scale this changes. A fairly significant increase is seen in the reverse bias current when 1 nm of AlO_x was introduced between the $\text{Co}_{90}\text{Fe}_{10}$ and Si at 300 K. As temperature decreases the increase also decreases and at 100 K the current value is lower than the junction without a barrier. However there is more interest in fabricating spin devices that operate at room temperature than there is in ones that operate at 100 K and for these nano sized devices AlO_x may open up the door to efficient spin injection into Si at room temperature. AlO_x between the $\text{Co}_{90}\text{Fe}_{10}$ and GaAs nano sized junctions does not have the same effect. There is a very slight increase in forward bias with 1 nm but in reverse bias the current gradually decreases. Transport through an MgO barrier at this size between $\text{Co}_{90}\text{Fe}_{10}$ and GaAs is also changed but sadly in this case it gradually decreases the current.

Looking only at the corresponding values of the Schottky barrier height for similar junction structures as a function of size in table 4.4 it can be seen that ϕ_B decreases drastically with size. For example in the most basic structure, $\text{Co}_{90}\text{Fe}_{10} / \text{Si}$, ϕ_B is 0.51 eV when the junction is $50 \times 50 \mu\text{m}$ but when the very same structure is reduced to only 100 nm in diameter ϕ_B is 0.11 eV. Although the ideality factors, n , are now very large compared to n obtained in Chapter 3 they are much the same as those obtained for the micro sized junctions². Before going any further in trying to explain the large current

²The active area, A_e , of the junctions in Chapter 3 are $\approx 36 \text{ mm}^2$, much larger than either of the junction sizes studied here.

values seen in the nano sized junctions it is necessary to consider two things.

The first is to ensure that there is no current leakage through the SiO_2 layer used to isolate the junctions from each other and excess contact material from the semiconductor substrate. This process was outlined in Chapter 2 but is worth repeating here. An area of the substrate with SiO_2 but no junction was contacted and the resistance measured. The resistance measured was between 100's of $\text{M}\Omega$ and $\text{G}\Omega$. This eliminates any possibility of current leakage through the SiO_2 as being a trivial explanation for such high forward bias currents.

The second is to look at the number of carriers actually present at the semiconductor / insulator / metal interfaces in the volume associated with the nano sized junctions. If it is only a few then the continuous medium picture is not valid. For Si the number of carriers are,

$$\begin{aligned} \text{in } 1 \text{ cm}^3 &\longrightarrow 1.6 \times 10^{15} \\ \text{in } 1 \text{ m}^3 &\longrightarrow 1.6 \times 10^{21} \\ \text{in } 2.355 \times 10^{-18} \text{ m}^3 &\longrightarrow 3.77 \times 10^3 \end{aligned}$$

which is just about enough for the model to hold true. However when looking at the number of carriers present inside the depletion region for junctions of this area it is approximately only 8 electrons. As said earlier the depletion width for the Si substrate is $0.71 \mu\text{m}$. This very low number of carriers raises questions about whether or not a valid Schottky barrier exists for the Si junctions. For the GaAs substrate the number of carriers present are,

$$\begin{aligned} \text{in } 1 \text{ cm}^3 &\longrightarrow 6.3 \times 10^{17} \\ \text{in } 1 \text{ m}^3 &\longrightarrow 6.3 \times 10^{23} \\ \text{in } 2.355 \times 10^{-18} \text{ m}^3 &\longrightarrow 1.48 \times 10^6 \end{aligned}$$

which is plenty of carriers for the thermionic emission / diffusion model to be applicable, even with the narrower depletion width of 31.7 nm for the GaAs substrate.

It has been proposed by Smit *et. al.*, [20], that once a diode, metal / semiconductor interface with rectifying $I - V$, becomes smaller than a characteristic length, l_c , that is associated with the semiconductor doping level, the thickness of the barrier, depletion region, x_d , is no longer determined by the carrier concentration of the semiconductor. Instead it will depend on the size and shape of the diode and the resulting thin barrier means that the Schottky barrier height *appears* to decrease with diode size. These thin barriers allow enhanced tunneling and tunneling is the key to efficient spin injection into a semiconductor. Figure 4.57 is a plot of this characteristic l_c versus the carrier concentration taken from [20]. The doping levels of the substrates used here have been connected to the corresponding l_c and have been marked on the original figure. As can be

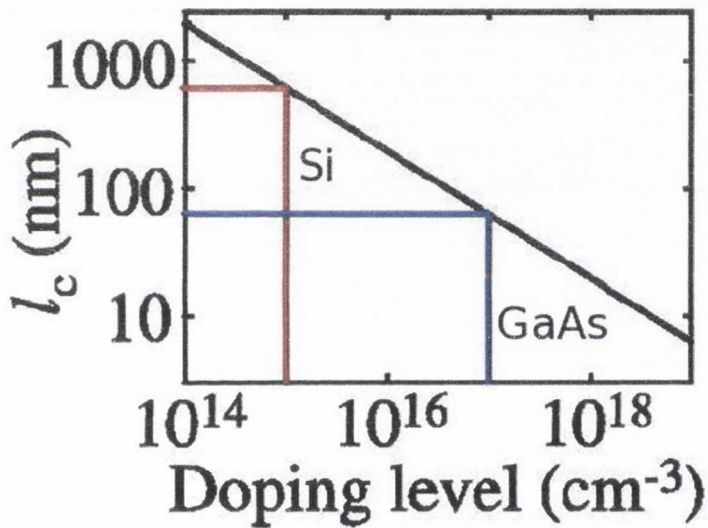


Figure 4.57: Graph of l_c versus carrier concentration (doping level) taken from [20]. The blue and red lines have been drawn in on the original graph and represent the doping levels of the substrates used in this Chapter. The red line is the Si substrate and the blue line is the GaAs substrate.

seen there is an inverse relationship between the doping level and the carrier concentration. From this graph it can be seen that for the Si substrate junctions the size of the diode, ≈ 100 nm, is less than then the characteristic length, l_c , and so can be used to explain the high currents seen in this junctions. However it is less certain in the GaAs case. For

these doping levels l_c is just less than 100 nm, meaning the GaAs systems are right at the limits of the model. However having eliminated the possibility of current leakage through the SiO₂ layer it is the mostly likely explanation for the high current observed in forward bias.

Similar observations in ϕ_B reduction have been reported for a number of extremely small diodes in various systems, for example carbon nanotube hetero-junctions [21], p and n-type Si nanowire junctions [23], and other metal / semiconductor junctions [22] & [24]. Here is the first time this has been observed in ferromagnetic metal / semiconductor and ferromagnetic metal / insulator / semiconductor systems fabricated by lithographic methods. Lithography gives huge control over device fabrication, it allows the use of complicated stacks and control over device shape. Overall the results here have been quite positive as regard to their utilization in spintronic devices.

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Chapter 5

Summary and Future Work

5.1 Summary

The focus of this thesis was to investigate transport through different interfacial barriers formed on silicon and gallium arsenide substrates when a ferromagnetic metal is grown on top of these substrates. This characterisation is important in the goal of realising usable and commercial Si- and GaAs-based spintronic devices. Two different ferromagnetic metals were used, Fe_3O_4 and $\text{Co}_{90}\text{Fe}_{10}$. Fe_3O_4 is a half metal and so theoretically has full spin polarization, and $\text{Co}_{90}\text{Fe}_{10}$ has the highest spin polarization of all Co-Fe alloys.

A thin insulating layer was introduced as tunnel barrier between the $\text{Co}_{90}\text{Fe}_{10}$ films grown on Si and GaAs substrates. Two different insulating materials were used, AlO_x and MgO. The barrier thickness was increased from 1 nm in 1 nm steps and the junctions were characterized as a function of barrier thickness as well as temperature. This time the junctions were patterned using UV lithography into pillars of well defined size, $50 \times 50 \mu\text{m}$, in order to get an exact value for the active area, A_e . More junctions were patterned using e-beam lithography into circular junctions of 90-100 nm in diameter, enabling a study of transport as a function of junction size. All films, except back contacts to the semiconductors, were grown by either DC or RF sputtering. The back contacts were made

by either thermal evaporation or high temperature soldering.

Good quality Fe_3O_4 was grown on four differently doped GaAs substrates, mid p and n-type and high p and n-type. The carrier concentration of these substrates were determined as follows; mid p and n-type have carrier concentrations of $1.0 \times 10^{18} \text{ cm}^{-3}$ and $7.7 \times 10^{-17} \text{ cm}^{-3}$ respectively and high p and n-type have carrier concentrations of $3.4 \times 10^{-18} \text{ cm}^{-3}$ and $3.5 \times 10^{-18} \text{ cm}^{-3}$ respectively. Electrical transport measurements were carried out as a function of temperature. The medium doped GaAs substrates revealed rectifying behaviour which is characteristic of thermionic emission / diffusion across a Schottky barrier. The data were fitted to the thermionic emission diffusion model, which was discussed in Chapter 1 and outlined in both Chapters 3 and 4, to determine the Schottky barrier height, ϕ_B and ideality factor, n , [1] & [2]. For the n-type medium doped GaAs, $\phi_B = 0.63 \text{ eV}$ and $n = 1.3$ and for the p-type, $\phi_B = 0.51 \text{ eV}$ with $n = 1.3$. An active area, A_e , of $\approx 40 \text{ mm}^2$ and a Richardson constant, A^{**} , of $8.2 \text{ Acm}^{-2}\text{K}^{-2}$, [1], were used to determine these values. The data were also plotted as activation energy plots, graphs of $\ln(I/T^2)$ vs. $1000/T$, [1], which are useful because there is no need to define an active area. However these plots do not give a value for n . The mid p-type substrate has a higher doping level than the n-type substrate and so at room temperature had quite a high leakage current, therefore fits for this substrate had to be carried out at temperatures for $T \ll 300 \text{ K}$. Values of ϕ_B obtained using an activation energy plot are 0.58 eV and 0.49 eV for the mid n and p-type GaAs semiconductors respectively. These values are in good agreement with values of ϕ_B obtained determined by fits to the thermionic emission diffusion model. For higher doping concentrations ($n, p \approx 3.5 \times 10^{18} \text{ cm}^{-3}$), transport across the $\text{Fe}_3\text{O}_4 / \text{GaAs}$ interface is dominated by thermionic field emission. In this case, electrons and holes tunnel through the Schottky barrier, resulting in nonlinear but nearly symmetric $I - V$ curves.

Fe_3O_4 was then grown on two differently orientated mid n-type Si substrates, Si(111) and Si(001). The carrier concentrations were determined to be $1.8 \times 10^{14} \text{ cm}^{-3}$ and $1.7 \times$

10^{-15} cm^{-3} for the Si(111) and Si(001) respectively. Transport measurements across these junctions again showed rectifying behaviour, that could be fitted using the thermionic emission / diffusion model at temperature regimes of $175 \text{ K} \leq 225 \text{ K}$ for the lower doped Si(111) substrate and $T \geq 250 \text{ K}$ for the Si(001) substrate. These fits give ϕ_B of 0.51 eV and 0.65 eV for the Si(111) and Si(001) junctions respectively and $n = 1.06$ for both using $A_e = 36 \text{ mm}^2$ and $A^{**} = 110 \text{ Acm}^{-2}\text{K}^{-2}$. Activation energy plots give ϕ_B of 0.52 eV on Si(111) and 0.65 eV on Si(001), which are in agreement with the previous values of ϕ_B . All barrier heights from Chapter 3 are summarized in table 5.1. The difference between the different barrier heights on Si(111) and Si(001) is due to interfacial layers formed during the initial stages of Fe_3O_4 growth. On the Si(111) substrate a crystalline iron silicide layer of $\approx 5 \text{ nm}$ and an amorphous oxide layer of $2 - 3 \text{ nm}$ are formed but on the Si(001) substrate the iron silicide layer is very thin, $< 1 \text{ nm}$, and a much thicker amorphous oxide layer of 6 nm is formed.

Semiconductor	Type	Carrier conc. in cm^{-3}	ϕ_B in eV	n	ϕ_B from AEP in eV
Si(111)	n	1.8×10^{14}	0.51	1.06	0.52
Si(001)	n	1.7×10^{15}	0.65	1.06	0.65
GaAs(100)	n	7.7×10^{17}	0.60	1.30	0.58
GaAs(100)	n	$\approx 3.5 \times 10^{18}$			
GaAs(100)	p	1.0×10^{18}	0.51	1.30	0.49

Table 5.1: Table of carrier concentrations and Schottky barrier heights for magnetite on various semiconductor substrates calculated in Chapter 3.

$\text{Co}_{90}\text{Fe}_{10}$ was grown on mid n-type Si(001) and GaAs(001) substrates with a tunnel barrier of AlO_x or MgO of increasing thickness from 0 nm in steps of 1 nm . These systems were patterned into micro and nano sized junctions. Electrical transport was then studied

as a function of temperature, barrier material and junction size.

In every case transport through these junctions was rectifying but with the insertion of a tunnel barrier a distortion was observed in the low forward bias region of the curves. The magnitude of this distortion depends very much on the barrier thickness and the junction system. For example, in the micro sized junctions with AlO_x , curves in the $\text{Co}_{90}\text{Fe}_{10} / \text{AlO}_x / \text{Si}$ systems could be fitted with the thermionic emission / diffusion model for all thicknesses of AlO_x . In the $\text{Co}_{90}\text{Fe}_{10} / \text{AlO}_x / \text{GaAs}$ systems once the AlO_x thickness was 4 nm or thicker the distortion was so large that the curves were impossible to fit. The ideality factors obtained were much larger than those obtained in Chapter 3 and made the junctions unsuitable for fits to activation energy plot as an ideality factor of 1 is assumed. When the size of the junction was reduced it became very difficult to fit the Si junctions with a tunnel barrier, despite rectifying behaviour being observed. Only one junction on Si with a tunnel barrier, 1 nm of AlO_x , could be fitted. All barrier heights and ideality factors for all sized junctions that could be determined are summarized in table 5.2.

Studies of the micro sized $\text{Co}_{90}\text{Fe}_{10} / \text{GaAs}$ system reveal a large increase in forward and reverse bias current with the introduction of a 1 nm MgO tunnel barrier. A direct comparison of ϕ_B of the same junction structure for different different A_e show that ϕ_B is dramatically reduced with size, however the increase in current with insertion of MgO between $\text{Co}_{90}\text{Fe}_{10}$ and GaAs is lost. Both of these results have interesting possibilities for the future of GaAs and Si based spintronic devices.

The introduction of 1 nm of a tunnel barrier results in the reduction of the Schottky barrier height, ϕ_B , for the micro sized junctions. As the tunnel barrier thickness increases from 1 nm the barrier height reduction appears to decrease. It is doubtful the actual height of ϕ_B changes again after the initial change brought about by the incorporation of an ultra thin barrier. It is more likely that as the tunnel barrier thickness increases it starts to limit the current flow along with the Schottky barrier and this results in an

Semiconductor material	Barrier material	Thickness in nm	ϕ_B in eV	n	A_e in m^2
Si		0	0.51	0.97	2.5×10^{-9}
Si		0	0.11	2.75	7.85×10^{-15}
Si	AlO_x	1	0.41	1.90	2.5×10^{-9}
Si	AlO_x	1	0.10	2.10	7.85×10^{-15}
Si	AlO_x	2	0.34	2.60	2.5×10^{-9}
Si	AlO_x	3	0.32	3.30	2.5×10^{-9}
Si	AlO_x	4	0.58	1.80	2.5×10^{-9}
Si	AlO_x	5	0.60	1.70	2.5×10^{-9}
Si	AlO_x	6	0.45	1.70	2.5×10^{-9}
Si	MgO	1	0.42	1.84	2.5×10^{-9}
Si	MgO	2	0.46	2.82	2.5×10^{-9}
Si	MgO	3	0.48	1.58	2.5×10^{-9}
GaAs		0	0.40	2.52	2.5×10^{-9}
GaAs		0	0.12	2.51	7.85×10^{-15}
GaAs	AlO_x	1	0.39	2.26	2.5×10^{-9}
GaAs	AlO_x	1	0.20	1.57	7.85×10^{-15}
GaAs	AlO_x	2	0.43	1.88	2.5×10^{-9}
GaAs	AlO_x	2	0.35	1.56	7.85×10^{-15}
GaAs	AlO_x	3	0.47	3.15	2.5×10^{-9}
GaAs	AlO_x	3	0.39	1.50	7.85×10^{-15}
GaAs	MgO	1	0.26	1.86	2.5×10^{-9}
GaAs	MgO	1	0.14	2.60	7.85×10^{-15}
GaAs	MgO	2	0.36	2.24	2.5×10^{-9}
GaAs	MgO	2	0.31	1.38	7.85×10^{-15}
GaAs	MgO	3	0.41	3.66	2.5×10^{-9}
GaAs	MgO	3	0.43	1.42	7.85×10^{-15}
GaAs	MgO	4	0.39	2.12	2.5×10^{-9}
GaAs	MgO	5	0.54	2.09	2.5×10^{-9}
GaAs	MgO	6	0.45	4.11	2.5×10^{-9}

Table 5.2: All barrier heights, ϕ_B , and ideality factors, n , for all junctions that could be fitted to the emission / diffusion model in Chapter 4. The active area, A_e , for the nanometer sized junctions was calculated using πr^2 , where $r = 50$ nm.

effective increase in the Schottky barrier height when fitted to the thermionic emission / diffusion model.

Despite the reduction in ϕ_B with the introduction of a 1 nm tunnel barrier, very few FM / I / SC systems had a corresponding increase in forward or reverse bias current. The $\text{Co}_{90}\text{Fe}_{10}$ / MgO / GaAs had the greatest ϕ_B reduction and a remarkable increase in both bias directions was observed but it was the only system to show any significant change.

In reducing the junction size down to ≈ 100 nm very little difference was made to the Schottky barrier height by the presence of a tunnel barrier. The effect of reducing the size of the junction into the nm range dramatically lowered ϕ_B to ≈ 0.10 eV in every case where the curves could be fitted to the thermionic emission / diffusion model, regardless of the system. This is because once the metal / semiconductor interface that is a diode becomes smaller than a characteristic length, l_c , that is associated with the carrier concentration of the semiconductor, the **thickness** of the Schottky barrier becomes linked to the diode size and decreases as the area of the diode decreases [3]. This results in an enhanced tunneling contribution to current transport through the barrier and manifests itself as an apparent reduction in ϕ_B when $I - V$ curves are fitted to the thermionic emission / diffusion model. However in reality there is no actual reduction in ϕ_B . This in turn should lead to an increase in spin injection efficiency and has positive implications for the incorporation of these junction systems into future nanosized spintronic devices. This is the first time such a reduction in ϕ_B has been seen for lithographically patterned junctions.

5.2 Future Work

The first step is to repeat the FM / I / SC structure but this time use CoFeB as the spin injector source for optimum spin polarized currents. The junction size should be reduced to 10 nm and finally to an atomic junction to allow a systematic study of transport as a function of device size. The junctions should also be studied as a function of magnetic field. All these should lead to the optimum electrodes for a spin injection experiment and

then a spin detection experiment should be carried out.

A lateral spin injection / detection experiment could be devised using e-beam patterning. A schematic of a device design that was used in an experiment by Palmstøm *et al.*, [4] is shown in figure 5.1. 5 nm of Fe is grown on a n-type GaAs substrate forming a Schottky barrier. The Fe junctions have been patterned into five $10 \times 50 \mu\text{m}$ bars with a spacing of $12 \mu\text{m}$ between the middle three bars and $160 \mu\text{m}$ from the end two. Low temperature measurements of voltage versus field reveal spin valve like behaviour, confirming spin injection.

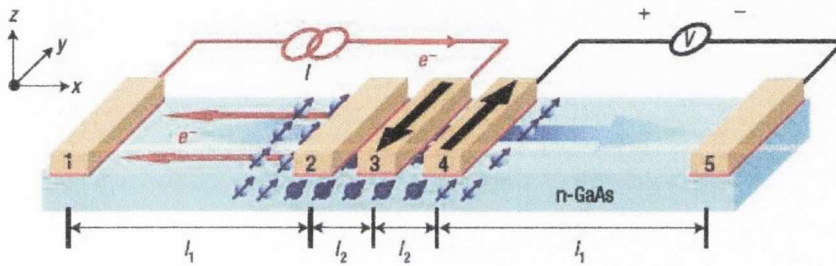


Figure 5.1: A schematic diagram of the non-local experiment (not to scale) carried out by Palmstøm *et al.*, [4]. The large arrows indicate the magnetization of the source and detector. Electrons are injected along the path shown in red. The injected spins (purple) diffuse in either direction from contact 3. The non-local voltage is detected at contact 4. Other choices of source and detector among contacts 2, 3 and 4 are also possible.

This experiment is particularly applicable to the systems used in this thesis and could be easily reproduced. The device dimensions could be reduced in size also, which should increase the detected signal. As it is solely based on electrical characterisation as a function of field spin injection in the Si systems could also be detected.

5.3 Publications

1. S.M. Watts, C. Boothman, S. van Dijken and J.M.D. Coey, *Magnetite Schottky barriers on GaAs substrates*, Appl. Phys. Lett. **86**, 212108 (2005)
2. C. Boothman, A.M. Sánchez, S. van Dijken and J.M.D. Coey, *Structural, magnetic,*

and transport properties of $Fe_3O_4/Si(111)$ and $Fe_3O_4/Si(001)$, J. of Appl. Phys. **101**, 123903 (2007)

3. S. Serrano-Guisan, Han-Chun Wu, C. Boothman, M. Abid, I.V. Shvets and H.W. Schumacher, *Time-resolved precessional magnetization dynamics in Fe_3O_4 thin films by pulsed inductive microwave magnetometry*, submitted for publication.

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Appendix A

Depletion Region Approximation

A.1 The Depletion Region Approximation

Analysis of a metal-semiconductor junction uses an approximation obtained by assuming the semiconductor is fully depleted over a distance x_d , called the depletion region. Using this approximation provides reasonably accurate information about how the electrostatic potential and electric field strength in a Schottky barrier depend on the barrier height, bias voltage and impurity concentration. The depletion region is defined here as being between the metal-semiconductor interface, $x = 0$, and the edge of the depletion region, $x = x_d$, where x_d is the depletion layer width. Outside the depletion region the semiconductor is neutral but within the region, the semiconductor is depleted of mobile carriers and there is a charge density, ρ , due to ionized donors. It can be seen from part (a) of figure A.1 that the semiconductor charge density can be given by,

$$\begin{aligned}\rho(x) &= qN_d & \text{for } 0 < x < x_d \\ \rho(x) &= 0 & \text{for } x > x_d\end{aligned}\tag{A.1}$$

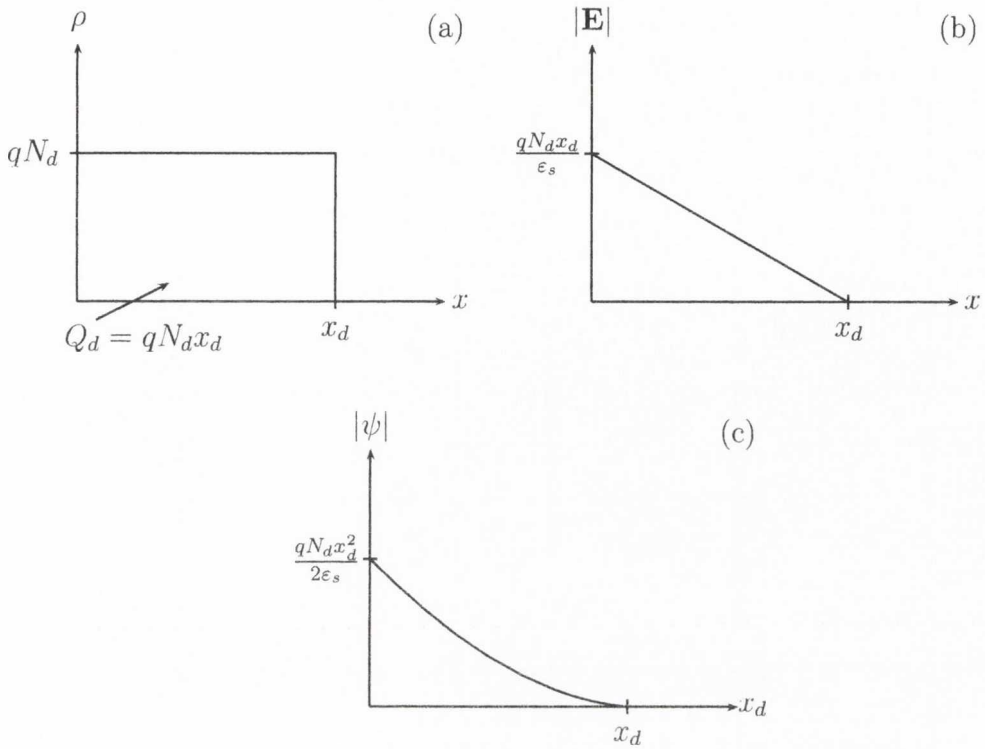


Figure A.1: Schematic of how (a) charge density, (b) electric field strength and (c) electrostatic potential varies as a function of distance within the depletion region, $0 \leq x \leq x_d$, according to the depletion approximation.

N_d is the donor density. Full ionization is assumed in the depletion region so the ionization donor density is equal to the donor density and is also N_d . At this point it is worth introducing Q_d , which is the total charge per unit area due to uncompensated donors in the depletion region. It can be seen from part (a) of figure A.1 that it is equal to qN_dx_d .

There is no electric field outside the depletion region otherwise a current would flow within the semiconductor. Gauss's law states that the electric flux through any closed surface is proportional to the enclosed electric charge and is given in the differential form as,

$$\nabla \cdot \mathbf{E} = \frac{1}{\epsilon_0} \rho \quad (\text{A.2})$$

where ϵ_0 is the permittivity of free space. Using Gauss's law here, ϵ_0 becomes ϵ_s , the

dielectric constant of the semiconductor, it is shown that the electric field increases as a function of position within the depletion region so that $\frac{\partial \mathbf{E}}{\partial x} = \frac{qN_d}{\epsilon_s}$. The magnitude of \mathbf{E} increases as a function of position within the depletion region, part (b) of figure A.1. It is given by,

$$\begin{aligned} E &= -\frac{qN_d}{\epsilon_s}(x_d - x) & \text{for } 0 < x < x_d \\ E &= 0 & \text{for } x > x_d \end{aligned} \quad (\text{A.3})$$

and the maximum value for \mathbf{E} is,

$$\mathbf{E}(x = 0) = |\mathbf{E}_{max}| = \frac{qN_dx_d}{\epsilon_s} = \frac{Q_d}{\epsilon_s} \quad (\text{A.4})$$

The electrostatic potential is also zero outside the depletion region. Within it the potential at x is given by integrating the electric field given in equation A.3.

$$\psi(x) = \int_x^{x_d} \mathbf{E}dx = -\int_x^{x_d} \frac{qN_d(x_d - x)}{\epsilon_s} = -\frac{qN_d}{2\epsilon_s}(x_d - x)^2 \quad (\text{A.5})$$

Therefore at the metal-semiconductor interface ψ has a maximum value given as,

$$\psi(x = 0) = |\psi| = \frac{qN_dx_d^2}{2\epsilon_s} \quad (\text{A.6})$$

At the interface the magnitude of $\psi(x = 0)$ is also equal to the diffusion potential, V_d and using equation A.6, V_d is given as

$$V_d = \frac{qN_dx_d^2}{2\epsilon_s} \quad (\text{A.7})$$

Using equation A.4 this can be re-written as,

$$V_d = \frac{\epsilon_s |\mathbf{E}_{max}^2|}{2qN_d} \quad (\text{A.8})$$

and

$$V_d = \frac{Q_d^2}{2\varepsilon_s q N_d} \quad (\text{A.9})$$

The differential capacitance per unit area can be obtained by taking the derivative of the charge with respect to the diffusion potential and according to equation A.9 is given by,

$$C = \frac{\partial Q_d}{\partial V_d} = \left(\frac{\varepsilon_s q N_d}{2V_d} \right)^{\frac{1}{2}} = \frac{\varepsilon_s}{x_d} \quad (\text{A.10})$$

The energy at the bottom of the conduction band relative to the Fermi level in the metal can be given as,

$$\begin{aligned} E_C(x) &= \phi_B + [\psi(0) - \psi(x)] \\ &= \phi_B + \frac{q N_d}{2\varepsilon_s} (x^2 - 2x_d x) \end{aligned} \quad (\text{A.11})$$

List of Symbols

ρ	–	charge density
q	–	positive charge equal in magnitude to the charge on an electron
N_d	–	donor density
x_d	–	depletion region width
Q_d	–	total charge per unit area
\mathbf{E}	–	electric field
ϵ_s	–	permittivity of the semiconductor
ψ	–	electrostatic potential
V_d	–	diffusion potential
E_C	–	energy of the conduction band in the semiconductor

References

Appendix A has been entirely referenced from,

- [1] B. van Zeghbroeck, *Principles of Semiconductor Devices*, online publication, ece-www.colorado.edu/~bart/book
- [2] E.H. Rhoderick and R.H. Williams, *Metal-Semiconductor Contacts*, 2nd Edition, Oxford Science Publications (1988)

Appendix B

LabVIEW Programs

B.1 Introduction

All the LabVIEW programs shown in this Appendix are ones that I wrote in order to make data analysis faster and to help avoid mistakes in repeated calculations. Other programs have been used in the collection of data and instrument control, these are not shown here as I did not write them.

B.2 Transport as a Function of Temperature

The transport data was collected using a program that performs an $I - V$ measurement every 5 K. All of these $I - V$'s are written to one data file. I wrote this program to split the data up into individual temperatures. The amount of data points used per $I - V$ must be specified. This value is divided into the total number of data lines and the number of different temperatures is output. A selected temperature is written to a new data file, containing only the data for this temperature. It is selected by picking the number corresponding to the temperature. The front panel of this program is shown in figure B.1.

The graphs in figure B.1 display the selected data as a plot of I vs V and as a plot

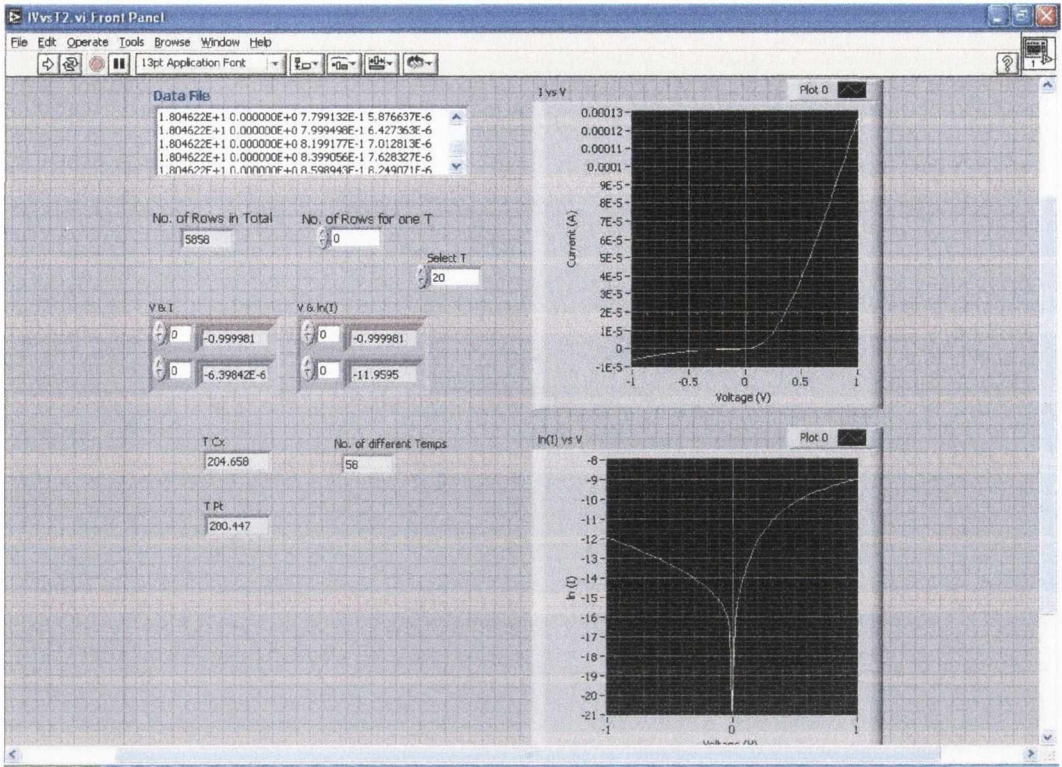
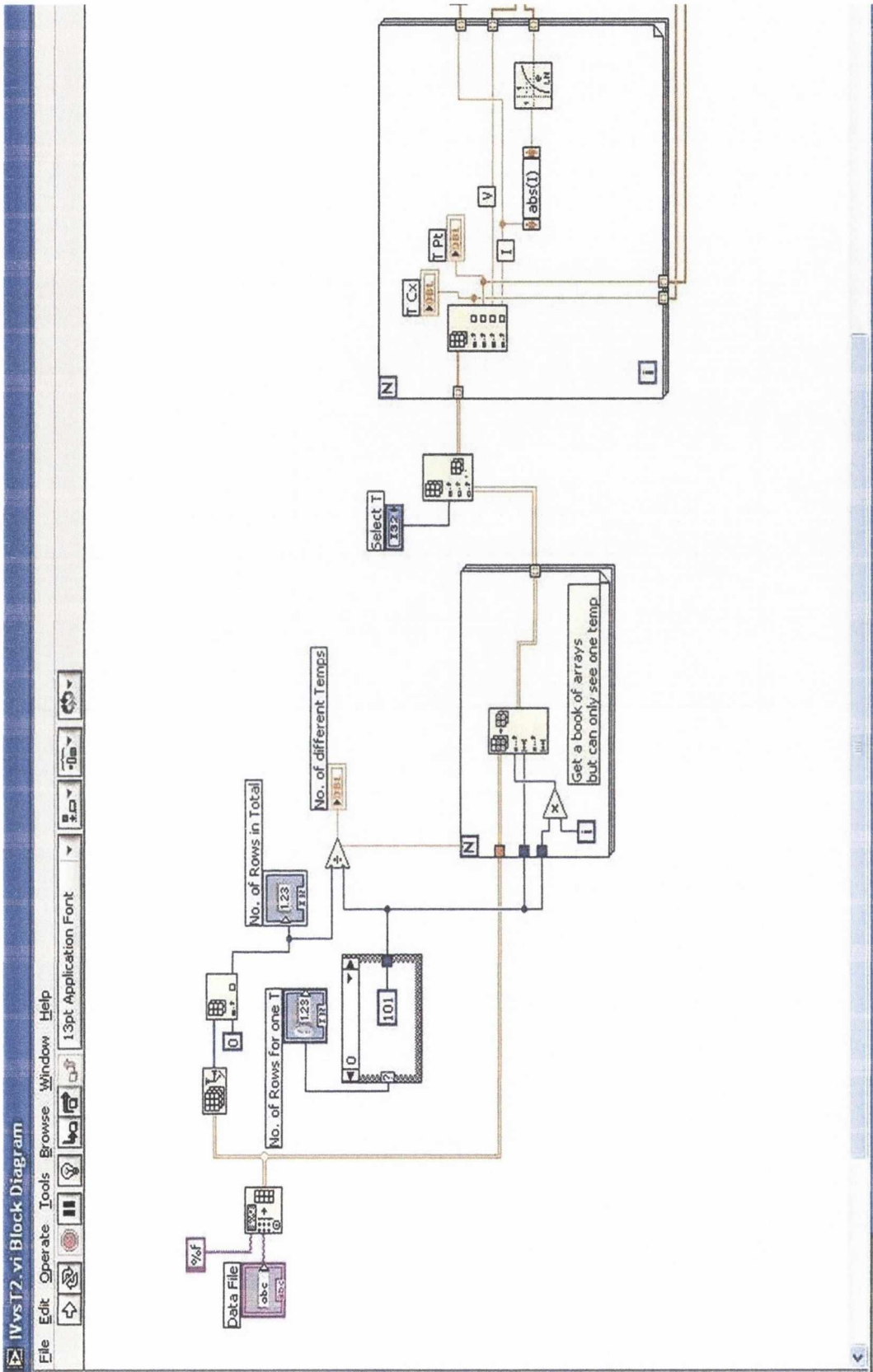


Figure B.1: Front panel of program to extract $I - V$ data for a chosen temperature from a much bigger data file.

of $\ln I$ vs V . The usual number of points per $I - V$ is 101 and so if no value is input for this a default value of 101 will be used. The block diagram of this front panel is shown in figure B.2.

This program writes the data of I vs V and $\ln I$ vs V for each selected temperature so that it can be plotted very easily.



B.2.1 Barrier Height and Ideality Factor Calculation

The barrier heights and ideality factors were all calculated by straight line fits to the small forward bias plots of $\ln(dI/dV)$ vs V . This program was written to do the calculations by inputting the slope and intercept of the line fit for a particular chosen temperature. The area of the junction and the Richard's constant for the semiconductor must also be input. The front panel is shown in figure B.3. And the back panel is shown in figure B.4

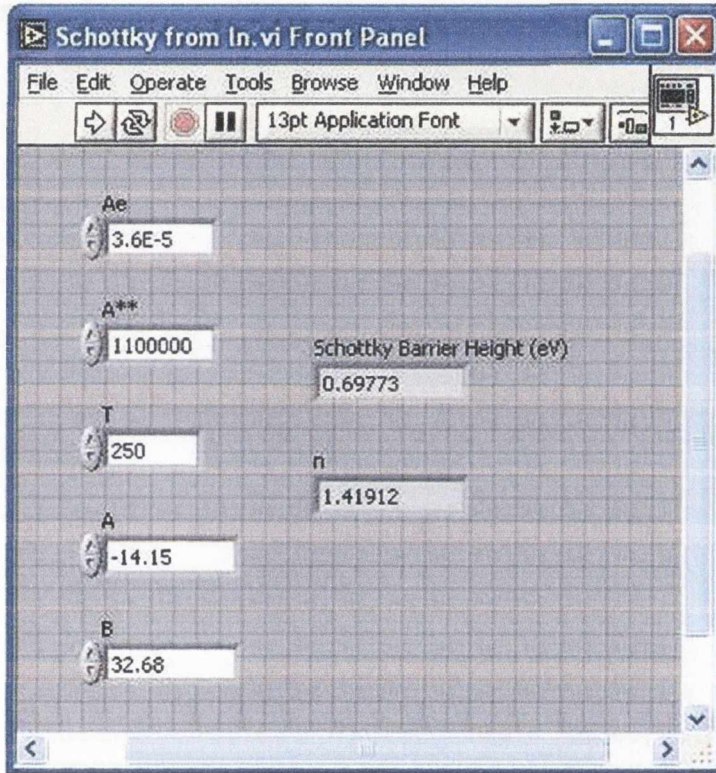


Figure B.3: Front panel of program to calculate the barrier height, ϕ_B , and the ideality factor, n , from the straight line fit to $\ln(dI/dV)$ vs V plots.

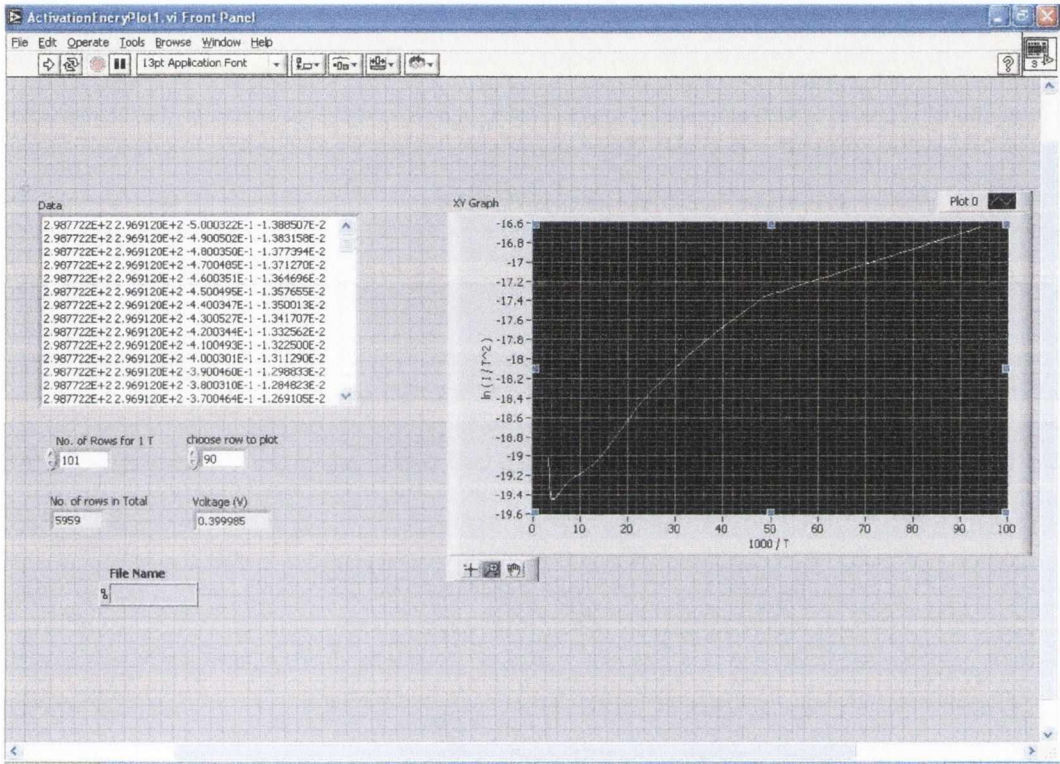
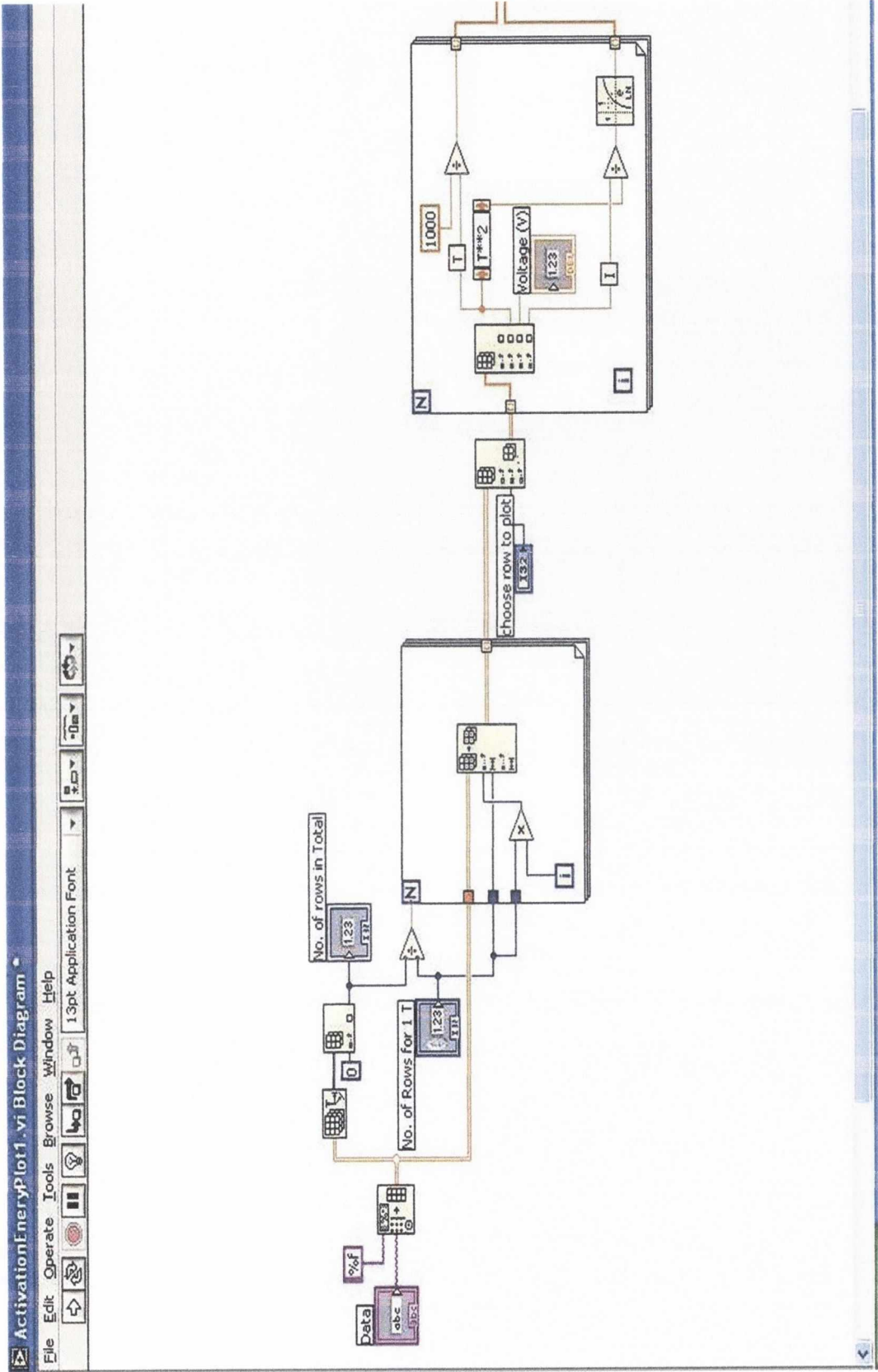


Figure B.5: Front panel of the program to select a specific voltage to get an activation energy plot. The data for that voltage is written to a new file.



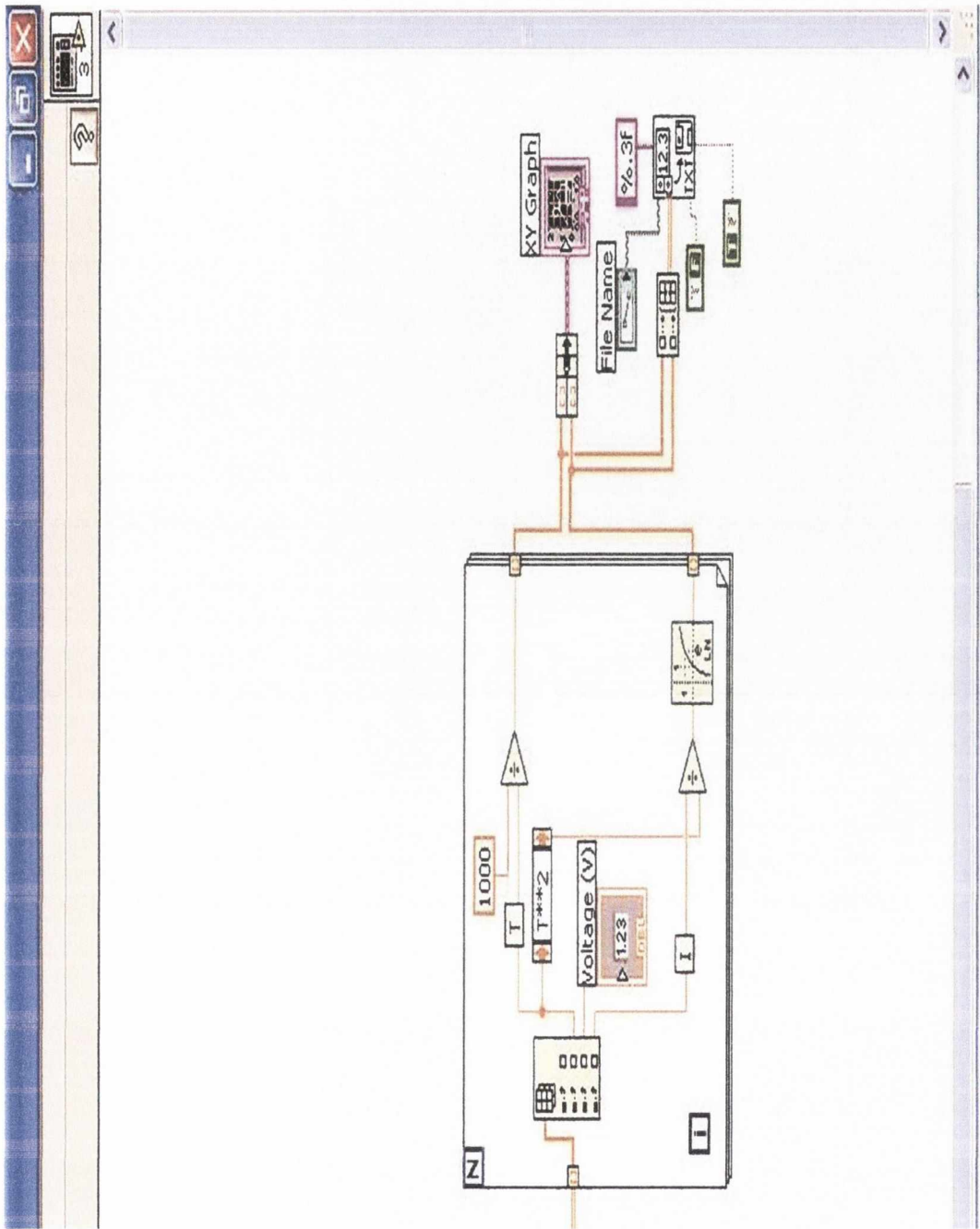


Figure B.6: Block diagram of the front panel shown in figure B.5. Note the overlapping section between the two pages.

B.4 Van der Pauw Technique

The following are the two programs used to determine the resistivity and carrier concentration once all the van der Pauw measurements have been taken as outlined in the section on Hall measurements in Chapter 2.

B.4.1 Resistivity Calculation

This program does two things. It calculates the resistivity by evaluating equation B.1 using the measured van der Pauw resistivity voltages.

$$\exp\left(-\frac{R_A}{R_S}\pi\right) + \exp\left(-\frac{R_B}{R_S}\pi\right) = 1 \quad (\text{B.1})$$

It also calculates the percentage difference in the reciprocity theorem,

$$\begin{aligned} R_{21,34} + R_{12,43} &= R_{43,12} + R_{34,21} \\ R_{32,41} + R_{23,14} &= R_{14,23} + R_{41,32} \end{aligned} \quad (\text{B.2})$$

The front panel is shown in figure B.7. The block diagram was written within frame, which has various iterations, all of which are shown in figure B.6.

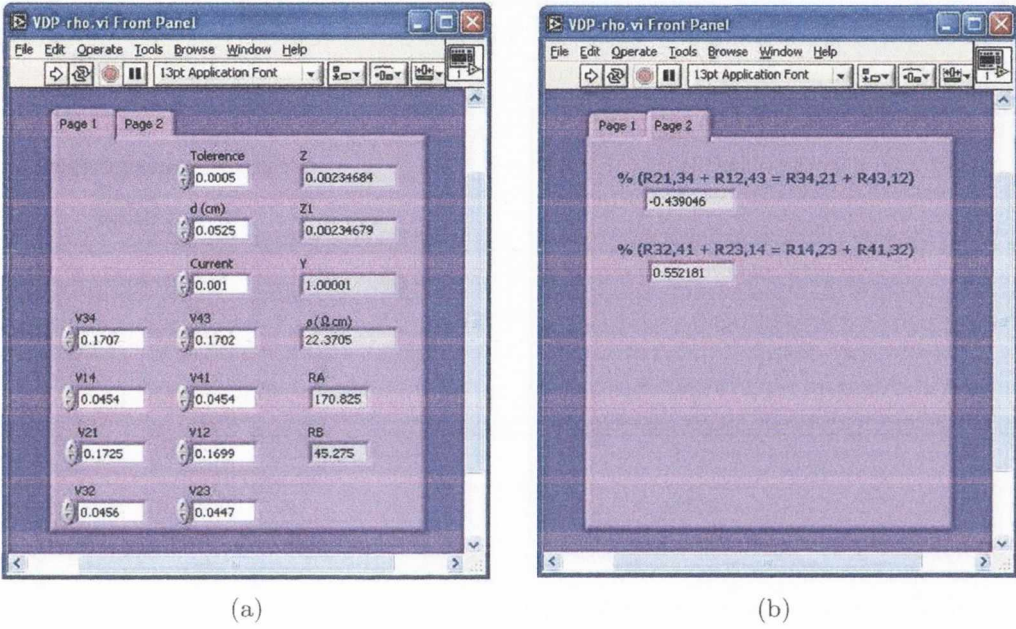
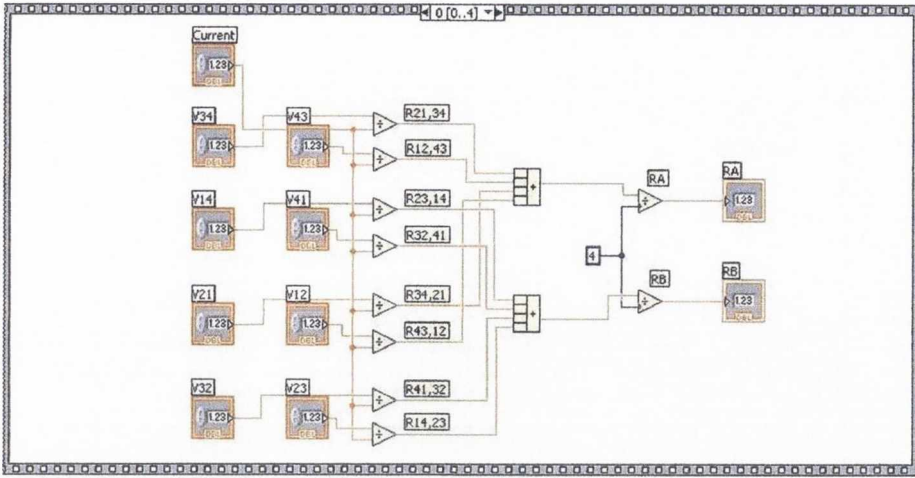
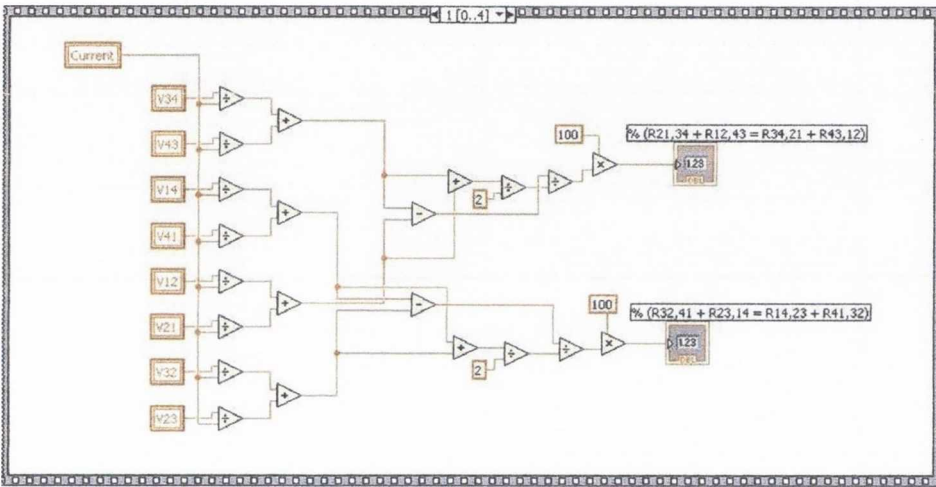


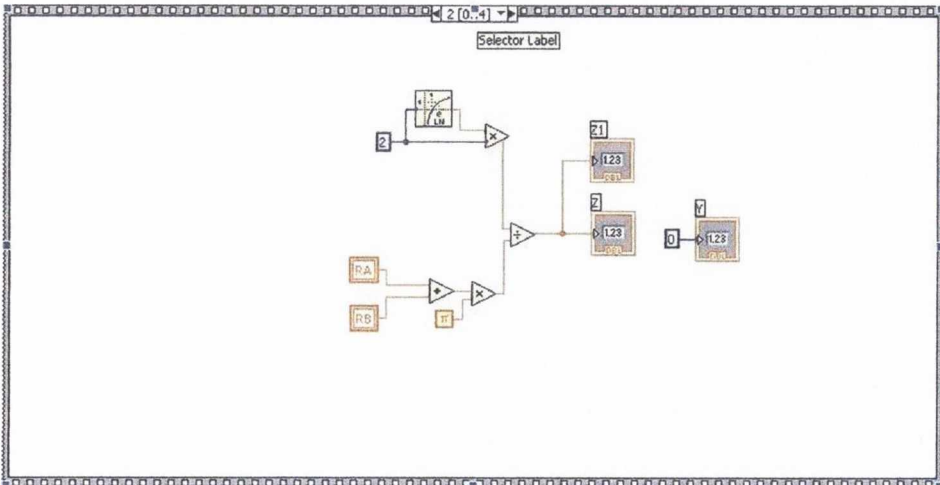
Figure B.7: Front panel of the program to calculate the resistivity of a semiconductor sample using the van der Pauw method. (a) is the section where the measured values are input and calculated resistivity in units of Ω cm is output. (b) is where the calculated percentage difference in the reciprocity theorem, equations B.2 is output so as the quality of the measurements can be verified.



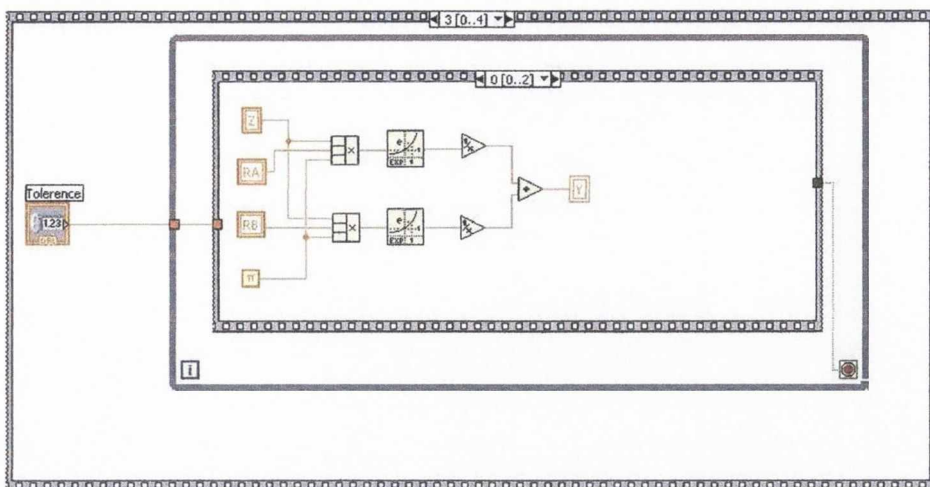
(a)



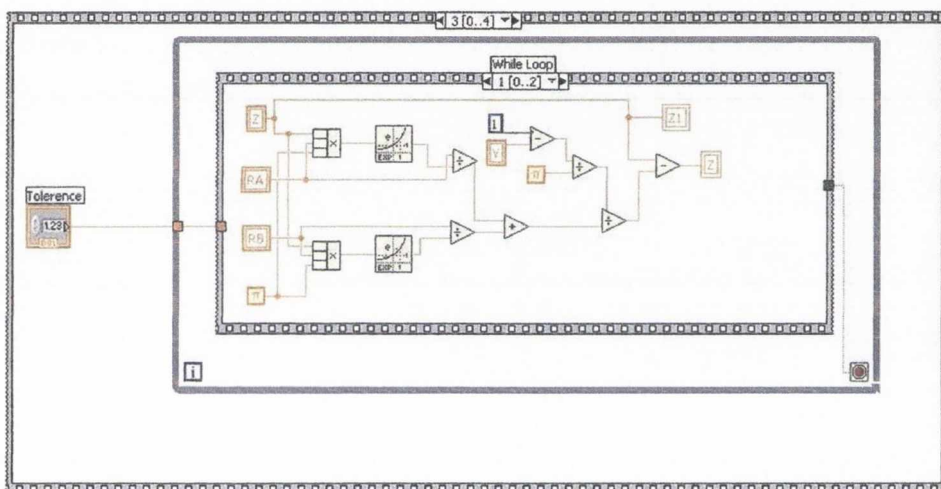
(b)



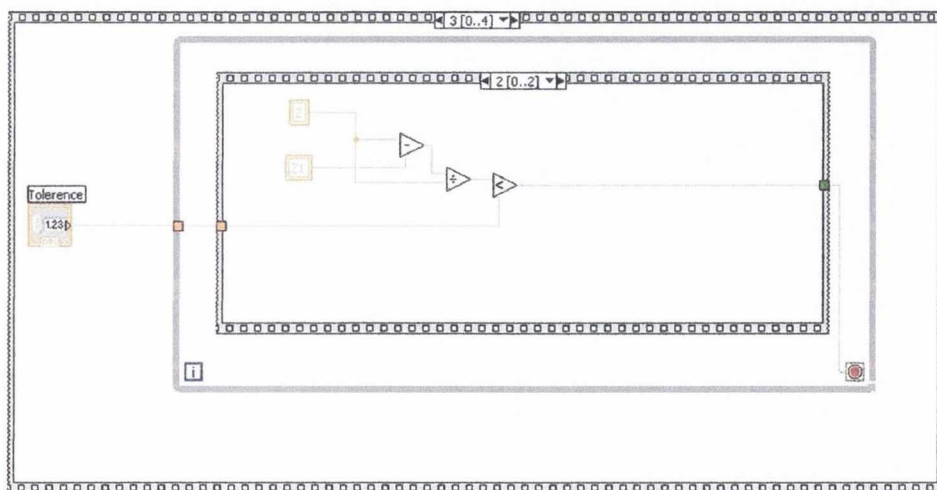
(c)



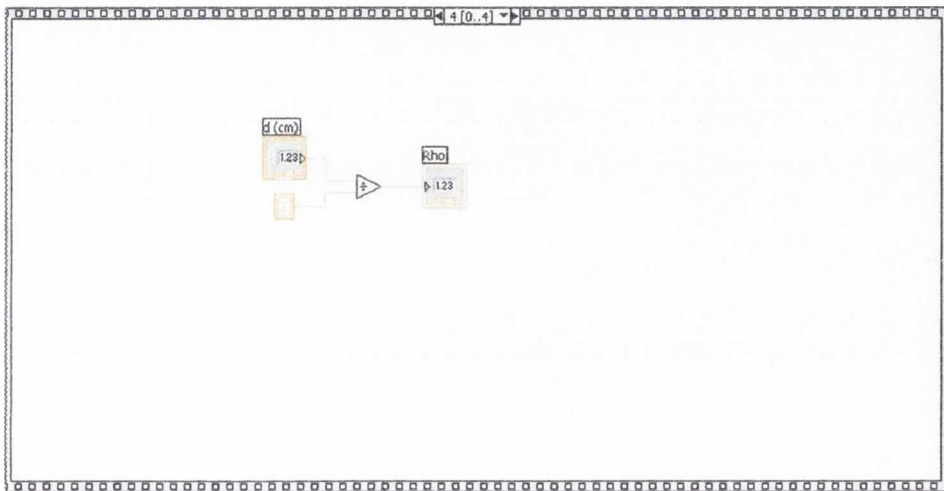
(d)



(e)



(f)



(g)

Figure B.6: Block diagram of the program to calculate the resistivity. (a) to (g) are the different frames in the program.

B.4.2 Semiconductor type and Carrier Concentration

This program is just a simple calculation of the carrier concentration and the sign gives away the semiconductor type. Positive means p-type and negative means n-type. When inputting the field and thickness values particular care must be paid to units, the field must be gauss and the thickness must be in cm. The current and voltages must be given in amps and volts respectively. The front panel is shown in figure B.7 and the block

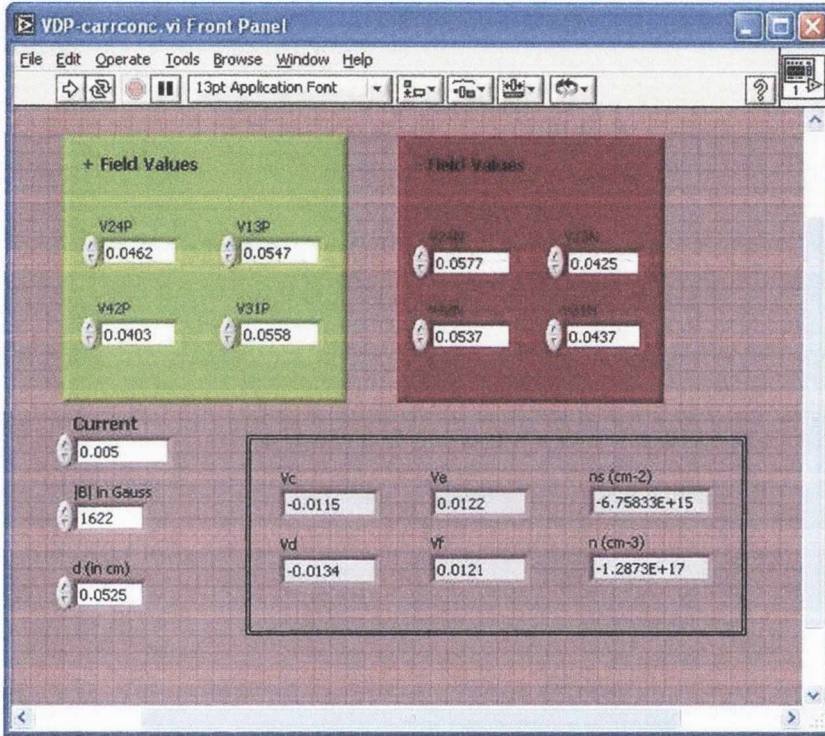


Figure B.7: Front panel of the program that uses the measured Hall voltages in order to calculate the carrier concentration of a semiconductor sample. If the sign of the output values is positive the semiconductor is p-type and if it is negative the semiconductor is n-type.

diagram is shown in figure B.8

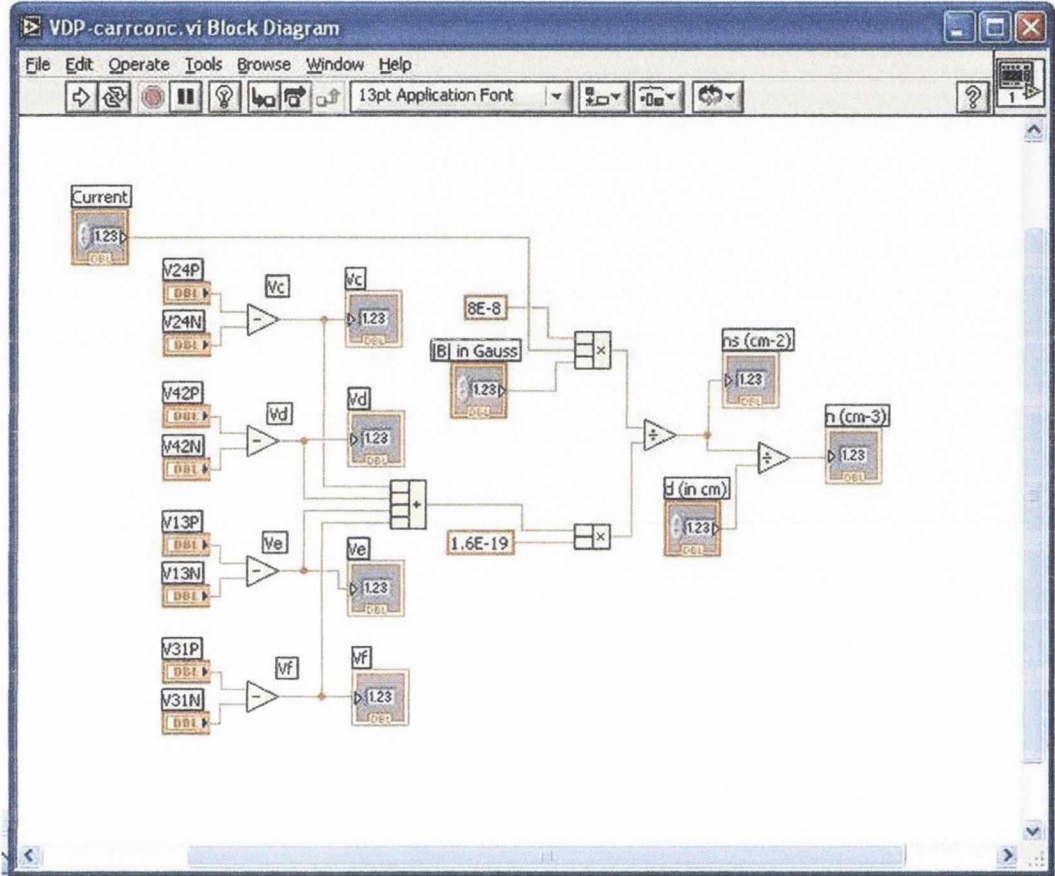


Figure B.8: Block diagram of program to calculate semiconductor type and carrier concentration.

Acknowledgements

There are many people to be thanked here so I'll begin by thanking my supervisor, Mike Coey, for the allowing me the opportunity of this project. I have thoroughly enjoyed all aspects of it and have learnt a great deal throughout it's course.

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