Nano-Fabrication and Electronic Transport Properties of Silicon Nanowires

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A thesis submitted in partial fulfilment of the requirements for the degree of

Doctor of Philosophy

February 2019
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Acknowledgements

First and foremost, I would like to express my deepest gratitude to my supervisor Prof. Plamen Stamenov for giving me the opportunity to work in his group. His consistent guidance, encouragement and tremendous support has enlightened my knowledge and expertise over the years. He has given me great advice which is not only restricted to the academics. During my illness he has been a great support. I would also like to extend my gratitude to Prof. Mike Coey for his contribution and support.

I would like to thank my parents Mr. Nirbhai Kumar Verma & Mrs. Sadhana Verma who have been always there for me and have motivated and provided me the strength to complete my PhD thesis. My sincere thanks to my brother Mr. Suryansh Verma who has boosted up my confidence during all these years. My dearest husband Dr. Vineet Kumar Singh has been a tremendous support to me for more than over a last 2 years. He has encouraged me through out these years and always stood by me whenever I needed his support. Thanks are also due to my in-laws who have shown patience and supported me.

I would also like to acknowledge past group member Dr. Stephen Connaughton who has guided and trained me in all the fabrication processes and measurement techniques and also for being very good friend and being there always to encourage and motivate me, Dr. Kiril Borisov for training me about the cryostate measurement and also for being a great friend, Dr. Naganivetha Thiyagarajah for EBL and past group members Dr. Pelin Tozman, Dr. Yong Chang Lau and Dr. Davide Betto who has made this journey less difficult. I also like express my appreciation to the present Magnetism and Spin Electronics group members Dr M. Venkatesan, Dr. Gwenael Atcheson, Dr. Zsolt Gersci and all others for motivating me from time to time.

I would also like to thank the finance staff Mrs. Jacqueline, Mrs. Tracy Byrne, Ms. Amanda Murtagh, and Mrs. Marie Kinsella for encouragement and looking after me and being so efficient in their work which helped me a lot in pursuing my work here.

Many thanks to our technical staff Julia Kremer (a very good friend), Dr. Alan Bell, Dermot Daly, Mike Finneran, David O Mahony and Alan O Meara for their constant help.

I am also indebted to Dr. Karsten Fleischer, Emma Norton, David for lending me Keithley 6430 system on which most of my measurement has been done, Dr. Cormac Coilein for his constant guidance regarding the cryostate and Mr. Chris Murry for teaching me all the CRANN cleanroom tools and for initial IWG meeting discussions as my Intel mentor.

I am eternally grateful to Dr. Sinead Winter for being a great and caring friend who has encouraged
me always and for the love she has bestowed on me from the day one, Dr. Eleanor Holmes my Latex
guru and very great friend who has always cared for me. Aunt Anne Gannon and Aunt Barbara
Winter for the love and care. Dr. Brendan O’Dowd and Dr. Zara O’Dowd for being a great friend.
Megan Canavan for her help to get all the TEM Images, for all the chit chat during coffee/tea meet
ups and for the motivating conversation to finish the PhD thesis. Dr. Romina Charifou for all her
fun crazy jokes and looking after me and Prabhava Sai N Barimar for all the discussion on solid state
physics and for providing me the SOI substrate. Mr. Peter Glesson taught me all about ICP etching
and discussion about the fabrication process and being a great friend. Words won’t be enough to
express their kindness towards me. Many thanks to Helen Thornbury for being kind and caring and
Dr. Parvaneh Mokarian for her great advice on life. My acknowledgement cannot be complete without
thanking Prof. Louise Bradley for all the advice from the beginning of my PhD and looking after me
throughout the course.

Very special people who made me feel like home in Ireland and were there to look after me Dr.
Jane O Reilly my soul sister, Dr. Stephen Porter who was always so kind and sassy Dr. Joao Coelho,
I express my sincere gratitude to them. I do not know what I would have done without you guys. In
the last, my sincere thanks to most important people with whom I have shared my office, my friends
who made my journey less painful Dr. Sonia Jaskaniec, Katarzyna Siewierska, Robbie McGuniess,
Gaurav Jain, Ajay Jha, Dr. Chuan Zhong, Dr. Matthias Kremer and, Robert Lucas and all others
whose names I might have missed to mention here.

I am grateful to Irish Research Council Enterprise Partnership Scheme (Intel), Project ID EP-
SPG/2012/450 for first three years of my PhD and for final year Science Foundation Ireland (SFI),
Grant No. 12/RC/2278 for providing financial support.
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Abstract

This project develops a robust and reliable process to pattern sub 20 nm features in negative tone Hydrogen Silsesquioxane (HSQ) resist using high resolution Electron Beam Lithography (EBL) and a low damage reactive ion etch (RIE) process to fabricate Silicon (Si) nanowires (NWs) on non-uniformly highly doped n-type Silicon-on-insulator (SOI) substrates. HSQ resist converts into SiO$_2$ due to its chemical composition upon exposure to electron beam of high energy and become a very stable high resistance mask against RIE etching after further thermal treatment. In addition, it also acts as an insulating layer a few nanometers thick to avoid the shorting of the contact electrodes in a Hall structure used extensively in this investigation.

Optimized processes for lithography, dry etch are employed to fabricate Hall bars 10 $\mu$m and 20 $\mu$m wide and NW devices with mean widths from 500 to 30 nm on SOI substrates having device layer thickness of 45 nm and a doping density $\approx 8 \times 10^{18}$ cm$^{-3}$ at buried oxide to $5 \times 10^{19}$ cm$^{-3}$ at surface. The devices are electrically characterized at room and cryogenic temperatures from 300 K down to 10 K to extract resistivity, mobility and carrier density for Si material as a film, microstructured Hall bar and nanowire. The room temperature mobility is observed to be 104 cm$^2$/Vs for the Si film which is consistent with the literature for heavily doped Silicon having doping level of $10^{19}$ cm$^{-3}$. For the Si Hall bar structure, the DC Hall measurement shows the obvious increase in Hall mobility on reducing the size of the bar width from 20 $\mu$m to 10 $\mu$m. These Hall contact electrodes are fabricated on the surface of device layer where the doping level is high and exactly opposite to each other, which has resulted in smaller measurement uncertainty.

Performing Hall measurements on single semiconductor NWs is a challenging task. To the best of our knowledge only few groups have been able to carry out these measurements so far [1–9]. For Silicon NWs from 30 to 500 nm, the Hall contacts of 200 nm in width are fabricated using the nanowires as a shadow masks due to which the Hall contacts are not exactly opposite to each other. Thus, the Hall voltage signal is extracted from longitudinal electrodes. Both DC and AC measurements are performed on these Si Nanowires. Electron transport data in non-uniformly heavily doped silicon nanowires is extracted from these measurements. The DC Hall measurements of low mobility samples can result in a poor signal to noise ratio and suffer from additional problems such as enhanced electromigration, thermal gradients, thermoelectric effects or Seebeck voltages whereas, the AC Hall effect measurements has yielded capability to measure low mobility sample with greater resolution and reduced Joule heating and eliminates some slow thermal effects. Thus, AC Hall effect measurements
are employed to extract the transport behavior in narrow Si NWs.

Two distinct options for AC measurement have been employed: 1) magnetic field sweeping in the range of ±14 T and 2) the sample is rotated under constant magnetic field at +14 T. The second option is relatively economical as the cryostat ramping at high magnetic fields consumes a large amount of liquid Helium per measurement. This approach minimizes the use of liquid Helium resources, while shortening substantially the acquisition time and therefore reducing the susceptibility towards thermal drift without compromising the accuracy of measurement.

The Hall voltage of Si NWs are recorded from these measurements by using the Physical Property Measurement System (PPMS) controller software package for AC Magneto-Transport. This software, supercedes the standard PPMS MultiVu, allowing for extended device control and real time data acquisition. For the pre-processes and fitting of the transport data, a custom routine written for Mathcad\textsuperscript{TM} has been implemented, allowing for the asymmetric and symmetric with respect to field components of the pick-up to be extracted together with their magnitude and phase and as a function of field magnitude, angular orientation and temperature.

The AC Hall measurement performed on these fabricated Si NWs distinctly exhibit the increase in Hall mobility from 41 cm\textsuperscript{2}/Vs to 181 cm\textsuperscript{2}/Vs as the width of the NWs reduces from 150 nm to 40 nm at 300 K. This could be contributed by use of high magnetic field to 14 T, which diffusive localizes the movement of electrons in the Si channel and hence improved the transport by reducing the surface scattering. The carrier concentration values extracted from these AC Hall measurements have shown the uncertainties in values due to the formation of a depletion layer. The depletion effect varies with the width of the Si NWs, this effect has low impact on larger width this effect also influenced by the non-uniform doping density of the Si device layer. As in this study, the Hall electrodes are fabricated at the side of the Si NWs wall, the electrodes which are in contact to the area of Si NWs of high doping level has provided close to ideal IV characteristics. Nanowire of width < 30 nm have shown a poor conductivity, that could be due to the formation of depletion width of 32 nm in the channel for an average carrier concentration of 5×10\textsuperscript{19} cm\textsuperscript{−3}. There is a substantial demand for the study of electronic transport of single semiconductor NWs. Here a successful methodology has been developed for Hall measurement of non-uniformly and non-degenerately-doped device layer of SOI substrate. This methodology can also be extended to other (i.e. compound semiconductors such as III-Vs and II-VIs) NWs.
Chapter 1

Introduction

Since the invention of the first transistor by John Bardeen, Walter Brattain and William Shockley in 1947, the microelectronics revolution of the past 70 years has always been intimately connected with the advances in material science and technology. First, the advances in lithographic tools and doping by ion implantation has brought about a Large Scale Integration/Very Large Scale Integration (LSI/VLSI) revolution where complexity has increased from the single transistor to integrated circuits, to the large scale integration to VLSI where systems or subsystems are placed on a single chip. Second, more recent developments in epitaxial growth techniques such as Molecular Beam Epitaxy (MBE) and Metal Organic Chemical Vapor Deposition (MOCVD) that allowed precise control of layer thickness, composition and doping profiles on an atomic scale has led to the fabrication of artificially structured semiconductors with enhanced electrical and optical properties. This has opened up a remarkable new world of semiconductor physics. Of these two, the first has definitely had a greater impact on the commercial arena whereas the second one has been mainly setting the stage for the exploration of device physics.

Carrier mobility and concentration are the governing physical transport parameters describing the ability of an electronic state to transmit information effectively. Novel materials and concepts are discovered, and their implementation into devices is driven forward. In 1959, Richard Feyman in his talk “There is a plenty of room at the bottom” mentioned his vision of miniaturization [10]. After few years in 1975, intel co-founder Gordon Moore estimated that the number of transistors per chip has doubled in every two years [11]. However, in 2018 it is thought that this prediction could be saturating. On the contrary, researchers are still finding innovative ways to keep alive this prediction with Silicon (Si) material, still in high demand [12]. Over the past few years, Si nanowires
(NW) having dimensions in the range of few nanometers to 100 nanometers have received considerable attention worldwide due to their promising physical properties and potential as active materials in future electronic, sensing, optoelectronic, and thermoelectric applications. A variety of devices, which have potential use for Si nanowires such as transistors [13–15], solar cells [16], chemical and biosensors [17], thermoelectric generators [18] and colour selective photodetectors [19] have been explored. The ultrafine semiconductor nanostructure in 1D structures can suppress the scattering and increase the mobility, which improves the transport properties of electron devices [20].

Silicon CMOS (complementary metal-oxide-semiconductor) has emerged as the predominant technology of the microelectronics industry. The ever increasing demand for higher speed, complexity and low power consumption has acted as a driving force for micro-miniaturization of MOSFETS [21, 22]. Although the bulk MOSFET device technology has been at the forefront for this miniaturization, the scaling of devices to nanometer regime has led to various short channel effects namely channel length modulation, drain induced barrier lowering (DIBL), hot carrier effect etc., resulting in poor electrostatic control over the channel. Various new technologies and device structures such as multiple gate structures [23], surround gate MOSFET [24], Si NW (Fin) FETs [25], tunnel FET [26] and technologies are being explored to minimize the short channel behaviour [14, 27].

In addition to the above, several research works have investigated the possible application of Si NWs as chemical and biochemical sensors [17]. The main driving force in the application of Si nanowires for sensing application has been the high surface to volume ratio, which opens up the potential to design sensors that are more sensitive than their bulk counterparts. Especially bio-sensors, where very small amounts of analytes have to be detected in very small volumes, can benefit from this feature. Si NW sensors work on the principle of conductivity modulation by electric field effects, where the charge at the surface of the NW modulates the free carrier concentration in the channel. A variety of sensors for gas, DNA, PH sensing, have been reported [28–33].

The Si based technology has dominated the industrial market for decades. Silicon-On-Insulator (SOI) is one of the most promising materials for next generation devices especially when combined with high-k dielectrics. SOI has a thin silicon film, called the device layer, that sits on top of an insulating layer of buried oxide (BOX), which itself sits on top of a bulk Si wafer. SOI is of tremendous technological interest as it offers a possible means to achieve improved device performance. SOI can provide low parasitic capacitance, which means it can reduce the power consumption compared to bulk Silicon [34] and reduce the overall leakage current. It can operate at low voltages and can provide ideal subthreshold slope and can operate in harsh environments such as high temperature and high radiation dose rate [35].
In the area of photovoltaics, the light trapping in solar cells is enhanced by forming radial structures, as pn junctions can be placed much closer to the carrier generation region, resulting in improved efficiency. Recently, Silicon wire waveguides based on SOI have emerged as a promising platform for highly integrated, ultra-small with complex functionality and increased performance and compatible with CMOS photonic integrated circuits. The large refractive index difference between Si and SiO₂ has made it possible to have single mode propagation and sharp bends waveguides, resulting in relatively smaller photonic circuits. The compatibility with CMOS processing has enabled integration of optical devices with waveguides for application in optical interconnects and communication [36, 37].

The fabrication of nanowires is based on two approaches namely bottom up and top down. The bottom up approach usually uses metal catalytic growth like the vapor-liquid-solid (VLS) mechanism which involves mainly three stages for nanowire growth i.e. metal alloying, crystal nucleation and axial growth. However, there are several issues with this approach. Difficulty in exact positioning, metal contamination and control of structure parameters are some of the issues that need to be considered for the fabrication of NWs. The bottom up method involves the synthesis of Si NW from a mass of Si wafer reacting with metal catalyst, while top down technique begins from a bulk Si wafer and brings down to preferred and required size and shape of these Si NWs using lithographic and etching processes.

Several investigations have been carried out in the past to investigate donor activation, surface roughness scattering and noise using data inferred from indirect measurements. So it is important to carry out direct Hall effect measurements. The study of temperature dependence on Hall voltage in Hall effect measurement aids to extract resistivity, carrier densities, and mobilities of these Si NWs to understand the physical transport mechanisms and interpret the underlying physics of transport in these NWs. Furthermore, most of these parameters are not only dependent on material properties but strongly depend on fabrication processes, therefore optimization of process parameters is of utmost importance for any meaningful conclusion.

For planar 2D structures, the electron concentration is commonly determined, very accurately, utilizing the quantum Hall-effect [38, 39] or Shubnikov-de Haas oscillations [40]. However, such measurements have not been able to achieve desired results for semiconductor nanowires, as fabricating the Hall bar geometry is difficult. So far, the most common method to determine the carrier concentration is the field-effect (FE) in a gated measurement geometry. As the source and drain tends to screen the gate potential in nanosize devices these measurements become uncertain. The density of surface states between the gate dielectric and the channel material affects the resulting value for the electron concentration dramatically. When the current pinch-off happens, all equilibrium carriers are
removed and the corresponding carrier concentration is calculated from the applied gate voltage and
the gate capacitance. Hence, the field effect measurement is an imprecise tool for study of transport
properties of NWs [2].

The other alternative method for the investigation of the transport properties of the NWs is the
Hall effect measurement [38] which is known to be more accurate compared to FE, current-voltage
(CV) measurement etc. [1, 6, 7]. A brief review of Hall measurements performed on single nanowire
is given in the section 1.2.

1.1 Thesis Outline

In this work, the main focus has been to develop optimized fabrication processes for making nanowires
of near ideal shape and size with reduced side wall roughness using top down approach, a methodology
to make side wall contacts and to carry out Hall measurements on a single NW. There is already
some work done in this area since 2012. During the last 6 years there have been many different
methodologies used for characterization of NWs having different shape and size. We have come across
a new methodology which has overcome some of the problems faced in these previous works. Mostly,
this work is done on highly doped materials and it has been said that going down on the scale of
sample size, would make the measurement more difficult. The technique which we have developed is
for rectangular-shaped NWs of sub 30 nm width and our samples are non-uniformly doped. The need
to design these methodologies is in response to the increasing demand of Si nanowires in electronic
deVICES.

This chapter provides a brief review of the work done in this important area of research (see
section 1.2 and 1.3). In the section 1.2 we have discussed some of the important findings on Hall
effect measurements carried out in the past on single nanowires and the problems faced during Hall
measurements. Chapter 2 contains the theory related with this work, which has been evolving the
field of physics for many years. In designing the methodology used in this project, lots of engineering
tools have been used. Chapter 3 presents the information and the working principle for these tools and
section 3.2 contains the information about the microscopy used for characterization of the Si NW and
Hall electrodes. In section 3.3, we present the measurement techniques used for the characterization
of single NWs.

Chapter 4 describes the processes used for fabrication of a single Si NW device. Our approach
towards optimization of two important fabrication processes namely the Electron Beam Lithography
(EBL), and dry etching are discussed. To fabricate the contact electrode a three-step EBL process is
used for the formation of the Hall electrode, metal is deposited at an angle using Si NW as a shadow mask. Chapter 5 contains the results obtained from the device, first time exploring the understanding of the metal and semiconductor contacts of rectangular shaped nanowire of sub 30 nm. The results in this chapter show the electrical DC measurement performed on Silicon NWs of different widths and the problems associated with measuring those NWs. Some of the problems encountered by us are similar to those faced by other groups mentioned in the literature section 1.2. To overcome these problems the Hall measurements have been done on these NWs. The results obtained from the Hall measurement on single Si NWs are presented in chapter 6. The two approaches used for the Hall measurement are magnetic field sweep and sample rotation with constant magnetic field. Chapter 6 also deals with the effects on Si nanowire due to temperature scan from room temperature to low temperature, 10 K. In chapter 5 and 6 the results of measured Si NW for transport data are compared with that of the film and Hall bar. In chapter 7 the conclusion and future work have been presented.

Hall measurement, when performed on a single nanowire can provide for the accurate determination of carrier concentration and mobility. These are the parameters which contribute in transport properties for the application of any electronic devices. There are important technological and technical challenges that need to be addressed to enable a wider deployment of this methodology.

1.2 Overview of Hall Measurements on Single Nanowires

This section provides a brief review of the research work carried out to investigate the transport behavior of nanowires. Figure 1.3 summarizes the past trends of research particularly dealing with the Hall effect measurements on NWs.

In 2012, the first nanowire fabricated for the Hall effect measurement had core-shell hexagonal shaped structure [1] as shown in figure 1.1 (a). The material used for the study was InP/ZnS as core/shell which is p-type/n-type grown by using the metal organic vapor phase epitaxy (MOVPE) technique, SEM image has been shown in figure 1.1 (b). These InP NWs are transferred to a silicon substrate for Hall effect measurement as shown in figure 1.1 (c). From their measured Hall voltage data, different values of carrier concentration along the nanowire are predicted, see figure 1.1 (d). Due to the non-uniform doping profile, their results show that the low doping region is dominated by Schottky contacts, which limit significantly the flow of current. At the junction between the shell and the core a depletion region would be formed, the depletion width varies with the core concentration gradient defining the effective electrical width thickness of the shell, see figure 1.1 (e). As the depletion width varies, the Hall signal also varies, see figure 1.1 (f). The applied magnetic field is 0.3 T and the
current is 100 $\mu$A. The smallest NW diameter is 80 nm. The contact electrode width is 300 nm. The Hall signal is observed to increase when the carrier density is reduced, and the measurements are thus expected to be limited by other factors such as contact resistance. For high doping concentrations the Hall signal decreases and the measurements are instead limited by the sensitivity of the measurement set-up [1].

In the same year, 2012, Hall effect measurement is performed on InAs NW [2] by using the same methodology as presented by [1]. InAs NWs are grown using MBE technique. The results obtained
from these measurements are used to evaluate quantitatively the charging effect of the interface and surface states. The Hexagonal shaped InAs NWs of width from 160 nm to 235 nm and length 2 µm are used for the measurements. These nanowires are mechanically transferred to the n-doped silicon substrate having thick layer of 200 nm of oxide on top of it. The EBL technique is used to pattern the Hall contacts and Ti/Au metal for contact formation as shown in figure 1.2 (a) & (b). The measurement is carried out in magnetic field of 0.5 T and current applied is in the range of 1 to 5 µA between source and drain. They have compared the efficiency of Hall measurement with the field effect measurement and showed that only 25% of charge carriers are involved in the conduction and rest of the induced charge ends up in the interface and surface states and does not contribute to electrical transport in the nanowire for FE measurements. Hence, Hall measurement is preferred choice to provide more accurate values of charge carrier density [2].

Figure 1.2: This figures depicts the research carried out on Hall effect measurements on InAs nanowire. Device used to measure Hall effect on single nanowires. (a) SEM of an InAs NW with source, drain and Hall contacts in top view (b) and under an angle of 35⁰. This wire is also of hexagonal shape (c), Resistance R between source and drain contacts both before and after electron exposure in the SEM. The extensive electron irradiation decreased the initial resistance of the InAs NWs by one to two orders of magnitude [2]. Reprinted from " Hall effect measurements on InAs nanowires"; Ch. Blmers, T. Grap, M. I. Lepsa, J. Moers, St. Trellenkamp, D. Gritzacher, H. Lth and Th. Schpers Appl. Phys. Lett. 101, 152106 (2012), with the permission of AIP Publishing

In 2013, the Hall devices were fabricated using the material MnSi and FeS₂ in a rectangular shaped semiconductor nanowire [3]. These NWs were drop casted on a Si substrate after their growth by using MBE technique. The smallest nanowire fabricated is of 150 nm thickness and 235 nm wide. The fabrication of above mentioned nanowire Hall devices required a highly engineered lithographic process. To utilize accurately and precisely position the Hall electrodes that only contact the nanowire on one sidewall facet and are separated by a distance of less than roughly 100 nm across the top nanowire facet, NWs are used as shadow mask for angled metal deposition. Ti/Au metal film for 40/30 nm thickness evaporated at an angle of 45⁰ is used as a Hall electrode. In this methodology, there is some offset of the Hall electrodes. Prior to the fabrication of Hall electrodes, the insulating layer of Al₂O₃ of 10 nm thickness is deposited on top of the NW to avoid the shorting of the Hall
contact during measurement. John P Degrave et al [3] have shown that the measurement without the insulating layer has resulted in Hall voltage close to zero. The applied magnetic field is 5 T. Multiple shaped nanostructures such as wire, rods and plates are compared for Hall measurement. Their results show that the measured Hall coefficient is independent of the dimension of the sample. As the Hall mobility is mostly dependent on the Hall coefficient, that is also deemed independent. This is attributed to the properties of the semiconductor material. In this approach, the electric equipotential offset is high since the Hall electrode are not exactly opposite to each other, which could have resulted in reduced sensitivity of the measurement.

In 2014, Muhammad M. Mirza et al [4] have carried out a systematic investigation on carrier transport in Si nanowires fabricated using top down approach. EBL and dry etch techniques have been employed to realize nanowires having average mean widths in the range of 4 to 18 nm. SOI substrates with uniformly doped device layer having doping level in the range of $2 \times 10^{19}$ to $20 \times 10^{19}$ cm$^{-3}$ and thickness of 50 nm have been used. Ni/Pt with thickness 20/50 nm has been used for metal contact and annealed in forming gas, to form silicides. The AC current source for Hall measurement technique is employed to minimize electron heating. The AC current source of 100 nA is applied at the frequency of 77 Hz and applied magnetic field is $\pm 1$ T. The geometrical accuracy of Hall measurement is observed to depend on the width of the voltage probe compared to the width of NW. Also the Hall voltage is observed to be small for heavily doped semiconductors. Mirza et.al.[4] have observed poor or no conductivity for the nanowires with widths below 12 nm and doping density of less than $2 \times 10^{19}$ cm$^{-3}$ indicating significant depletion effect at this doping level. The doping level of $8 \times 10^{19}$ cm$^{-3}$ is needed to avoid depletion effects in nanowires having widths around 4 nm. The non-ideal IV characteristics in low-doped device layer, similar to Coulomb blockade or single electron tunneling at low temperatures, is observed with an energy gap of $\pm 0.4$ V. This is predicted to be perhaps due to either Coulomb gap or as a result of the Schottky barrier formation at the source-drain ends of the channel. Large uncertainty in carrier density is predicted from Hall effect measurements carried out on Hall bars below 20 nm mean widths due to geometrical uncertainty. The carrier density value is estimated to be accurate to within a factor of 2 of the true value. Their results have shown the dimensionality effect in the transport of carriers. It is concluded that nanowires of average width of 18 nm and 12 nm show 3D, 7 nm as 2D and 4 nm show 1D transport behaviour. However, their nanowire structures have higher widths at the bottom as compared to the top, perhaps due to isotropic dry etching used, suggesting mixed dimensionality in transport of carriers. The 4 nm nanowire is actually 10 nm at the bottom and around 2 nm on the top and similarly all the samples have a triangular shaped structure. In order to investigate scattering mechanism taking
place in single Si nanowires, temperature dependence of resistivity, carrier density and mobility have also been studied. The resistivity and carrier concentration, consistent with bulk transport, are observed to decrease with temperature and hence, increase in mobility of silicon nanowire at low temperature is observed. The experimental mobility is directly compared with theoretically calculated total mobility using Matthieson’s rule. For this, various scattering mechanisms such as interface-roughness, neutral impurity, ionized impurity, acoustic phonon and longitudinal optical, non-polar optical phonon scattering have been considered. It is predicted that neutral impurity scattering rather than interface roughness scattering is the dominant scattering mechanism limiting the performance of Si NW. There is an advantage of having high quality passivated nanowire fabricated by top down over bottom up approach. The unpassivated nanowire grown from bottom up approach which is known to an issue of donor deactivation [4]. Later in 2017, Vihar Georgiev et al. [15] fabricated a junction less transistor using Si NW, following similar approach as [4] on a heavily doped substrate and observed increased drift mobility, compared to Hall mobility by a factor of two, this increase in drift mobility is due to the geometrical uncertainty of Hall test devices [4].

In 2014, same group in Lund University, Sweden [5] has investigated core-shell structures for InP doped with Sn, having hexagonal or similar to hexagonal shape of the nanowires. They have shown that the different shape and doping level affects the movements of Sn and In on the nanowire surface. The devices are fabricated by using the same methodology as [1]. For carrier concentrations below $10^{19}$ cm$^{-3}$, Sn has little effect on the dynamics of shell growth and the carrier concentration is homogeneous along the nanowire length whereas if the carrier concentration exceeds $10^{19}$ cm$^{-3}$ inhomogeneous carrier concentration and shell thickness is observed along the nanowire length. The reason for inhomogeneity is surface diffusion of the In and Sn species on the nanowire side facets that shift from [110] to [111] as the doping concentration increases [5].

In 2015, David Lindgren et al [6] have carried out micro-photoluminescence ($\mu$PL), cathodoluminescence (CL) and Hall measurements on single Zinc-blende InP core-shell pn-junction NWs. The degenerately doped n-type shell material has shown better results than doped by Sn [5]. The Hall devices are fabricated in a similar fashion as described by [1]. They confirmed that the Hall measurement is an accurate technique for the measurement of carrier concentration and mobility of the semiconductor devices which are highly doped and thick in size [6].

In 2016, Olof Hultin et al [7] have characterized Sulfur doped InP cylinder shaped nanowires by Hall, back-gate and top-gate field effect measurements. The nanowires are of 200 nm in diameter, 2.5 $\mu$m in length with different doping levels. Ti/Au-10 nm/210 nm is used for metal contact. The EBL technique is used to fabricate 8 contacts on nanowire. The measurements are carried out at
applied magnetic field of ± 2 T and applied voltage is ± 3 V. When the NW radius approaches the semiconductor Debye length, then diffusion current will play an important role and the charged layer caused by the Lorentz force acting on the charge carriers cannot be completely formed, this leads to a decrease in the Hall voltage [41]. Due to this effect the use of Hall measurements on very thin (20 nm) NWs with low doping concentrations of about $10^{17}$ cm$^{-3}$ is not very accurate one. Within this limit, the other problem associated with measurements on very small devices is to achieve a good contact to measure the Hall voltage with sufficient precision and defining contacts to the NW with sufficient spatial precision. Another effect that could strongly influence Hall effect measurements on nanostructures is the bypassing of current through the Hall terminals [42]. However, if the contacts are narrow and have relatively high contact resistance, this effect is negligible in the devices [7].

In 2017, Olof Hultin et al [8] presented a method to measure Hall effect in nanowires by 3 contact electrodes in order to make the fabrication of Hall test structures easier. The diameter of the nanowires is 65 nm. EBL technique is used to define the contacts. Three contact electrodes are fabricated. In order to measure the Hall voltage, the change in potential in one of the Hall contact electrode, on varying the magnetic field strength, as a function of time is observed. Over 300 voltage measurements has been taken in approximately 20 minutes to get each cluster of data points. The same growth and fabrication technique mentioned above is used for realizing Sn-doped InP NW [7] for the measurement. The contacts are made using Ti/Au (10/100 nm) at the top of the NW with an angle of 90°. The applied magnetic field is ±2T and current is 100 µA. They have confirmed reasonable agreement in the measurement data by comparing 4 contacts with 3 contacts devices. The Hall effect measurement in NW of low doped and thin NW is a very challenging task. In addition to fabrication challenges and the shunting effects, a thinner NW is more prone to get influenced by factors such as surface charges, and Schottky contacts formed on a low doped NW which could modify the physical structure and charge carrier concentration locally. The Hall voltage in thin NWs with low doping levels would be limited by diffusion currents. They presented this as an alternative approach which is developed during the course of our work.

The very latest article we came across in 2017, [9] deals with the measurement of Hall effect on InGaAs NWs. These NWs are selectively grown with a width down to 50 nm, and thickness 10 nm in a Hall bridge geometry. The metal Ti/Pd/Au is deposited on these NWs of thickness 10/10/80 nm. For Hall measurements, the applied magnetic field was ±2 T and the voltage sourced was 0.2 V. From these measurements the obtained result is that the magnitude of carrier concentration reduces with the width of the nanowire. From the Hall mobility measurements, it is concluded that for the NWs width above 200 nm, the mobility is constant at 1000 cm$^{2}$/Vs. For thinner NWs, less than 200 nm in
width, the mobility decreases with the width of NWs. It is due to the process involved in fabrication of NWs which has induced surface roughness. Lindelow et al [9] believed that a fully optimized EBL process for NW definition would reduce the side wall roughness and have a positive effect on electron mobility for the most scaled down device.

On measuring AC Hall effect on nanowire there are two new phenomena observed in [41], first one is the influence of diffusion currents in nanowires with radius comparable with the screening length of carriers and second is the presence of eddy currents in non-planar finite size Hall contacts. Both of these effects reduced the measured Hall voltage compared with the bulk samples and hence the effective carrier concentration determined by using standard formula may exceed the real concentration in NWs up to two orders of magnitude. In the framework of classical transport, the relationship between the measured Hall voltage and the carrier concentration is not the same as in bulk samples as it will depend on the NW radius. The solution of the above problem is to include corrections due to drift and diffusion by means of modeling. The other solution is to have rectangular-shaped NWs because non-rectangular shaped NW have a different potential at different points of NW surface. In thin NWs, lateral contacts inevitably do not have a point character, but occupy a noticeable part of the surface. Such contacts partially shunt the Hall voltage, and create eddy currents, this results in a decrease of the measured Hall voltage. Similar effects exist in in-homogeneous samples where they also result in decrease in the Hall voltage, with the one determined based on nominal impurity concentration and measured conductivity.

Barbut et al [42] have presented a theoretical work, to show that from the H-shaped nanostructure can provide a better accuracy for Hall effect measurement in NWs. However, this structure is questionable on the basis of concept of Hall voltage measurement because the Hall electrodes are made up of Si material itself with moderate difference in doping level.
1.3 Project Overview

In this investigation, we have carried out optimization of two critical fabrication processes, namely Electron Beam Lithography and Dry etch to fabricate Si NWs with nm dimensions and attempted sidewall contact for Hall structures. The main objectives of this project are to investigate the transport behavior in single Si NW through Hall effect measurement of carrier concentration and mobility as a function of the nanowire dimensions, and magnetic-field-strength independently of actual field-effect-transistor (FET) structure.

In most of the earlier research, we found that all the Hall contacts are opposite to each other and positioned on top of the nanowire. The ideal Hall contact should be deposited at the side wall of the nanowire and should not be shorting the contact with each other [3, 15, 42]. For this purpose, we have thermally cured and exposed the HSQ to convert into SiO$_2$ of few nm on the top of Si NW. Angled evaporation using Si NW as shadow mask has been used to make side wall contacts to Si NWs.
for fabricating Hall test structures. Similar, angled deposition technique has been done in 2013. The
figure 1.4 explains the fabrication process of Hall contacts. The only issue in this case is that the
Hall electrodes are not opposite to each other, therefore, the longitudinal resistance pick-up had to be
taken into account when extracting the Hall signal of the NW. This has influenced the measurement
accuracy to some extent.

In some early work reported on Hall effect measurements [4] their smallest Si NW structures have
near triangular shape with average width of 4 nm, see figure 1.5 (a) to (c), thus adversely affecting
the accuracy of their results due to geometrical uncertainty [15]. Perhaps the large proximity effect in
EBL at these dimensions could be responsible for deformation in shape of their nanowires. Whereas,
we have been successful in realizing near rectangular Si NWs using optimized fabrication parameters.

In this early reported work [4], Si NW device Hall contacts are also shorted [3, 42]. However, the
Hall mobility measured shows an increasing trend at 300 K while reducing the size of the NWs, figure 1.5 (d). By reducing the size of NW depending upon their carrier concentration, fabricated devices are fully depleted, see figure 1.5 (e).

Figure 1.5: These figures depict the research carried out on single Si NWs, using the technique of UV lithography to fabricate the Hall contacts. Hall mobility has been measured on different widths of Si NWs and of different carrier concentration. Cross-sectional TEM image of a Si nanowire fabricated by etching (a) with a 10 nm HSQ lithographically defined resist line after thermal oxidation and (b) with 30 nm HSQ lithography defined resist. The samples are surrounded by an amorphous Pt protection layer deposited by focus ion beam during the sample preparation for TEM. (c) SEM image of a 4 nm mean width Si nanowire with four terminal connections used to measure the mobility. Inset: a Greek cross with 12 nm probes used to measure the carrier density. (d) Mobility (squares) and carrier density (circles) as a function of temperature measured for Si nanowires with mean widths of 4 nm (green), 7 nm (red), 12 nm (blue), and 18 nm (black) all doped at $8 \times 10^{19}$ cm$^{-3}$. (e) Two-terminal resistivity measurements of nanowires with different widths for four different doping densities. For the lower doping densities, the smallest nanowires were fully depleted [4]. "Reprinted (adapted) with permission from (Muhammad M. Mirza et al "Determining the Electronic Performance Limitations in Top-Down-Fabricated Si Nanowires with Mean Widths Down to 4 nm"; Nano Lett., 2014, 14 (11), pp 60566060). Copyright (2014) American Chemical Society".

In this thesis, we report the results of Hall effect measurements carried out on single Si NWs of rectangular shape having different widths in the range of sub 30 to 500 nm. The Hall electrodes fabricated by using Si NWs as a shadow mask for angled metal deposition technique. The thin Si
NW have poor electrical conductivity, DC techniques showed non-ideal I-V behaviour indicating high resistance [4]. We also report the electrostatic analysis of a semiconducting NW, since we have a non-uniform distribution of NW dopants, and explore its effect on the resulting electrostatics. We observed a strong experimental evidence of doping distribution of NW and its significance. The non-uniform profile exhibits lower depletion widths, at the highly doped sidewall of NW. The existence of such doping profiles supports thin NW characteristics [43].

The DC Hall measurement of low mobility samples can result in poor signal to noise ratio [44, 45] and suffer from additional problems such as enhanced electro-migration, thermal gradients, thermo-electric effects, Seebeck voltages. Out of these factors, the ones that increase both the random and systematic uncertainties of the Hall measurement are particularly unpleasant, [46, 47] therefore here AC current sourcing has been used to minimize these problems. The main advantages of AC Hall effect measurement has been its ability to measure low mobility sample with greater resolution and reduced Joule heating and the elimination of some slow thermal effects.

Finally, performing AC Hall measurement on single silicon nanowires is considered to be challenging in general and on non-uniformly doped NWs in particular, but the methodology used in this investigation has been largely successful as reflected in our measurement and analysis results.
Chapter 2

Theory of Electronic Transport in Nanowires

Attractive features of semiconductor nanowires such as their ability to be integrated into electronic devices, novel sub-wavelength optical phenomena, their large tolerance for mechanical deformations and their high surface-to-volume ratio have been the main drive towards the study of their properties that are remarkably different from those of bulk materials [48]. Electronic properties of Si NWs depend on diameter, length, growth direction, chemical composition and doping level of the nanowires, which in turn influence the performance of devices made from these NWs. Small diameter Si NWs exhibit quantum confinement, which affects the effective mass of carriers and the band gap. Diameter of Si NWs and bandgap are in reverse relationship, so that, when diameter decreases, the band gap increases. Quantum confinement can also lead to other phenomena like negative differential resistance, linear magnetoresistance as well as conductance oscillations. In view of this, it is important to understand and directly measure the transport properties of Si NWs, in order to accurately test the theoretical predictions and also to exploit these properties for performance enhancement as the transport behavior can be much different from bulk Si.

Electronic transport of Si NWs based two terminal devices can be described using various properties. One such property is the conductivity, which can be changed by addition of impurities or dopants. An important cause of the degradation of the conductivity in Si NW based devices is the scattering process at the surface in presence of surface defects or surface roughness. Besides surface disorder, the other most critical source of scattering is the presence of impurities. In the semi-classical approach used to study the transport in bulk materials, impurities are point like centers that randomly scatter
the incoming carriers. This chaotic process slows down the carrier flow and results in reduction of conductivity.

Also, the resistance of the NW depends on how the inter electrode spacing of the device compares with some characteristic length scales determined by the nature of scattering processes encountered by charge carriers (electrons and holes) in the NW. In discussing transport in the NWs the length scales to consider are electron mean free path, localization length and phase coherence length. In addition, electron transport properties are also influenced by the type of contacts formed with Si NWs. This chapter deals with the theoretical basis of transport in Si NW in detail.

In order to understand the transport property of semiconductors it’s good to start from Drude’s model, which was derived for the understanding of metal conduction in 1897.

### 2.1 Drude’s Model

Drude model [49, 50], developed 3 years after J.J Thomson’s discovery of the electron, has a vast and great impact on the theory of the structure of the matter, this has suggested a mechanism of the conduction in metals. Based on Thomson’s discovery Drude had his theory of electrical and thermal conduction by applying kinetic theory of gases to a metal, considered as a gas of electrons. Drude also made the assumption that an electron is the charge carrier which conduct the electricity in a metal. For electrons there is a compensating positive charge i.e. ions, which are heavy and hence immobile. Using these assumptions, Drude derived the conduction of the electron in the metal.

Suppose an atom of the metallic element has a nucleus of charge $eZ$, $Z$ is the atomic number and $e$ is the electron charge, the electron density in metal is;

$$n = \frac{\rho_m Z N_v}{M}$$

(2.1)

where, $n$ is the number of electrons per cubic centimetre, $\approx 10^{22}$-$10^{23}$ cm$^{-3}$, $\rho_m$, Density of metal, $M$ Molecular weight of the metal, $N_v$ is the Avogadro’s Number.

The basic assumptions are such as [51]:

1. In the absence of applied electro-magnetic field electrons moved in a straight line. On applying the field, electrons follow the trajectory of applied external field as per the Newton’s law of
motion and neglect the electron-ion interactions. When they neglect the electron-electron interaction it is known as independent electron approximation and when they neglect the electron-ion interaction it is known as free electron approximation.

2. The interaction of electrons with ions is considered and electron-electron interaction is neglected. This scattering mechanism does not affect the conduction of metal severely and travels in a straight line. However, electrons experience a collision with a probability per unit time of $\frac{1}{\tau}$, $\tau$ is relaxation time or mean free time which means if one electron randomly experiences a collision, the average time before electron’s next collision is $\tau$.

3. The electrons reach thermal equilibrium by collision. The velocity of electrons just after the collision depends on the surrounding temperature. Electrons do not remember the velocity before the collision.

### 2.1.1 DC Electrical Conductivity of Metal

According to Ohm’s law, the current $I$ flowing in a wire is proportional to the potential drop $V$ along the wire, $R$ is the resistance of the wire,

$$ V = IR \quad (2.2) $$(1)

The resistivity $\rho$ is defined as a proportionality constant between electric field $E$ at a point in metal and the current density $J$ that it induces,

$$ E = J\rho \quad (2.3) $$

The shape and size of the wire is also essential in order to know the properties of metal. The current $I$ flows through a wire of length $L$, and cross sectional area $A$, since the potential drop along the wire is $V=EL$, using equations 2.2 and 2.3,

$$ R = \frac{L\rho}{A} \quad (2.4) $$

In absence of electric field, the average velocity of electron is zero, whereas on applying an external electric field $E$, an electron emerges out of collisions, in time $\tau$ after a collision the electron velocity changes to:

---

1$V$ stands for the voltage here.
\[ v_{\text{avg}} = \frac{-qE\tau}{m} \]  \hspace{1cm} (2.5)

In time \( dt \), the electrons will move the distance \( vdt \), so that \( nqEdt \) electrons will cross an area \( A \) perpendicular to the direction of flow, each electron carries a charge \(-q\), giving a current of,

\[ I = -nqvA \]  \hspace{1cm} (2.6)

Using equation 2.5, 2.3 and 2.6 and combining them, the conductivity can be derived as:

\[ \sigma = \frac{nq^2\tau}{m} \]  \hspace{1cm} (2.7)

And mobility can be defined as:

\[ \mu = \frac{\sigma}{qn} \]  \hspace{1cm} (2.8)

Drude model is used to extract the electrical conductivity parameters for Si film, Hall bar and NWs devices in chapters 5 and 6.6.

In 1927, Sommerfeld has combined the classical Drude model with quantum mechanics Fermi-Dirac distribution known as Drude Sommerfeld model [51, 52]. The free electron model was successful in describing the shape of electronic density of states, electrical and thermal conductivity of metals. But mainly, Fermi-Dirac occupancy for energies around the Fermi level. This model is also known as free electron model [53].

In classical model, the electron is considered as a gas and its total energy is sum of kinetic and potential energy,

\[ E = \frac{p^2}{2m} + V \]  \hspace{1cm} (2.9)

In quantum mechanics, the electron motion is also considered in a wave form, which is described from the Schrodinger wave equation [54], and it is expressed in two forms, time dependent and time independent.

\[ E\psi(r,t) = \left[-\frac{\hbar^2}{2m} \nabla^2 + V(r,t) \right] \psi(r,t) \]  \hspace{1cm} (2.10)

where, momentum operator is \( -i\hbar \partial / \partial x \) in quantum mechanics, \( \hbar \) is reduced Planck’s constant i.e. \( \frac{\hbar}{2\pi} \).

\[ V \] stands for potential energy here.

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Now consider a free electron gas in 1D structure as shown in the figure 2.1, neglecting the potential energy, an electron of mass \( m \) is confined to a length \( L \) by infinite barriers, it can be expressed as,

\[
E_n \psi_n = -\frac{\hbar^2}{2m} \frac{\partial^2 \psi_n}{\partial x^2}
\]

(2.11)

where \( E_n \) is the energy of the electron in the orbital,

\[
\psi_n = A \sin \left( \frac{2\pi x}{\lambda_n} \right) \quad \frac{n\lambda_n}{2} = L
\]

(2.12)

where \( A \) is constant,

\[
\frac{\partial^2 \psi_n}{\partial x^2} = -A \left( \frac{n\pi}{L} \right)^2 \sin \left( \frac{n\pi x}{L} \right)
\]

(2.13)

The energy \( E_n \) can be expressed by combining above two equations 2.12 and 2.13 as:

\[
E_n = \frac{\hbar^2 n^2 \pi^2}{2m L^2}
\]

(2.14)

Figure 2.1: First 3 energy levels and wave equations of a free electron of mass \( m \) confined to a line of length \( L \). The energy levels are labeled according to the quantum number \( n \) which gives the number of \( \frac{2\pi}{\lambda} \) in the wavefunction. The wavelengths are shown on the wavefunction. The energy \( E_n \) of the level of quantum number \( n \) is equal to \( \frac{\hbar^2}{2m} \left( \frac{n\pi}{L} \right)^2 \) [53].

Orbital is used to denote a solution of wave equations for a system of only one electron. From this we can separate between a quantum state of the wave equations and an approximate quantum state. The quantum state of wave equations is a system of \( N \) interacting electrons and an approximate quantum state is constructed by assigning \( N \) electrons to \( N \) different orbitals. Each orbital is a solution of a wave equation for one electron. The orbital model is exact only if there are no interactions between electrons. The boundary conditions are \( \psi(0) = 0 \) and \( \psi(L) = 0 \) imposed by infinite potential energy barriers. This is satisfied when wave functions are sine waves and when \( n \) is an integer and \( \lambda \) is the wavelength of the electron.
Let us say $N$ number of electrons are accommodated on the energy level. According to Pauli exclusion principle no two electrons can have same quantum number \[55\]. The number of orbitals with the same energy is called degeneracy. The energy level $E_F$ is the uppermost filled level in the ground state of the $N$ electron system, where we start filling the levels from the bottom ($n=1$) and continue filling the higher levels with electrons until all $N$ electrons are accommodated. For one dimension by substituting $n = \frac{N}{2}$ in equation 2.14, it can be written as,

$$E_F = \frac{\hbar^2 N \pi}{2m 2L^2} \tag{2.15}$$

As mentioned before Fermi-Dirac distribution is used to explain the temperature dependence of fermions. The equation 2.15 describes the state of the $N$ electron system at absolute zero temperature. The kinetic energy of the electron gas increases as the temperature increases. The Fermi-Dirac distribution gives the probability that an orbital at a given energy will be occupied by an ideal electron gas in thermal equilibrium,

$$f(E) = \frac{1}{\exp\left(\frac{E-\mu}{k_bT}\right)+1} \tag{2.16}$$

At absolute zero temperature $\mu = E_F$, when $E < E_F$ the function $f(E)$ is 1 i.e. filled states and when $E > E_F$ the function $f(E)$ is 0 i.e. empty state. On increasing the temperature when $E > E_F$, the Fermi function decays exponentially to zero with increasing energy and $E < E_F$ means that the Fermi function decays exponentially to zero with decreasing energy.

### 2.1.2 Failure of Free Electron Theory

The free electron model presents several inadequacies that are contradicted by experimental observation. Some inadequacies are mentioned below:

1. **Hall coefficient and Magneto-resistance** - The Hall coefficient fails to describe the dependence of magneto-resistance on magnetic field and temperature. The magneto-resistance model predicts that the resistance in a wire perpendicular to a uniform magnetic field does not depend on the strength of the field, which is not true. This diversity is not predicted by the model and can only be explained by analysing valence and conduction bands. Additionally, electrons are not the only charge carriers in a metal, electron vacancies or holes can be seen as quasiparticles carrying positive electric charge. The spin is mostly neglected in the free electron model and its consequences can lead to emergent magnetic phenomena like Pauli paramagnetism and
ferromagnetism.

2. **Directional** - The conductivity of some metals can depend on the orientation of the sample with respect to the electric field. Sometimes even the electrical current is not parallel to the field. This is because the model does not integrate the crystallinity of metals, i.e. the existence of a periodic lattice of ions.

3. At intermediate temperature **Wiedemann-Franz law** fails free electron theory.

4. **Temperature dependence** - The free electron model presents several physical quantities that have the wrong temperature dependence, or no dependence at all like the electrical conductivity. The thermal conductivity and specific heat are well predicted for alkali metals at low temperatures, but fails to predict high temperature behavior coming from ion motion and phonon scattering.

In order to overcome these difficulties there was a need for a new modified model, which was developed by Bloch in 1928 to extend the understanding of the behavior of electrons in crystal lattices, ferromagnetism, and nuclear magnetic resonance [56]. The Bloch theorem underlines the concept of electronic band structure, discussed in section 2.2.

### 2.2 Electronic Band Structure

In order to overcome the failure of free electron model a new model was studied, named as nearly free electron model. It is a quantum mechanical model of physical properties of electrons that can move freely through the crystal lattice of a solid. This model aids in describing the electronic band structure of metals, semiconductors and insulators.

To study the transport properties of solids, it is required to understand how electrons respond to an applied electric field. Electrons in crystal are arranged in an energy band. The transport properties of the solids depend on these energy bands. The energy band diagram shown in the figure 2.2 classifies the solids in semiconductor, metal and insulator. Semiconductors are different from metals and insulators, as the conduction band is almost empty and valence band is almost full.
2.2.1 Effective Mass

The mass of free electrons in energy band can be simplified as effective mass, it can be defined as

\[
\frac{1}{m^*} = \frac{1}{\hbar} \frac{\partial^2 E}{\partial k^2}
\]

(2.17)

The conduction band energy in \(k\) space depends on the effective mass. For direct band (parabolic representation) it is defined as;

\[
E(k) = E_c + \frac{\hbar^2 k^2}{2m^*}
\]

(2.18)

where \(E_c\) is the conduction band-edge at minima.

In the indirect band gap materials conduction band is either \(s\) and \(p\) mixture (longitudinal) or \(p\)-type (transverse), whereas, direct band gap is purely \(s\)-type [57].

\(E(k)\) for indirect band along a particular axis can be defined as,

\[
E(k) = E_c + \frac{\hbar^2 k^2}{2m^*_t} + \frac{\hbar^2 k^2}{2m^*_l}
\]

(2.19)

where, \(m^*_t\) and \(m^*_l\) are the transverse effective mass and longitudinal effective mass respectively.

Here valence band is the band which is full of electrons and a mixture of few degenerate states as shown in the figure 2.3. It has top three bands which are sub-divided into heavy holes, light holes and split off bands. These bands are made of \(p\)-orbitals and degeneracy at the point of the \(p\)-states forming the top of valence band, which is lifted with increasing dopants. This effect is due to spin orbit coupling of the electron spin \(s\) to the orbital angular momentum \(l\). So the total angular momentum is \(j_z = l + s\). Since orbit angular momentum of \(p\)-states is \(l=1\) and magnetic spin quantum number \(s\) for spin down and spin up is \(\pm \frac{1}{2}\). Angular momentum is \(|l - s| < j < l + s\) which gives rise to two bands at two different energy levels \(p_{\frac{3}{2}}\) and \(p_{\frac{1}{2}}\). The \(p_{\frac{3}{2}}\) derived band have more energy than split off bands.
band derived from $p_2$ by the spin splitting energy $\Delta_{so}$. This energy increases with atomic number or dopant because electron at the orbit experiences an internal atomic magnetic field [59]. The band at higher energy $p_2$ is quadruply degenerate at $\Gamma$, whereas split off band at $p_4$ is doubly degenerate. As the radius of the curvature of the band is inversely proportional to the effective mass the two higher bands at $p_2$ states are called heavy holes and light holes [60].

The table 2.1 gives the values of effective mass used for the calculation of transport properties of the carriers.

<table>
<thead>
<tr>
<th>Property</th>
<th>Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m^*_{L}$</td>
<td>is the longitudinal effective mass</td>
</tr>
<tr>
<td>$m^*_{T}$</td>
<td>is the transverse effective mass</td>
</tr>
<tr>
<td>$m_{hh}$</td>
<td>is the heavy holes effective mass</td>
</tr>
</tbody>
</table>

Table 2.1: Effective masses in the silicon band structure
2.2.2 Definition of Bulk (3D), Quantum Well (2D), Quantum Wire (1D) and Quantum Dot (0D)

It can be seen from the figure 2.4 that when the active layer has all three dimensions larger than the de-Broglie wavelength of the carriers, it shows bulk behavior and density of state shows parabolic distribution. Quantum well is realized by reducing the active layer thickness to two dimensions. The corresponding density of state function becomes a step type function due to confined electron motion in the \( z \)-direction. Similarly, one can further limit the motion of the carriers in \( y \)-direction by reducing the size, resulting in quantum wire structure. In this case the density of state function becomes almost like discrete spikes. Finally, if one further limits the carrier motion in \( z \)-direction, the density of state function is truly discrete known as quantum dot structure. Bulk behavior in electronic transport of Si device is studied and by using the top down fabrication methodology, the device is thinned down to 1-D. However, the transport behavior of carriers still behaves as 3-D. The effective physical length reduces to 1-D and it results in transport behavior similar to quantum wire.

![Diagram illustrating the electronic density of states depending on their dimensionality](image)

2.3 Carrier Transport Theory

The three primary types of carrier actions which occur inside the semiconductor are drift, diffusion and recombination-generation, and these are described in this section. A brief description of carrier
transport in non-equilibrium conditions is also given below.

### 2.3.1 Drift and Diffusion

On applying electric field across a semiconductor material, the resulting force on the carriers tends to accelerate the charge such as holes in the direction of applied electric field and electrons in the opposite direction. During the motion of charge particles these carriers will collide with the ionized impurity and thermally excited lattice atoms, hence the acceleration would be interrupted and carriers would be scattered [62]. For a $n$-type semiconductor the current, $I_n$, flowing within the semiconductor as a result of carrier drift is given as,

$$ I_n = qnv_d^dA \quad (2.20) $$

At high electric field $v_d$ saturates and becomes independent of $E$,

$$ v_d = \frac{\mu_0 E}{1 + \left( \frac{\mu_0 E}{v_{sat}} \right)^\beta} \quad (2.21) $$

where, $\beta$ is 1 for holes and 2 for electrons, $\mu_0$ is constant of proportionality between $v_d$ and $E$ at low to moderate electric fields, $v_{sat}$ is the saturation velocity approached at high fields.

Substituting the value of drift velocity for $n$-type semiconductor, given in equation 2.5, into equation 2.20 we get equation 2.22,

$$ \vec{J}_n = q\mu_n n^d E \quad (2.22) $$

And here $\mu_n$ is mobility, details are given in section 2.4.1,

$$ \mu_n = -\frac{q\tau}{m^*} \quad (2.23) $$

When the spatial dimension of the semiconductor are reduced to nanoscale the equation 2.21 is no longer valid as velocity overshoots [63].

Diffusion process tends to redistribute the random thermal motion of carriers from high concentration region to low concentration region. The current density due to diffusion in $n$-type semiconductor material obeys the Fick’s law [64] and is given as,
\[ J_n = qD_n \nabla n \]  

(2.24)

Using Einstein relationship for electrons, the diffusion coefficient \( D_n \) for \( n \) type semiconductor can be written as:

\[ D_n = \frac{\mu kT}{q} \]  

(2.25)

The total current in the semiconductor is sum of drift and diffusion current given in equations 2.22 and 2.24, under equilibrium condition. Einstein relationship given in equation 2.25 is used for non-uniformly doped semiconductor [62]. The electron concentration gradient increases in non-uniformly doped sample under equilibrium conditions, also results in electron diffusion current flowing in the one direction. Hence, there would be a built-in electric field oriented in the opposite direction, which would give rise to a drift current [62].

### 2.3.2 Recombination-Generation (R-G)

R-G events occur in semiconductor materials during the motion of the carriers. Recombination is the process whereby electrons and holes are annihilated and destroyed. Generation is a process whereby electrons and holes are created. R-G occurs between energy levels of band structure such as between valance band and conduction band. The addition of dopants such as P (\( n \)-type) and B (\( p \)-type) will shift the energy level and create traps for carriers between the valence band and conduction band. These energy levels are known as donor level (\( n \)-type) and acceptor level (\( p \)-type), as shown in figure 2.5, where R-G process takes place and is known as indirect recombination. R-G process always occurs in semiconductors, both optically and thermally, and their rates are in balance at equilibrium. The product of the electron and hole densities (\( n \) and \( p \)) is a constant \( n_o p_o = n_i^2 \) at equilibrium, maintained by recombination and generation occurring at equal rates. The \( n_o \) and \( p_o \) are equilibrium values, \( n_i \) is intrinsic. When there is a high concentration of carriers (\( np > n_i^2 \)), the rate of recombination becomes greater than the rate of generation, driving the system back towards equilibrium. Similarly, when there is a low concentration of carriers (\( np < n_i^2 \)), the generation rate becomes greater than the recombination rate, again driving the system back towards equilibrium [65]. As the electron moves from one energy band to another, the energy and momentum that it has lost or gained must go to or come from the other particles involved in the process.
2.3.2.1 Auger Recombination and Generation

This process occurs between the collision of two like carriers and energy is transferred during the collision to the surviving carrier. Such as, an electron from the conduction band moves to the valence band neutralizing a hole in the valence band. The excess energy is transferred to an electron in the conduction band. Other possibility, in a similar process the excess energy is transferred to another hole in the valence band. In Auger generation process an electron is excited directly from the valence band into the conduction. When a highly energetic hole from the valence band transfers its energy to an electron in the valence band, which is then excited to the conduction band generating an electron-hole pair. This process mainly takes place in highly doped semiconductor material.

2.4 Transport Theory of Semiconductors

The theory of electron transport in semiconductors has become increasingly sophisticated over the years following the invention of the transistor. New phenomena have been discovered and new devices have been engineered; our ideas about transport regime and scattering mechanisms have matured, which is briefly described in the sections 2.4.1 and 2.4.2. We have seen the relationship between mobility and scattering time in equation 2.23.

The use of silicon semiconductor material in electronics devices is high in demand due to its extraordinary transport properties. Silicon belongs to group IV of the periodic table. In single crystal form, it adopts the diamond lattice structure, with each atom covalently bonded to four nearest neighbor atoms in tetrahedral configuration. The electrons present in outermost shell are known as valence electrons located at the uppermost energy level of valence band and separate from the conduction band. This conduction band consists of energy level which is unfilled, these two bands are separated from the energy of 1.1 eV known as energy gap. Si is an indirect bandgap semiconductor. The invention of the transistor gave rise to a tremendous amount of research on the properties of highly
purified single crystals of various semiconducting materials, as a result of which our understanding of the energy bands and scattering mechanisms in such relatively perfect crystals is quite advanced. However, much less attention has been paid to heavily doped semiconductors. The properties of these materials are still in need of detailed study. The purpose of this work is to present some new electrical and Hall effect data in highly doped Si NW.

2.4.1 Mobility

The force exerted on the electrons is proportional to the applied electric field \( E \).

\[
\vec{F} = q \vec{E} \quad (2.26)
\]

\[
\vec{F} = m \vec{a} \quad (2.27)
\]

In equilibrium state,

\[
m \vec{a} = q \vec{E} \quad (2.28)
\]

In equilibrium state when there is no applied external electric field, the charge carriers move in random direction with velocity \( \vec{v}_d \). Collisions occur between charge carriers in time \( \tau \), this provides some acceleration \( a \) to the carriers.

This above equation 2.28 can be rewritten as:

\[
\frac{\vec{v}_d \tau}{\tau} = \frac{q \vec{E}}{m} \quad (2.29)
\]

The amount of distance covered by electrons or holes in one second is known as drift velocity \( \vec{v}_d \), as expressed in equation 2.5. Under the influence of electric field \( E \) charge carriers moved with a drift velocity \( \vec{v}_d \) within the solid. This is characterized as mobility \( \mu \). Its unit is expressed in cm\(^2\)/Vs.

\[
\vec{v}_d = \mu \vec{E} \quad (2.30)
\]

In a material electrons and holes move with velocities associated with kinetic energies and the charge carriers have an energy distribution as given by the Fermi-Dirac distributions.

\[
\vec{v}_d = \frac{q}{m^3} \vec{E} \tau \quad (2.31)
\]
\( m^* \) is the projection of longitudinal effective mass.

Mobility depends on drift velocity and is determined by scattering time \( \tau \), equation 2.32 tells us how long the carrier is ballistically accelerated by the applied external force until it scatters, which changes its direction and energy.

\[
\tau = \frac{m^* \mu}{q}
\]  

(2.32)

The presence of impurities and dopants, lattice defects etc. is primary contributor of scattering. A series of scattering events can be visualized as generating a random walk resulting in no net flow of charge carriers at equilibrium conditions. On applying the electric field this random walk will move in a direction of the field, and on moving an electron can collide with other electrons and lose its energy. But on interacting with one electron the other electron will gain energy and the drag force will be experienced in opposite direction, which eventually reduced the mobility in the material. The detailed description on scattering theory and types of scattering is given in section 2.5.

The change in momentum for the electrons can be expressed as \( p=mv \). The value of \( v \) is replaced by the drift velocity, \( v_d \), by substituting the equation 2.29. The applied force is equal to the change in momentum due to scattering, and it can be expressed as equation 2.33.

\[
\Delta p = qE\tau
\]  

(2.33)

Before collisions or experiencing any scattering the charge carrier will cover some distance. This distance defines the transport property of any material known as mean free path. The longer the path the better device efficiency would be. This is briefly described in the section 2.4.2.

### 2.4.2 Characteristic Length Scales and Transport Regime

The electronic transport mechanisms in semiconductor and metal are defined in terms of transport regime, various characteristic length scales and scattering mechanisms. A brief description relevant to transport in nanostructured materials and devices is discussed below.

#### 2.4.2.1 Diffusion Length

The length an electron travels after the collision and before it is disrupted by scattering events. It is defined as;

\[
l_D = \sqrt{D\tau}
\]  

(2.34)
2.4.2.2 Debye Length, $L_D$

The distance over which the charge separation can occur. It limits the electrostatic interactions between the charged particles. It is defined as,

$$L_D = \sqrt{\frac{\epsilon_r \epsilon_0 V_T}{qN_D}}$$  \hspace{1cm} (2.35)

where, $\tau$ is the scattering time, $D$ is the diffusion constant, $l_D$ diffusion length, $\epsilon_r$ relative permittivity, $\epsilon_0$ permittivity of vacuum, $V_T$ thermal voltage and $N_D$ carrier density.

2.4.3 Transport Regimes

In this section, we will briefly discuss the types of transport that can occur in the active region of the semiconductor device based on their size and shape. Consider a rectangular shaped semiconductor channel of length $L$ and width $W$ and thickness $t$. In bulk the type of transport that takes place is diffusive. In figure 2.6 (a) the mean free path $l_e < W < L$, which means the scattering events are higher. Figure 2.6 (b) shows the Quasi-Ballistic and Ballistic transport which occurs in nanostructures due to the size confinement and the scattering events are reduced. For Quasi-Ballistic $W < l_e < L$, the transport is ballistic in one and diffusive in other dimension, whereas for Ballistic $W < L < l_e$, electrons are not supposedly scattered within the active channel. From figure 2.6 (c) one can see the quantum mechanical tunneling, where the electrons tunnel through the barrier without any hurdle [66]. However, the figure 2.6 (d) is the most realistic case for the nano-structured active channel. In this case, ballistic transport will be dominated by few scattering events mainly by interface roughness scattering especially if the device is fabricated by top-down approach. The scattering mechanisms influence the transport properties of the device, which has been briefly discussed in the section 2.5.
2.5 Scattering Theory

The nature of interactions of electrons and holes can be determined from mobility of semiconductor material. The mobility for any absolute temperature can be calculated from Einstein relation, given in equation 2.25, but it does not provide any further information to determine any specific scattering mechanism. Here we will discuss briefly some of them which are related with highly doped nano-structured material, such as ionized impurity scattering, neutral impurity, electron-electron scattering, acoustic phonon, optical phonon, electron-phonon and surface or line edge roughness or interface roughness scattering. For degenerately doped semiconductors, Fermi level will lie inside the conduction band of the nano-structure and to account for this into the calculations, the effective mass ($m^*$) is defined to include a non-parabolic factor [67], see section 2.2.1 and 2.1.

2.5.1 Ionized Impurity Scattering

The addition of dopants as substitutional impurity atoms into the Silicon lattice results in point defects which act as charge traps or become ionized and lose energy. Also the interstitial point defects can trap charge and become ionized. Both of these point defects have a huge impact on mobility. For $n$-type dopants the phosphorous is added which brings the energy state near the conduction band
in forbidden energy gap, so the dopants are thermally ionized, donating a mobile electron to the conduction band and creating an immobile cation at the dopant site. Coulomb interaction between free charge carrier and fixed charge dopant sites have enormous effect on electron scattering resulting in reduced mobility. Doping level of $10^{19}$ cm$^{-3}$ results in mobility for electrons $\approx 100$ cm$^2$/Vs and for holes $\approx 50$ cm$^2$/Vs [68]. In semiconductor nanowires, these effects are restricted to quasi-1D [69]. At low temperature, the carriers' motion is slowed down due to low thermal energy. Hence, the effect of ionized impurity scattering decreases with increasing temperature due to the average thermal speeds of the carriers being higher [63].

### 2.5.2 Neutral Impurity Scattering

The neutral impurity scattering dominates at low temperature. Ionized impurities become neutral due to carriers freezing out and conduction electrons no longer emit photons due to low thermal energy [70].

### 2.5.3 Electron-Electron Scattering

Electron scattering occurs when electrons change their path due to the applied external force that can be electrostatic forces within matter or interaction with magnetic field. On applying magnetic field the electron may be deflected by the Lorentz force which results in scattering. This is also known as Coulomb scattering. Due to the Pauli exclusion principle, electrons can be considered as non-interacting if their density does not exceed the value $10^{16}$-$10^{17}$ cm$^{-3}$ or electric field value $10^3$ V/cm. However, significantly above these limits electron- electron scattering starts to dominate. Long range and non-linearity of the Coulomb potential governing interactions between electrons make these interactions difficult to deal with.

### 2.5.4 Surface Scattering

In quasi-1D nanowire the surface to volume ratio increases as dimensions are reduced which results in structural in-homogeneity and limits the mobility due to quantum confinement charges being confined in one dimension and this creates energy-quantized states. However, it has been found in silicon nanowires that the surface roughness term does not become important until the wire diameter is below 10 nm [71]. But there is an influence of line edge roughness on the Silicon nanowire which would lead to scattering. This type of scattering occurs due to the edges of the structure of nanowires which are not straight due to the limitation of the EBL. The variation in the Silicon nanowire width leads to
spatial variation in the band-gap, and the fluctuations in the band-edges cause carrier scattering and hence reduced mobility [72].

2.5.5 Phonon Scattering (Lattice Scattering)

A phonon is a packet of waves which can travel throughout the crystal with a definite energy and momentum, so in the quantum mechanical description these waves are treated as particles. Any solid crystal consists of atoms bound into a specific repeating three-dimensional spatial pattern called a lattice. Because the atoms behave as if they are connected by tiny springs, their own thermal energy or outside forces make the lattice vibrate. Due to lattice vibrations, this scattering dominates at high temperature which is caused due to excessive thermal energy and this reduces at lower temp.

2.5.6 Electron Phonon Scattering

When electrons accelerate, the probability of emitting a phonon is high and as a consequence of repeated phonon emission the electrons are not able to increase in net velocity with increasing electric field. Like electrons, phonons can be considered to be particles. A phonon can interact with an electron and scatter it. In nano-structures, an electron is considered as a wave when the wavelength of the electrons is larger than the crystal spacing, the electrons will propagate freely without any collision. Mainly in electron-phonon interactions energy is exchanged. Phonons are quasi particles and carry momentum. As electrons and phonons collide and scatter, their energy exchange gives rise to momentum differences. This means electron momentum can change allowing scattering between different energy valleys in the electronic band structure due to phonon scattering. These scattering processes, depending on the nature of the electron’s momentum change along the single axis during a scattering event also known as intervalley scattering. At higher temperature, there are more phonons, and thus increased electron-phonon scattering, which tends to reduce mobility. In lightly doped semiconductors Jie Zou et al [73] observed that the phonon-electron scattering does not have a strong influence on the lattice thermal conductivity. However, for higher carrier concentrations, phonon-electron scattering becomes important, reaching the level of other relaxation mechanisms.

2.5.7 Acoustic Phonon Scattering

The acoustic phonon scattering mechanism is based on lattice vibrations that occurs due to phonon induced strain in the material. Due to these vibrations there will be a shift in potential known as deformation potential. This will disrupt the band structure and change the crystal potential which
changes the lattice spacing and hence varies the lattice constant [74]. The mobility due to this scattering depends on the temperature and electron density [63].

The mobility values affected by the scattering process in this study are discussed in details in chapter 6.

2.6 Contact Effects

To efficiently connect the semiconductor devices to the outside world, metal contacts must be used. Two types of contacts are often used: Ohmic contacts and rectifying or Schottky contacts. In ideal Ohmic contacts, the current varies linearly with the applied voltage and it is implicitly assumed to have low resistance. Schottky contacts, however, should have very low resistance in forward direction and an infinite resistance in reverse direction, similar to diode characteristics. The current across a Schottky diode is determined by thermionic emission i.e. the carriers in this case have sufficient energy to surmount the barrier. The formation of Ohmic contacts, requires high doping level and reduced width of depletion layer where the carriers can tunnel through the barrier rather than being limited by thermionic emission over the barrier. A brief description of underlying physics of contact formation is discussed in this section and in section 2.7. The problems faced in contact formation to Si NWs and its effect on conduction mechanism, observed during this investigation, are given in chapter 5.

2.6.1 Schottky Contacts

The energy band diagram for the formation of metal and semiconductor contacts, assuming both of them are electrically neutral and separated by an insulating layer and also do not have any surface states present, is shown in the figure 2.7.

![Figure 2.7: Schematic diagram of contacts between metal and semiconductor with an insulating layer of δ [75].](image-url)
If n-type silicon has a work function $\phi_s$ which is less than metal work function $\phi_m$, then in order to equalize the Fermi level $E_F$ electrons will flow from Si to metal as shown in figure 2.8, resulting in band bending and formation of depletion region at the interface. The current transport across such contacts is determined by their barrier heights. The barrier height by definition is the energy difference between the Fermi level and the edge of the majority carrier band of semiconductor.

Figure 2.8: Schematic diagram of formation of the barrier between metal and semiconductor when insulating layer $\delta$ is reduced [75].

Rectification in metal and semiconductor contacts was first discovered by Barun in 1874 [76]. The observation of depletion layer at the semiconductor interface was done by Schottky and Mott in 1938 [77–79]. Depletion region is formed near the surface of the silicon by accumulating positive charge which is uncompensated. The width of this region is $w$. There is negative charge at the surface of metal which is balanced by the positive charge at the silicon surface. $V_i$ is the difference between the electrostatic potential outside the surface of the metal and Silicon, $V_i = \delta \xi$ where $\delta$ is the separation and $\xi$ is the field in the gap between conduction band and Fermi level. The schematic diagram of this formation is shown in figure 2.8. The amount of energy by which the bands are bent is $V_{d0}$. The height of the barrier is measured from the Fermi level to the surface of the band bending, as shown in the figure 2.8, which is given in the equation 2.36 below:

$$\phi_b = \phi_m - \chi_s$$  \hspace{1cm} (2.36)

where electron affinity of silicon is $\chi_s$, $\phi_m$ is the work function of the metal and $\phi_b$ is the barrier height. There are a few assumptions made before the calculation, such as semiconductor is homogeneous to the boundary of the metal so that the space charge will be created at the depletion region. The electric field strength increases linearly with the distance from the edge of the depletion region.
The magnitude of the electrostatic potential will increase quadratically, and the resulting potential barrier will be parabolic in shape. This barrier is known as Schottky barrier. The calculations of barrier height between the metal and the silicon is given in chapter 5.

However, achieving the ideal contact situation as shown in figure 2.9 is not practically possible, there will always be a few nanometer of insulating layer of oxide through which electrons can tunnel. The above equation 2.36 is referred to as Schottky Mott limit [75].

![Figure 2.9: Schematic diagram between metal and semiconductor with no insulating layer, δ is zero [75].](image)

For n-type silicon, if the work function is $\phi_s \ll \phi_m$, the bands will bend downwards and result in depletion region as shown in figure 2.9. If $\phi_m \ll \phi_s$, the bands bend upwards, electrons flow from semiconductor to the metal, resulting in better Ohmic contacts.

The barrier height does not depend strongly on metal work function due to the presence of localized surface states. In 1947 Bardeen [80] derived a relation for this case which is given in equation 2.37 as follows:

$$\phi_b = E_g - \phi_0$$  \hspace{1cm} (2.37)

These are states present at the surface of semiconductor when forming the contacts with the metal. Their electronic structure at surface is slightly different from bulk. At the surface, the atoms are bonded on one side and free on the vacuum side which is known as dangling bond. So each surface atom is associated with the unpaired electrons in a localized orbital. Surface states form two dimensional bands which may overlap the valence and conduction bands. Such overlapping surface states would differ from valence and conduction states which extend through the bulk. The surface states mainly depend on the location of the atoms at the surface and it is also influenced by the reconstruction of the surface. A condition of no net charge on the surface atoms may correspond to a
partial filling of these states. In case, the density of surface levels is sufficiently high, then there will be a formation of double layer which consists of a net charge from electrons in surface states and a space charge of opposite sign. According to the Fermi-Dirac distribution, the charge on these surface states depends on the position of the Fermi level $E_F$. At absolute zero temperature the states below Fermi level are occupied and above are empty. The position of the Fermi level when the surface is assumed to be electrically neutral is known as neutral level $\phi_0$. The position of the neutral level may change, it can lie in the bands or in the gaps between the bands depending upon the surface states. If states below $\phi_0$ is empty the surface has positive charge (donor-like), if states above the $\phi_0$ is full the surface has negative charge (acceptor-like). In case when $\phi_0$ lies between the occupied and the unoccupied bands of the surface states and if the Fermi level does not match with the neutral level then there will be a net charge at the surface. This will produce an electric field in the semiconductor which can cause the bending of the energy bands. If the surface charge is positive, bands will bend downwards near the surface and the majority carrier concentration will be increased and the region of the semiconductor will be accumulated. If the surface charge is negative the band will bend upwards near the surface and the region will be depleted.

As stated by Schottky-Mott limit [77], [78], the semiconductor is separated from a metal by an insulating layer of oxide. There will be a distribution of surface states at the interface of semiconductor and the insulator, which is characterized by $\phi_0$ neutral level. These surface states would be known as interface states. Let’s assume the negative charge on the surface of metal is $Q_m$, the positive charge at the semiconductor is $Q_d$ and in case if there is a presence of surface states its charge is referred as $Q_{ss}$, then the electrically neutral condition is $Q_m + Q_d + Q_{ss} = 0$.

If no field is applied then the occupancy of the surface state can be determined by the Fermi level, since it is constant through the barrier region. If neutral level $\phi_0$ is above the Fermi level $E_F$, then surface states contain net positive charge due to which $Q_d$ becomes smaller. $Q_d$ is small on comparing with when no surface states are present. The reduction in $Q_d$ means reduced barrier height, reduced depletion region $w$ and hence the amount of band bending is also reduced. The reduction in barrier height will result in pushing the $\phi_0$ towards $E_F$, this tends to reduce the positive charge in the surface states.

If neutral level is below $E_F$ then $Q_{ss}$ is negative and $Q_d$ is greater on comparing with when no surface states are present. Hence, this increased the barrier height and depletion width $w$ and neutral level is pulled up towards the $E_F$.

The section 2.7 describes the conduction mechanism between metal and semiconductor junction under applied bias. The current transport will occur in four ways and its mechanisms are briefly
2.7 Conduction Mechanisms

In this section the ways through which electrons can conduct across the metal and semiconductor junction are covered. There are four ways in which current can conduct (as shown in the figure 2.10) under forward biasing such as: (a) emission of electrons from the semiconductor over the top of the barrier into the metal i.e. thermionic emission (b) quantum mechanical tunneling through the barrier i.e. field emission (c) recombination in the space-charge region (d) recombination in the neutral region (hole injection).

![Figure 2.10: Schematic diagram of transport process in a forward biased barrier between metal and semiconductor [75].](image)

2.7.1 Emission over Barrier

Among these four types of transport the majority of the electrons are transmitted from semiconductor to metal over the barrier, they need to transport through the depletion region of the semiconductor. The motion of electrons is determined by the mechanism of drift and diffusion. The first theory of conduction was diffusion theory by Wagner in 1931[81], Schottky and Spenke in 1939 [82]. According to this theory, current is limited by drift and diffusion in the depletion region. Assumption is made that the electrons in semiconductor adjacent to the metal are in thermal equilibrium with the metal.

Another theory, introduced by Bethe et al [83] in 1942, known as thermionic emission theory proposed that the current is limited by the emission process, and assumptions are made that the quasi Fermi-level for electrons remains flat throughout the depletion region. At the interface of metal
and semiconductor there will be a flow of electrons from the semiconductor to metal to equalize the Fermi-level. These electrons, known as hot electrons, penetrate into the metal and they lose their energy due to the collisions.

According to the diffusion theory the limitation for the current flow is the effects of drift and diffusion in the depletion region. Whereas according to the thermionic emission theory the limitation is in the process of emission of electrons in the metal. Practically, both have the combined effect.

According to the diffusion theory current density in the depletion region can be written as equation 2.38

\[ J = qD_n \frac{\partial n}{\partial x} \]  

(2.38)

where, \( n \) is the concentration of electrons in \( n \)-type semiconductor, \( \mu \) is mobility, \( D_n \) is diffusion constant, \( E \) is electric field in the barrier and \( q \) is the electron charge.

By introducing the quasi Fermi level for electrons \( \zeta_n \), the concentration of electrons can be defined as equation 2.39:

\[ n = N_c \exp\left(\frac{-q(E_c - \zeta_n)}{k_B T}\right) \]  

(2.39)

where, \( N_c \) is effective density of states in the conduction band, and \( E_c \) is the bottom energy level for conduction band.

Using Boltzmann approximation to the Fermi-Dirac distribution and the Einstein relationship given in equation 2.25, the equation 2.38 can be rewritten as equation 2.40;

\[ J = q\mu n \frac{\partial \zeta_n}{\partial x} \]  

(2.40)

where, \( \zeta_n \) is the gradient which supplies the driving force for electrons.

Assuming the Fermi level of the material at 0 energy level, the voltage required to break the depletion region is equal to the applied voltage \( V \) which means the \( V \) is the difference between the Fermi levels at the interface. So the concentration of electrons \( n \) at the interface of the semiconductor is not changed on applying the voltage which means \( \zeta_n(0) = 0 \) and the current flow depends on the drift and diffusion in the depletion region. \( E \) is proportional to \( (V_{do} - V)\frac{1}{2} \) and hence according to the diffusion theory the current density \( J \) is given below:

\[ J = qN_c \mu E \exp\left(\frac{-q\phi_b}{k_B T}\right) \left[ \exp\left(\frac{qV}{k_B T}\right) - 1 \right] \]  

(2.41)
This equation can be rewritten as \( J = J_0 \left[ \exp \left( \frac{qV}{k_BT} \right) - 1 \right] \).

According to the thermionic emission theory the assumption made is that the current limiting process is the actual transfer of electrons across the interface between semiconductor and metal. The effects of drift and diffusion in depletion region are assumed to be negligible which means infinite mobility, and \( \frac{\partial n}{\partial x} \) is so small and can be neglected. This means quasi Fermi level for electrons remain flat throughout the depletion region and in bulk semiconductor. The concentration of electrons on the semiconductor side at the interface increases by a factor of \( \exp \left( \frac{qV}{k_BT} \right) \) on applying a voltage \( V \). Imagine that electrons tunnel through the insulating layer with probability \( p \), if \( p < 1 \) then most of the electrons will reflect back to semiconductor and remain in thermal equilibrium with those in bulk. Hence, the electron concentration on the semiconductor side of the boundary is given in equation 2.42 below:

\[
n = N_c \exp \left( \frac{-q(\phi_b - V)}{k_BT} \right) \tag{2.42}
\]

The number of electrons at the insulating layer between metal and semiconductor is distributed by isotropic Maxwellian distribution of velocities due to the kinetic theory. The flux of electrons can be given by \( \frac{n \bar{v}}{4} \), where \( \bar{v} \) is average thermal velocity of electrons in semiconductor. The current density due to electrons passing from the semiconductor into the metal is:

\[
J_{sm} = \frac{pqN_c \bar{v} \exp \left( \frac{-q(\phi_b - V)}{k_BT} \right)}{4} \tag{2.43}
\]

Only a fraction, \( p \), of the electrons can tunnel into the metal from semiconductor and simultaneously there will be a flow of electrons from metal to semiconductor this is not affected by the applied voltage. So the current density:

\[
J_{ms} = \frac{pqN_c \bar{v} \exp \left( \frac{-q\phi_b}{k_BT} \right)}{4} \tag{2.44}
\]

Hence, the net current density is: \( J = J_{sm} - J_{ms} \),

\[
J = \frac{pqN_c \bar{v} \exp \left( \frac{-q\phi_b}{k_BT} \right)}{4} \left[ \exp \left( \frac{qV}{k_BT} \right) - 1 \right] \tag{2.45}
\]

For a Maxwellian distribution of velocities, \( \bar{v} = \left( \frac{8k_BT}{\pi m^*} \right)^{\frac{1}{2}} \) where \( m^* \) is effective mass of electrons in the semiconductor.

If the insulating layer is very thin, then \( p = 1 \) is assumed which means the electrons are not reflected...
back to semiconductor and electrons over the barrier are unidirectional. So the concentration of these electrons at the interface is half and so the thermal velocity is $\frac{v}{2}$ and $N_c = 2\left(\frac{2\pi m^* k_B T}{h}\right)^{\frac{3}{2}}$. Hence the current density, $J$, by substituting the value of $N_c$, $v$ and $p$ in equation 2.45 can be written as,

$$J = A^* T^2 \exp\left(\frac{-q\phi_b}{k_B T}\right) \left[ \exp\left(\frac{qV}{k_B T}\right) - 1 \right]$$

(2.46)

where $A^*$ is the Richardson constant, which is defined as

$$A^* = \frac{4\pi m^* q k^2}{h^3}$$

(2.47)

### 2.7.2 Quantum Mechanical Tunneling

The electrons which have lower energies than the top of the barrier can penetrate the barrier by quantum mechanical tunneling. This emission is expressed in two ways, field emission and thermionic field emission. This depends on the carrier density and temperature of the semiconductor material. At low temperature, in highly doped semiconductor material emission will occur, which is known as the field emission. On increasing the temperature, the electrons will gain some energy to tunnel through the barrier which is known as thermionic field emission (see section 2.7.2.1).

#### 2.7.2.1 Field and Thermionic field emission

The amount of energy required by an electron to tunnel is smaller than the amount of energy required by an electron to cross from the top of the barrier. By using WKB (Wentzel Kramers Brillouin) approximation and depletion approximation tunneling theory is constructed [84]. $E_{00}$ plays an important role in tunneling theory, it has dimensions of energy divided by charge and is given in the equation 2.48 below:

$$E_{00} = \frac{h}{2} \left( \frac{N_d}{m^* \epsilon_s} \right)^{\frac{1}{2}}$$

(2.48)

The emission depends on the doping level for highly doped semiconductor, $>10^{25}$ m$^{-3}$ the emission is field emission and for $<10^{25}$ m$^{-3}$ but $>10^{23}$ m$^{-3}$ the emission is thermionic field emission. The dependance of emission on the temperature can be defined as, if $k_B T << qE_{00}$ it is field emission and if $k_B T >> qE_{00}$ then thermionic emission and if $k_B T \approx qE_{00}$ then thermionic-field emission [85]. $E_{00}$ is the diffusion potential of a Schottky barrier [75], [86]. Therefore $\frac{k_B T}{E_{00}}$ is a measure of thermionic emission and tunneling.
2.7.3 Back to Back Schottky Model

In metal/semiconductor contacts there are two types of contacts—Ohmic and rectifying contacts. In the case of an Ohmic contact a linear J(V) curve is achieved, while in the non-linear and rectifying case, a non-linear and at least partially asymmetric curve is the ultimate signature. The conduction in Schottky devices is influenced by thermionic emission and field effect emission. The field effect emissions is described in section 2.7.2.1 for highly doped samples, where the tunneling probability is increased.

Consider the two Schottky barriers, one at the source and another at drain end of the device. The presence of surface states randomly affects the Schottky barrier formation for both contacts in the case of a nanowire, which might be characterized by different barrier heights. The voltage V is applied in the device through a source contact and the drain contact is grounded. The barrier height is voltage dependent [75]. It has been assumed that the current limiting process is not the electron reaching the interface, but rather the movement across the interface itself. There will be an accumulation of electrons inside the semiconductor at the interface. This will induce an equal and opposite charge inside the metal resulting in additional electric field across the interface, which will act to reduce the barrier height under forward bias [75]. It is customary to define a quantity, $\eta$, known as the ideality factor as [75]:

$$\frac{1}{\eta} = 1 - \left(\frac{d\phi_b}{dV}\right)$$  \hspace{1cm} (2.49)

The equation 2.46 for thermionic field emission theory, for two barriers can be rewritten as [87];

$$J_{1,2} = A^* T^2 \exp \left(\frac{-q\phi_{b,2}}{k_B T}\right) \left[\exp \left(\frac{qV}{\eta k_B T}\right) - 1\right]$$  \hspace{1cm} (2.50)

where $\phi_b$ is the barrier height at zero applied voltage and $\eta=1$ for ideal Schottky barrier in case of thermionic emission theory.

Since our sample is highly doped so the conduction in our device is affected by tunneling as well. So the barrier height is voltage dependent [75], [88], [89] and our device is non-ideal Schottky barrier, $\eta \neq 1$. So the barrier height $\phi_{b_{1,2}}$ can be replaced as given in equation below [88],

$$\phi_{b_1} := \phi_{b_s} - V((1/\eta_1) - 1)$$  \hspace{1cm} (2.51)

$$\phi_{b_2} := \phi_{b_d} + V((1/\eta_2) - 1)$$  \hspace{1cm} (2.52)
where $\phi_{b_1}$ is the effective barrier height at source, $\phi_{b_2}$ is the effective barrier height at drain, they are voltage dependent. These effective barrier heights are influenced by interface states and image-force lowering which clearly perturbs the electric field distribution at the metal and semiconductor interface. Where $\phi_{b_s}$ and $\phi_{b_d}$ are values of barrier in an ideal Schottky junction for source and drain, $^3$ $\phi_{b_s,d} = \phi_m - \chi$ which modified to effective barrier height due to effect of tunneling conduction in our device. The ideality factor $\eta > 1$ for the combination of conduction mechanism due to thermionic emission and tunneling.

Total current density is $J (\pm J_1 = -J_2)$ in a metal-semiconductor-metal device where both interfaces have barriers of different heights. For these devices back to back Schottky model has been developed [88], [89].

$$J = \frac{(J_{01}J_{02} \sinh \left( \frac{qV}{2k_BT} \right))}{(J_{01} \exp \left( \frac{qV}{2k_BT} \right) + (J_{02} \exp \left( -\frac{qV}{2k_BT} \right))}$$ (2.53)

And $J_0$ can be written as,

$$J_{01,02} = AT^2Exp(q\phi_{b_{1,2}})/(k_BT)$$ (2.54)

Where, $m$ is the effective mass, $\frac{m^*}{m_0}$ which is 0.98, Boltzmann constant is 1.38×10$^{-23}$ m$^2$kg s$^{-2}$ K$^{-1}$, $q$ is charge 1.6×10$^{-19}$ C, Planck constant $h$ is 6.623×10$^{-34}$ m$^2$ kg/s, and $A$ is Richardson constant given in equation 2.47, and has the value 1.176×10$^6$ A m$^{-2}$ K$^{-2}$, $\eta$ is ideality factor, $V$ is the applied bias.

Using equation 2.53 as a fitting model provides barrier heights of both interfaces of the nanowire device. The results obtained from actual nanowire devices are presented in chapter 5.

2.8 Hall Effect

Hall effect, discovered in 1879 by Edwin Hall [38], is a widely accepted technique to accurately determine carrier density, type of carrier and mobility of any conducting material. The Hall measurement is carried out with a constant current flowing across the material, let’s say in $X$ direction and the magnetic field is applied lets say in $Z$ direction which means the magnetic lines of force are cutting across the material. Due to this force experienced by a charge carrier they are deflected towards one side of the material let’s say in $Y$ direction. A build-up of charge at the sides of the material will balance this magnetic influence, producing a measurable voltage between the two sides of the material. The presence of this measurable transverse voltage is known as the Hall effect. This measured voltage

$^3$the detailed explanation is given in section 2.6.1
is known as traverse voltage whereas the voltage measured in the direction of current flow is known as longitudinal voltage [38]. A schematic diagram depicting the Hall effect is shown in figure 2.11

![Diagram showing Hall effect](image)

Figure 2.11: Schematic illustration of film on which Hall measurement is performed, external magnetic field applied in Z-direction which is perpendicular to the current $I$ applied in X-direction, due to force experienced by the charge carriers, electrons(-) or holes(+) are collected along the thickness of the film in Y-direction. The variable $w$ is the width, $l$ is the length and $t$ is the thickness of the film.

The force experienced by charge carriers on applying magnetic field is known as Lorentz force, it’s an electromagnetic force on the charge particles,

$$\vec{F} = q\vec{v}_d \times \vec{B} + q\vec{E}$$

(2.55)

The magnetic force is proportional to $q$ and to the magnitude of the vector cross product $\vec{v}_d \times \vec{B}$. If the angle between $\vec{v}_d$ and $\vec{B}$ is $\theta$, then magnitude of the force equals to $qv_dB \sin \theta$.

For maximum Hall effect $\theta$ is $90^\circ$. The direction can be guessed by using the Right hand rule, $FBI$, where force is $F$, magnetic field is $B$ and electric current is $I$. This helps to predict the direction of magnetic force.

For equilibrium state

$$F_m = F_e = \frac{V_H}{w}$$

(2.56)

where, $V_H$ is the measured Hall voltage and $w$ is the width.

$$V_H = \frac{IB}{nqt}$$

(2.57)

where $t$ is thickness. In equilibrium state mentioned above, this electric force is balanced by the magnetic force set up by the Hall voltage, so that there is no net force on the carriers in the $y$ direction. So the electric field can be written as:

$$E_y = v_dB_z$$

(2.58)

The Hall coefficient can be obtained by using equation 2.57 as,
The negative sign indicates that the majority carriers are electrons.

Hall mobility can be defined as:

\[ \mu_H = \frac{R_H}{\rho} \]  

(2.60)

The \( r \) is the scattering factor which can be included in the expression as:

\[ n = -\frac{r}{qR_H} \]  

(2.61)

\( r \) can be defined as \( \frac{\langle r^2 \rangle}{\langle r \rangle^2} \), \( \tau \) is the mean time between carrier collision and \( n \) is electron density in \( \text{m}^{-3} \). For lattice scattering \( r=1.18 \), for impurity scattering \( r=1.93 \) and for neutral scattering \( r=1 \) [90, 91]. This scattering factor \( r \) depends on the magnetic field and temperature and can be determined by measuring the \( R_H \). In this investigation we have extensively used Hall effect measurements to characterize the Si NWs. The detailed results are presented in chapter 6.

2.8.1 High Magnetic Field

The use of high magnetic field, affects the electron trajectories within the channel and for an easier to interpret reduced scattering semi-classical transport, as well as quantum oscillations. High magnetic field causes localization of electrons, which can reduce their motion in the transverse directions, thus making it difficult for them to reach the physical walls of the channel and scatter there. This can ultimately result in quasi-ballistic transport at sufficiently high fields and low-temperature. The use of high magnetic fields reduces the effect of line-edge roughness scattering by diffusive localization, the electron trajectories are confined within the channel length. Considering \( B=14 \text{ T} \) diffusive localization, radius \( r_d \) will result in \( \approx 6.4 \text{ nm} \) which means that the nanowire channel length of size greater than \( \approx 6.4 \text{ nm} \) will have less roughness scattering due to diffusive localization effects. The electrons’ trajectory is confined at the central part of the nanowire and edges and surfaces become less effective, for our measurements, this occurs when magnetic field of 14 T is applied and the nanowire is rotated. Hence, the electrons are confined at the center of the nanowire reducing line-edge roughness scattering, due to which transport can become quasi-ballistic transport.

Diffusive localization radius,
\[ r_d = \frac{24 \text{nm}}{\sqrt{B}} \]  

where B is magnetic field.

2.9 Conclusions

In semiconductors or metals, the electronic transport mechanisms are defined in terms of transport regimes, various characteristic length scales and scattering mechanisms. In this chapter, underlying physics of these transport properties is discussed. Also a brief description on Hall Effect and its measurement, a technique extensively used to measure the transport properties is presented.
Chapter 3

Experimental Methods

In this project, a lot of hardware tools are used for fabrication and characterization, both structural and electrical of the fabricated Si nanowires. This chapter presents the brief description of hardware tools employed in this investigation along with related processing steps and their principle of operation.

3.1 Fabrication Tools

The important experimental tools which will be discussed, in brief, here are UV-Lithography, Electron Beam Lithography and, Reactive Ion Etching-Inductively Coupled Plasma (RIE-ICP) along with the theory of their operation. Also discussed are Ion Etching techniques and Electron Beam Evaporator used extensively in the present investigation.

Lithography was used to draw a pattern on the Silicon On Insulator (SOI) substrate, Electron beam Evaporator is used to deposit the metal layer on these patterns for contact formation, RIE-ICP is used for etching the silicon, Ion Etching is used to remove the silicon dioxide or any contamination. Wire bonding is the technique used to bond the sample with the chip carrier and make contact for the measurement.

3.1.1 UV-Lithography

UV Lithography is a technique of using photons to transfer a geometric pattern from a hard mask onto a light sensitive polymer called photo-resist on the surface of a substrate. The process flow along with cross sectional view for the photo lithographic process is shown in figure 3.1.

In semiconductor device research or manufacturing, the fabrication process always starts with wafer
cleaning in order to minimize the presence of dust particles and contaminants on the wafer surface. With the continuing trend of reduction of device dimensions and layer thickness to nm regime and the role of contaminants and dust particles in adversely affecting the performance and yield of devices, a well optimized cleaning process is used in clean room conditions. We have used ultra-sonication for 3 minutes in acetone, followed by IPA and sonicate for 2 minutes. To dry the substrate high purity nitrogen gas is used followed by pre-baking of the substrates for 5 minutes at 150°C.

A photomask in UV lithography is usually made of fused quartz substrate, coated with an opaque chromium layer. The desired geometric pattern is first written on a photoresist-coated mask by direct writing, followed by the resist development. After that, the patterns are formed on the mask via wet etching method, by immersing the mask into a chrome-etch solution. The undeveloped resist will serve as a hard mask for the etching and the chromium at the regions that are not protected by the resist will be etched. The chemical properties of the photo-resist, notably the solubility of the resist changes significantly upon exposure to light, the photo-resist layer on the wafer will reproduce the mask pattern after being developed in a solvent called the developer.

There are two types of resist namely positive and negative. Positive resist, on exposure to photons the resist breaks its chemical bonds and dissolves when rinsed in developer. Negative resist, on exposure become polymerize and rinse away the unexposed resist from the top of the substrate. Negative resist can provide better resolution compared to positive resist. The pattern transfer is realized on the wafer by etching when using the negative resist as a hard mask. When using the positive resist, a thin film of metal is deposited followed by the lift-off process.

To define the structure on the substrate, first UV light sensitive resist S1813 (positive resist) is spin coated at the speed of 5000 rpm for 45 seconds as shown in figure 3.1 (a), to provide 1.3 μm of thickness. The post bake is carried out for 75 seconds at 115°C to remove the solvent from the resist. The substrate is then exposed to UV light through the mask as shown in figure 3.1 (b). These photosensitive resist are exposed to the I-line of a mercury vapor discharge lamp (365 nm) through a hard-mask using OAI (Optical Associates (OAI) Incorporated Mask Aligner) UV mask aligner. The μm resolution required for the fabrication of the device are well within the capability of this mask aligner. The substrate is exposed under UV light for 6 seconds on contact vacuum mode. The exposure dose is usually between 60 and 100 mJcm². The UV light changes chemical bonds of the resist polymer and the resist becomes soluble in a developer solution of MF319 for 40 seconds and then immediately rinsed in deionized (DI) water resulting in desired pattern on the substrate as shown in figure 3.1 (c). In order to remove the exposed resist from the substrate acetone or 1165 remover has been used.
In our case the mask used in UV lithography to pattern the alignment markers contains 36 identical sites. On each site there are 16 contact pads of 500 $\mu m^2$ and EBL alignment marks of $\sim 10\mu m^2$. Each site is labeled as A1, B1, C1, etc. in the X-direction and A1, A2, A3, etc. in the Y-direction. Figure 3.2, shows a photomask containing pre-designed patterns of contact pads and alignments markers to print the structures on the substrates, A1 sites of the mask is depicted in the figure 3.2 (a).

To fabricate the device, first, pre-patterns (see figure 3.2 (a)) are defined using UV Lithography mask aligner on SOI substrates. Metal is deposited, by electron beam physical vapor deposition (Temescal FC 2000 Metal Evaporation system) at a base pressure of $10^{-6}$ to $10^{-7}$ mbar (see section
3.1.4), on the substrate. To define exposed bond pads and alignment markers. As contact material a double-layer of Ti/Au of thickness 5/40 nm is deposited. The deposition rate of 1 Å/s for Ti and 2 Å/s for Au is used. The 5 nm layer of Ti acts as an adhesive layer for the Au contacts. This substrate is then placed in acetone to remove the remaining unexposed resist and lift off process is used to realize metal pattern. After the lift off process, the pattern comes out as shown in figure 3.2 (b). With the help of 4 alignment markers, in the red square box (see figure 3.2 (b)), the nanowire patterns and contact electrodes are defined using EBL (see figure 3.2 (c)). This central area is of 200 by 200 μm.

3.1.2 Electron-Beam Lithography

EBL is a technique widely used in nanofabrications. One of the first demonstrations of EBL was made by Mollenstedt and Speidel in 1961 [92, 93] over a year after Feynman's lecture on "There is plenty of room at the bottom" [10]. Fifteen years later, the technology had progressed to the point that sub-10 nm lines could be fabricated [94, 95]. Today electron beam direct write is regularly used in research, to fabricate nanoscale features which are difficult to achieve through optical lithographic methods. With optical lithography the production line push to 32 nm era. Other known non-optical lithography techniques are electron-beam projection, ion-beam projection, and soft X-ray extreme ultraviolet which are mix & match with optical lithography. In recent years, the use of EBL has become economically viable for the semiconductor industry [96].

EBL has a similar concept to UV Lithography. However, in EBL the focused beam of electrons are scanned on the electron sensitive resist to draw custom shapes on a surface of the substrate. EBL does not require a hard mask, rather a focused e-beam is scanned across the surface in the pattern desired by the user. Proprietary software (Raith GmbH) is used to draw the pattern and control the electron beam. Beam blanker plates must be installed in the SEM column for EBL operation. This direct the beam away from the sample at very high speeds, controlling the exposure. The dimension of the exposure patterns is limited by electron scattering in both electron beam resists and substrates. EBL systems with high acceleration voltages will reduce the forward scattering angles in the resist and have a wide secondary electron spread in the substrates. The electron scattering process depends on incident electron energy and resist/substrate properties so the resultant energy-intensity distribution in the resist has to be calculated using Monte Carlo simulation. The calculated distribution is of Gaussian shape, and the contribution of secondary-electron exposure is exponentially suppressed with increased incident beam energy. Due to the long penetration depth in the resist, high-energy EBL allows for the exposure of very thick resists, which are useful for forming nanostructures with large height-to-width ratios [97].
Resolution in microscopy is limited to about half of the wavelength of the illumination source. One way to beat the diffraction limit of light is to use an illumination source as electrons because electrons have a shorter wavelength. Louis de Broglie showed that every particle propagates like a wave in 1924 [98]. The wavelength of a particle can be calculated from given equations,

\[ \lambda = \frac{h}{p} \] (3.1)

where \( \lambda \) is the wavelength of a particle, \( h \) is Planck’s constant \((6.626 \times 10^{-34} \text{ J seconds})\), and \( p \) is the momentum of a particle. Since the momentum is the product of the mass and the velocity of a particle, \( p = mv \). Because the velocity of the electrons is determined by the accelerating voltage, or electron potential where;

\[ qV = \frac{1}{2}mv^2 \] (3.2)

The velocity of electrons and the wavelength of propagating electrons at a given accelerating voltage can be calculated from the above equations, 3.1 and 3.2. Since the mass of an electron is \( 9.1 \times 10^{-31} \text{ kg} \) and \( q = 1.6 \times 10^{-19} \text{ C} \), putting the values in above equation, wavelength of electrons is proportional to \( V \) accelerating voltage, \( \lambda = (12.25) \times 10^{-10}/\sqrt{V} \) [99]. Thus, the wavelength of electrons is calculated to be 8.6 pm, when the microscope is operated at 20 kV.

EBL system can generate a high-resolution electron beam with a large electric current for drawing fine patterns on the substrate. EBL system consists of two major components: the main body and the control system. EBL also includes the electron-optical column, high-precision stage and the lithography control system [97], as shown in the figure 3.3.

An EBL system uses hardware similar to a scanning electron microscope (SEM) (see section 3.2.1) to guide a nanometer sized focused beam of electrons to form a pattern on the resist. This exposure is to render the resist by modifying the solubility, either more soluble (called a positive resist) or less soluble (negative resist) in an appropriate developer solution. Resists may be positive or negative similar to UV lithography based resist. Electron exposure to the beam induces two reactions: bond-breaking and polymerization.

Electron-Optical control (EOC) system generates a focused electron beam within the column. There are six main components of the EOC system as indicated in the figure 3.4 out of them three components used for beam generation and focusing i.e.

- Thermal Field Emission Electron Gun,
• Accelerator and

- Electromagnetic Lens.

The electrons are sourced from electron gun by applying an electric field close to the filament tip here in Carl Zeiss Supra 40 SEM combined with Raith Lithography System tool, the type of electron gun is installed is Schottky field emitter.

Accelerator is responsible for high acceleration voltage to accelerates the electron beam into the specimen. The stability of the high-voltage system is important, as any fluctuation in the acceleration voltage directly affects the electron beam energy, changing the focus distance and the deflection angle of the electron beam. This in turn causes defocusing in the drawn patterns. The micro-discharge during the drawing session will also occasionally cut the electron beam, leaving some parts of the pattern undrawn.

There are four electromagnetic lenses which the electron beam passes through as shown in figure
3.4. The beam spot diameter will be reduced to almost one electron when reached to specimen. These lens are composed of coils of wire through which current flows and produces a magnetic field at right angles the fields push the electrons beam inwards into the hole in the center of the aperture. This shape the electron beam and reduce the diameter of the beam as well into a spot. Out of 4 electromagnetic lens top three are condenser lens and bottom one is objective lens.

The other three components which controls the focusing position of the electron beam are:

- beam axis alignment coils,
- blanking electrodes, and
- electrostatic deflector.

Beam axis alignment coils work to align the electron beam throughout the column from electron sources to the electromagnetic lens. There are 4 sets of alignment coils; they are placed immediately
above each of the four electromagnetic lenses. Each alignment coil consists of two coils which generate a horizontal magnetic field in the X-Y plane, deflecting the electron beam slightly by the Lorentz force. Blanking electrodes and electrostatic deflectors, turn off the electron beam between the designed entities. This is done by a beam blanker which deflects the electron beam far away from the center so that the beam will not reach the specimen by applying an electric field perpendicular to the center. However, if the beam is on the surface of the specimen when it is deflected from the axis, an unwanted line is drawn on the specimen. To overcome this issue, the beam blanker consists of two deflectors placed above and below the aperture. The two deflectors generate an electric field of the same strength at the same time and bend the beam by the same amount. As a result, beam is shifted with no lag.

High-precision stage control system controls the high-precision movement of the sample/substrate to be processed. It consists of the X-Y-Z stage for sustaining and moving the sample/substrate, specimen chamber which houses the stage and the specimen changing chamber. Lithography control system sends the lithography control data to the main body. It consists of the hardware including the lithography pattern generator and the Raith software for system operations.

The electron beam scans the surface, in a vector-scanning system, which has better pixel delivery rate due to the shape of the electron beam. The electron beam scan only the area where the pattern has to be drawn as shown in figure 3.5 [101]. In vector scan, the pattern is composed of multiple units referred as a fields and sub fields. The dose is delivered by changing the spot (step size) and dwell time, \(d\) [97, 99, 101]. Hence, the EBL resist is affected by the accelerating voltage, beam current, spot size, type of substrate.

The amount of beam energy required to exposure an electron beam resist can be calculated by given equation,

\[
D_d = \frac{id}{a}
\]

where \(d\), dwell time of the spot \(i\), beam current, which reached to the area, \(a\) defined by a single pixel or beam. This is known as dose \(D_d\), usually expressed in units as \(\mu C/cm^2\).

The important factors to consider when selecting a resist are sensitivity, thermal stability, conductivity, adhesion characteristics, film thickness required for acceptable resolution, the resistance to RIE, and process ability. When all of these factors are understood, proper proximity corrections can be derived. Proximity effect corrections are achieved by changing the dose received by various features in the pattern.

From Monto Carlo simulation electron trajectory can be determined. The effect of the electron beam based on the accelerating voltage on the coated resist and the substrate is shown in the figure.
3.6 (a). The accelerating voltage is 10 kV the scattering effect is high whereas, when the accelerating voltage is 20 kV the scattering effect is lower but it could cause damage to the substrate due to its large penetration depth. The electrons (called secondary electrons) that return to the resist from the substrate possess energies, that are lower than the threshold for breaking the polymers in the resist, and do not make effective exposures. The exposure is mainly contributed by the primary electron, which produces a much narrower exposure width for high accelerating voltage. However, when the electron beam bombards the resist, many of the electrons experience small-angle forward scattering, which tends to broaden the primary beam size. As the electrons penetrate the resist and enter the substrate some of them undergo large-angle scattering events, leading to backscattering, in which these electrons return back to the resist in places far from the spot where the primary beam entered. The forward scattering arises from electron-electron interactions, which deflect the primary electrons by a typically small angle, thus statistically broadening the e-beam in the resist (and further in the
substrate). The majority of the electrons are not terminated in the resist but penetrate the substrate. These electrons can still contribute to the exposure of the resist by scattering back into the resist, causing subsequent inelastic exposure. This backscattering process originates, for example, from a collision with a heavy particle such as a substrate nucleus, leading to wide angle scattering of the electrons as shown in figure 3.6 (b). Penetration depth of the electron is greater for lower atomic number substrate and backscattering emission increase with atomic number. The collisions take place in an area several micrometers from the substrate surface. This causes additional, usually undesirable, exposure in the resist and is known as the electron beam lithography proximity effect [97, 99, 101–103]. As the beam energy increases, the forward scattering is reduced and the back scattering area gets deeper and wider, as shown in figure 3.6 (c). Both forward scattering and backward scattering distributions are of a Gaussian shape. The proximity effect turns out to be the most significant factor limiting the resolution of EBL, it broadens the effective area of exposure in the resist, thus increasing the minimum attainable feature size. This effect not only depends on accelerating voltage but also on the atomic number of the substrate. Higher accelerating voltage and higher the atomic number leads to, higher proximity effect [102].

Mix and match technique continues to gain acceptance as a valuable strategy for reducing capital costs and increasing throughput productivity in semiconductor manufacturing. This is a technique for drawing an EBL pattern overlapping the photo lithographic made pattern already drawn on the substrate. Here, by using UV lithography the alignment markers are made in the beginning of the process flow [97], followed by Au metal deposition as explained earlier (see section 3.1.1). In order to draw a pattern of nanowire, the negative resist HSQ (FOX-15 Flowable oxide, Dow Corning) is used. On use of EBL, electron beam induces polymerization via cross-linking of the polymer chains, thereby reducing its solubility [96]. HSQ can provide better resolution and high resistance to RIE-ICP etching further details explained in section 4.2. The HSQ is mixed with MIBK (Methyl isobutyl ketone also known as 4-Methyl-2-pentanone) at a ratio of 1:9. The resist is spin coated at 5000 rpm onto the pre-patterned substrates to achieve a thickness of about 45 nm as shown in the schematic diagram of figure 3.7 (a). As the alignment markers are covered by an e-beam resist, they should be thick enough to give off a clear secondary electron image. This helps in locating the area to exposure the pattern. The exposure was carried out immediately in order to have the high sensitivity of the resist. To expose the patterns on HSQ resist the electrons beam is accelerated (see figure 3.7 (b)). After EBL process unexposed HSQ resist need to be cleaned away. The combination of the sodium hydroxide and sodium chloride is used as developer. After development, the substrates are rinsed in de-ionized (DI) water, then dried by blowing nitrogen gas (see figure 3.7 (c)). In order to provide thermal, chemical
Penetration depth is small for electron beam for high atomic number (Z) substrate and greater for lower atomic number.

Figure 3.6: Schematic illustration of EBL process. (a) spin coat the resist on SOI wafer and incident the electron beam of two different accelerating voltage 10 kV and 20 kV (b) proximity effect increase if the atomic number is high for the substrate, (c) the effect of backscattering and forward scattering in defining the structure on applying the 10kV accelerating voltage is more compare to the 20kV, the distribution of the scattering is low in case of 20 kV, after [102].

and physical stability to the resist structures, a hard-bake is carried out on a hot plate (see section 4.2.1.1 for post-Baking Process), for SOI substrate [104].
Figure 3.7: Schematic illustration of EBL process. (a) spin coat the HSQ on patterned SOI wafer (b) electron beam bombarded electron on resist to define the structure of single nanowire, (c) develop the SOI wafer and observed the HSQ pattern (HSQ in aqua green, metal in yellow).

3.1.3 RIE-ICP Etching

Reactive Ion Etching is a dry etching plasma based technique developed in eighties particularly for anisotropic etching of dielectrics for Si integrated circuits. Other techniques, such as electron cyclotron resonance (ECR), and inductively coupled plasmas (ICP), are introduced, with mixed success [105] for etching high aspect ratio structures in the nineties.

There are two types of inductively driven sources such as planar and cylindrical geometries. In case of cylindrical geometries coils wrapped around a multipole permanent magnets (see figure 3.8) that will increase the density and the uniformity of the plasma. An RF voltage is applied to the coil, which results in a current flowing and this induces a magnetic field in the reactor. The ions and electrons are mainly generated by the inductive coupling so is possible to control independently the plasma density and the energy of the incoming ions. The wall of the reactor is dielectric which is generally made up of Alumina material. Electrostatic shield is used to eliminate capacitive coupling and this reduces electrical damage to devices.

Oxford Instruments OIPT Plasma Lab System 100 ICP 180 is used for etching the Silicon layer in this investigation. SF$_6$ Sulfur Hexafluoride and CHF$_3$ Fluoromethane are the plasma gases used to etch the Silicon layer in chamber of approximately 50 volumes. These gases break their bond and release the Fluorine to react with silicon device layer and form volatile by-product Silicon Tetrafluoride SiF$_4$. This system can generate ion densities of the order of $10^{11}$ to $10^{13}$ per cm$^{-3}$, neutral species $10^{15}$ per cm$^{-3}$, reactive neutral species $10^{12}$ to $10^{13}$ per cm$^{-3}$ at pressures lower than 2 Pa [102].
At 13.56 MHz electric field generated, which energized free electrons. These free electrons collide to gain further acceleration whereas heavier ions (positive) have less influence by the applied electric field. In low pressure of 2 Pa electrons can cover longer distances than the ions, this results in frequent collisions which can change the plasma to be positively charged. Applying the DC bias to the substrate will maintain the plasma neutrality. The DC voltage is influenced by the process parameters. The DC voltage is created to repel electrons, so therefore higher the electron density and energy, higher the modulus of the DC voltage. A highly negative voltage is required to repel a larger number of electrons, with higher energies. This can be achieved by using high electronegativity gases such as SF₆ and CHF₃. These Fluorine based gases is more prone to absorb free electron and decrease the density of the free electrons in the plasma which would increase the number of negative ions. However, when these gases enter the reactor they are in form of molecules. These molecules are not reactive enough to react chemically with the SOI substrate. The plasma is able to dissociate these molecules into
reactive atoms called radicals. The fluorine which released from these gases will then diffuse to the surface of the Silicon substrate. These fluorine atoms will arrive and recombine, rest will be lost to the walls or go to the pump [102]. The fluorine then chemisorbed by forming a covalent bond with the Silicon into SiF. SiF is not a volatile molecule it will remain on the surface. At room temperature, the first volatile compound formed is SiF$_4$ which is formed on more release of fluorine atoms. Once SiF$_4$ is formed at the surface of the substrate, it can desorb from the surface and become a gas molecule, which is then removed from the reactor through the pump to the exhaust. Ion bombardment can influence the adsorption rate, ions break Si-Si bonds, thus forming active sites, which can more easily filled with fluorine. The adsorption of the fluorine atoms is accelerated by the ion bombardment. The incoming ions will have enough energy to form the covalent bond of the fluorine to the silicon, also to rearrange the silicon and fluorine atoms, so the incoming fluorine can more easily form SiF$_4$. This product molecule remains initially at the surface of the SOI substrate which is also removed from the incoming ions by providing sufficient energy as shown in the figure 3.9. In order to obtain the high quality vertical etching in addition to ion bombardment the use of passivation layer is required at the vertical surface which helps in achieving anisotropic etching. The use of CHF$_3$ gas will help to form a polymer which will protect the side walls during etching process. The disadvantage is that formation of too much polymer will stop the etching and also increase the contamination on the sample [105].

![Figure 3.9: Schematic illustration of the Induced Coupled Plasma-Reactive Ion Etching mechanisms.](image)

The HSQ due to chemical composition get modified as a silicon dioxide under EBL exposure and
followed by thermal curing which act as a mask for ICP-RIE etching, the schematic diagram of process shown is in figure 3.10. It is apparent from the above discussion that there are several parameters which need to be optimized for achieving dimensionally accurate structures like Si NW without any under etching and side wall roughness. Extensive optimization of etching parameters using RIE-ICP is carried out in order to achieve desired Si NWs. The details of optimized process parameters are reported in section 4.2.2.

![Schematic diagram of Induced coupled plasma etching process](image)

**Figure 3.10**: Schematic illustration of Induced coupled plasma etching process. (a) HSQ pattern on SOI wafer to act as mask for etching (b) after etching for 15 s with etch rate of 4 nm/s produce Si single nanowire (HSQ in aqua green, dark green in silicon dioxide, metal in yellow).

### 3.1.4 Electron Beam Evaporator and Ion Etching

E-beam evaporation is a physical vapor deposition (PVD) technique. In this technique an electron beam is created through an electron gun in which a filament is heated by thermionic emission, causing electrons to be emitted in random directions. By using electric and magnetic fields the electrons generated from the filament strike the source material (metal) and vaporize it in vacuum environment. Permanent magnets located underneath the water-cooled copper crucible are responsible for bending the electron beam through 270° as shown in figure 3.11. The electron beam is also controlled in a sweep pattern so that it effectively heats the metal evenly until evaporation occurs. In order to achieve this there are additional electromagnetic coil known as sweep coil to effectively raster the beam around the surface of the metal for evenly heating in the crucible. The metal is heated and its surface atoms will have sufficient energy to leave the surface. These atoms travel to the substrate in the vacuum chamber at thermal energy less than 1 V. Since thermal energy is so low, the pressure in the chamber must be below the point where the mean free path is longer than the distance between
the electron beam source and the substrate. The mean free path is the average distance an atom or molecule can travel in a vacuum chamber before it collides with another particle thereby disturbing its direction to some degree. This is typically around $4.0 \times 10^{-4}$ Pa or lower. After the pressure in the chamber, the rate of evaporation is an important parameter to consider. Evaporation responds rapidly to temperature changes which can be affected by the power of the electron beam subjected to the metal. Crystal monitors can sense the rate of evaporation and provide feedback to control the level of power to the metal which, in turn, regulates deposition and evaporation rates. As film is applied and reaches the desired thickness the electron beam current is decreased and a shutter is placed over the source to inhibit further deposition. We have used Temescal FC 2000 E-Beam Evaporation System which is equipped with programmable features for control of the above processes via individual recipes [106].

![Schematic illustration of electron beam evaporation techniques.](image)

The recipes used in this process of forming contact electrodes with the silicon nanowires are performed in two steps; first one involves Ti followed by Au metal deposition, of thickness 10 nm/60
nm, the rate of evaporation of 1 Å/s for Ti 2 Å/s for Au. In this case, the sample is located at an angle of 70° with respect to the crucible of metal source to deposit the metal at one side of the edges of the Silicon NW as shown in the figure 3.12. In this case, nanowire is acting as a shadow mask for the formation of contact electrode. In the second step the sample is flipped at 180° and the same deposition step is repeated (see section 4.4).

As mentioned earlier, we have employed ICP-RIE process for etching silicon layer to form Si NW. This process is known to leave organic contamination on the surface of the wafer after etching. This can cause severe problem of high contact resistance. In this investigation we found a solution to the problem of poor contacts. An obvious choice to remove the silicon dioxide and contamination is to use well known wet etching process before metal contact formation [107, 108]. We have used Buffered Hydrofluoric Acid (HF) also known as Buffered Oxide Etch (BOE), which is a mixture of a buffering agent, such as ammonium fluoride (NH₄F), and hydrofluoric acid (HF). A common BOE solution comprises of 6:1 volume ratio of 40% NH₄F in water to 49% HF in water. This solution etches thermally grown oxide at approximately 2 nm per second at 25°C. Fluorine reacts with silicon dioxide (SiO₂) to form SiF₄ and O₂. However, there are few problems with the use of wet etching for SOI substrates such as, HF can reacts with the BOX (Buried Oxide) which is silicon dioxide and will end up in floating the silicon device layer in the HF solution as shown in figure 3.13. Also it can
remove the insulating layer on top of silicon device layer as shown in the SEM image of figure 3.14.

Figure 3.13: Schematic illustration of the SOI substrate was dip in the HF solution, the fluorine will react with silicon dioxide on the surface and also on the BOX.

An alternative method is required to remove these contamination and silicon dioxide prior to metal deposition. Therefore, we required a dry etching technique for this process. The ion beam etching is one of the options considered for this purpose. In this investigation, we have used Temescal FC 2000 system which has an ion gun (Veeco 3 cm FC) attached inside the vacuum chamber. So prior to metal deposition the contamination and silicon dioxide at the side walls of the NW are removed before metal deposition in single pump down. This environment will also slow down the re-growth of silicon dioxide resulting in a good quality Ohmic contact. A schematic of the metal deposition system having in-situ ion beam etch facility is shown in figure 3.15.

In this process Veeco 3 cm FC source Ion gun is used. The photo image of Ion gun is shown in figure 3.16. The argon gas is supplied as source gas for ion beam to produce ions and accelerate these ions to high velocities so they are ejected downstream from the source to form a beam. An ion beam source consists of four key elements i.e Discharge Chamber, Electron Source, Grids, and Neutralizer are shown in the figure 3.17.

The source gas is delivered to the discharge chamber, the discharge chamber is also referred as the body. The body will have a magnetic field produced using permanent magnets. The purpose of the magnetic field is to control the motion of electrons leaving the electron source. An electron source is used to ionize the gas and establish a plasma in the chamber. In case of DC sources, the electron source usually a hot filament referred as cathode filament. Electrons leaving the filament will have several ionizing collisions with the argon gas before being collected on the anode. The cathode is
heated using an AC power supply. The cathode filament current is 3.73 A. The discharge voltage is 38 V and current approximately 0.53 A. The beam supply, is also connected to the anode and biases the discharge plasma positive with respect to ground. The beam voltage is 500 V and the total ion current leaving the source is 49 mA. There will be a resistor between body and anode due to which there will be a proper biasing and thereby directs electrons to be collected on the anode surface. Ions created in the discharge chamber are then accelerated to high velocities with the source grids. These grids are electrodes separated from each other by a few millimeters. Each grid has several apertures that are aligned and allow for the extraction of ions. The grid closest to the discharge chamber is referred to as the screen grid (S) and made up of graphite material. Moving downstream, the next grid is referred to the accelerator grid (A) made up of Molybdenum. The S screen grid is biased positive (beam voltage) with respect to ground and consequently the plasma in the discharge chamber is also biased positive with respect to ground. The grid called accelerator is negative biased with respect to the ground. The grid assembly extracts ions from the discharge chamber by applying specific potentials to each grid. An electric field created along the source centerline, hence electrons located in the discharge chamber or downstream from the source are separated due to this established electric field. Positive ions in the discharge chamber that drift close to this electric field are accelerated. The accelerator voltage is 800 V and the accelerator current collected by the grid is around 3 mA. The accelerated
ions then decelerate after passing the A accelerator grid and exit the aperture with a net, ion energy of approximately beam voltage. All these three supply are DC bias. A/B ratio of accelerated to beam currents indicates quality of grid focusing which is <20%. The neutralizer filament is heated with an AC power supply. The purpose of the neutralizer is to emit electrons into the environment downstream from the ion beam source. The emitted electrons provide a charge balance for the ions leaving the source. However, in most situations, electrons from the neutralizer do not directly combine with the ions in the beam to form high energy neutrals. In fact, more electrons are emitted from the neutralizer than ions from the source due to minimize surface charging effect that could occur. The neutralizer can be a plasma bridge neutralizer where a hot filament is placed in a smaller discharge chamber through which an inert process gas is supplied [109]. The filament current is 3.21 A and neutralizer emission current is 62 mA.
3.1.5 Wire Bonding

The wire bonding is an essence of a process in which a thin wire of Al, Au or Cu is locally attached on top of the metal bond pads of the semiconductor device. In order to provide interconnections between device and chip carrier. Amongst the various options, the energy for wire bonding is normally provided either by pure thermal or ultrasonic or combination of the two depending on the application. We have used a thermosonic wedge wire bonder supplied by M/S Kulicke and Soffa Ltd. model 4700 in this investigation. Wire bonding is done in either wedge bonding or ball bonding mode. In our case, Silicon nanowires are wedge bonded due to concern over the electrical current which flow during the ball formation in the ball bonding method which can create an electrostatic discharge in the device. The samples are bonded with gold wire on gold bond pads of size 500 µm. Before wire bonding, the sample and the bonder are kept at the same potential for proper grounding. These precautions are
taken in order to reduce the chance for a nanowire to blow off during the bonding procedure. The force, time and power are the main parameters which determine the bonding process. The tail and loop determine how much wire is left after a bond is made and how high the wedge is retracted after the first bond. Heating of the sample stage, facilitates the adhesion process. The bonding parameters depend on the geometry of the wedge as well as the adhesion of the bond pads. The wire bonding process is optimized and good quality bonds with adequate bond strength is achieved at substrate temperature of 100°C. An important note is that the bonding is heavily affected by contamination of the wedge, the wire must never be touched with hands to avoid carbon contamination, and the wedge should be cleaned often as well. The photograph of the bonding tool used in this investigation is shown in figure 3.18.

![Figure 3.18: Photo image of the wire bonder model 4700.](image)

### 3.2 Microscopy

A human eye can distinguish between two points of 0.2 mm without any lenses, this is distance is called the resolving power of the human eye. A set of lenses can be used to magnify this distance and human eye through the assembly of lenses can see the points closer than 0.2 mm. Light microscope
can magnify up to 1000X but it is limited by the quality of the lenses and wavelength of the light. This results in an achievable resolution that is of the order of half the wavelength of light $\sim 250$ nm. The optical microscope has high power objective lens which has a short focal length, this increase the aperture angle and decrease the depth of field. Electron microscopes are developed due to these fundamental limitations involved with the conventional optical microscopes. As the nanomaterials which are less than 100 nm in dimensions are not possible to observe under optical microscope. Louis de Broglie theorised that electrons have a wave like nature in 1924 [98] which is verified experimentally in 1927 by electron diffraction experiments [110]. Electron microscopes generally operate between 0.5 kV and 300 kV, so at the highest accelerating voltages resolutions up to 0.2 nm can be achieved. The detailed calculation is shown in section 3.1.2. Electron Microscope helps to resolve objects that are very close to one another and it also provides good depth of field which allows the user to see objects as apparent in 3 dimensions.

Multiple advanced microscope systems are used in this work, for both analysis and fabrication. Here in this section the SEM (Scanning electron Microscope), SE-VC (Secondary Electron-Voltage Contrast) Technique, AFM (Atomic force microscope) and TEM (Transmission Electron Microscope) will be discussed briefly.

### 3.2.1 Scanning Electron Microscopy

The first scanning electron microscope (SEM) was developed by Knoll in 1935 [111]. This microscopy tool had issues with the collection and amplification of the signal from the specimen. In 1967, Charles Oatley developed the technology as we know them today [112].

A schematic diagram of a modern SEM is shown in figure 3.19. The basic operation is very similar to that of a conventional light microscope. The working principle is similar to EBL mentioned in previous section 3.1.2.

Electron microscopes may use one of three types of electron source: tungsten(W), lanthanum hexaboride (LaB$_6$), and a field emission gun (FEG). These sources are composed of three components:

- filament or cathode made of tungsten wire, or LaB$_6$ crystal or FEG materials
- a wehnelt cylinder that controls the flow of electrons
- a positively charged anode plate which attracts electrons down the electron column towards the specimen

All SEMs used in this work have FEG source (see figure 3.20). FEG is construct by fabricating a
W needle with a very sharp tip of less than 100 nm, which improves emission and the focusing ability. Hence, extremely high electric fields can be generated at the apex. The high field ($\sim 10^{10} \text{ Vm}^{-1}$) narrows the surface energy barrier to such an extent that electrons may tunnel across it, even at room temperature known as cold field emission (CFE). Unfortunately, due to the sensitivity of the cathode to surface adsorbents, cold FEGs require much higher operational vacuums as well as regular flashes to remove adsorbents. An alternative to the CFE is the Schottky emitter (SE) FEG. A monatomic layer of ZrO is formed on a flattened tungsten tip, lowering the work function from 4.54 eV to 2.8 eV \cite{113} and thereby reducing the barrier to tunnelling operated at 1800 K \cite{113}.

The important characteristics of the electron source are the brightness and size. The brightness of the source is related to the current density and ultimately determines the contrast, resolution and signal to noise ratio of the microscope. FEGs have higher brightness compared to tungsten at the same accelerating voltage. The reason being that the emission current for FEG sources occurs within a very small source size. The beam exits the gun from this source, which is on the order of nanometres compared to a few microns for the other source types. The gun must be kept under ultra-high vacuum ($\ll 10^{-9} \text{ mbar}$) otherwise the filament would burn out. Additionally, the chamber needs to be kept under high vacuum ($\ll 10^{-6} \text{ mbar}$) otherwise the electron beam would be scattered because
of interactions with molecules in the chamber before reaching the specimen. The characteristics of each type of electron source are given in Table 3.1.

<table>
<thead>
<tr>
<th></th>
<th>(SE)FEG</th>
<th>(CFE)FEG</th>
<th>Tungsten</th>
<th>$LaB_6$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Brightness ($A/cm^2$ sr)</td>
<td>$10^8$</td>
<td>$10^9$</td>
<td>$10^7$</td>
<td>$5 \times 10^6$</td>
</tr>
<tr>
<td>Effective Source Size</td>
<td>15 nm</td>
<td>10 nm</td>
<td>15 um</td>
<td>5 um</td>
</tr>
<tr>
<td>Resolution (nm)</td>
<td>1nm</td>
<td>1.2</td>
<td>3</td>
<td>2.5</td>
</tr>
<tr>
<td>Max Probe Current</td>
<td>500-2nA</td>
<td>500-2nA</td>
<td>1uA</td>
<td>750 nA</td>
</tr>
<tr>
<td>Vacuum requirement (mbar)</td>
<td>$10^{-8}$</td>
<td>$10^{-10}$</td>
<td>$10^{-4}$</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>Operating temp. (K)</td>
<td>1800</td>
<td>300</td>
<td>2800</td>
<td>1400-2000</td>
</tr>
<tr>
<td>Service Life</td>
<td>$\gg$ 1.5 yrs.</td>
<td>$\gg$ 1 yr.</td>
<td>100 hrs.</td>
<td>1000 hrs.</td>
</tr>
</tbody>
</table>

Table 3.1: Comparison of electron sources

In this work, a Carl Zeiss Ultra Field Emission SEM with a Gemini column is used, it can provide a high resolution. Accelerating voltages between 100 V and 30 kV. Extensive electron detection system including: Energy Selected Backscattered detector, Angular selected backscatter detector (for atomic number or Bragg scattering contrast) and Secondary Electron detector in lens and out lens.

The working principle is similar to EBL (see section 3.1.2). However, the SEM is used to image
the surface of the sample. For this purpose, the SEM detector used to collect the electrons coming off the sample. There are two types of detector typically used:

- imaging secondary electrons (SE)
- backscattered electrons (BSE)

There are two of secondary electrons detectors one is Everhart-Thornley detector also known as Out-lens and other is annular in-lens detector. Both of these detectors are used to obtain an SE image. The annular in-lens detector located inside the electron column. The other is the out-lens detector [112] located on the wall of the specimen chamber.

In 1994, Carl Zeiss presented a break-through technology for SEM which is the Gemini E-beam column. Column based on this technology have improved the imaging quality compared to conventional SEM. The Gemini field emission column consists of $U_{up}$ which acts as an extractor voltage at first anode, $U_{ex}$ as an accelerator voltage at second anode and $U_{B}$ as a booster voltage (see figure 3.21). The electron beam booster voltage $U_{B}$ is fixed at 8 kV in normal use inside the electron column to accelerate the incident electron [116, 117]. The electrons extracted from SE-FEG and accelerated
by the beam booster voltage, UB. After passing through the scanning system, these boosted electrons are decelerated to the given energy at the pole-piece of objective lens at the end of the electron column. The retarding field not only acts as an electrostatic lens for the incident electron beam but also acts as collector for the SEs to accelerate them into column [118]. Thus, the in-lens detector located in the column above the specimen has an advantage to collect the incoming SEs efficiently. The property of this SE collecting function of the retarding field is a very important factor in image formation. The Gemini column also benefits of in-lens detectors with increased signal-to-noise ratio, improved dynamic range and no aging effect on the detection material. While in-lens detector provides best high resolution information and out-lens SE detector in the specimen chamber provide optimum topographical information. Backscattered electrons are higher energy electrons that are elastically backscattered by the atoms of the sample. Atoms with higher atomic numbers backscatter more efficiently and therefore backscattered detector can give compositional information about the sample.

![Figure 3.22: Schematic illustration of incident beam interacted with a specimen known as interaction volume [119].](image)

The incident electron beam pass through the specimen to a certain distance without any scattering with the specimen atoms. However, when the electron beam collides with the atoms there are several different scattering events that can occur and the interaction volume where all the scattering processes occurs is depicted in figure 3.22. The volume of the interaction depends on the atomic density, topography of the specimen and the acceleration voltage of the incident electron beam. If electrons collide with electrons of the specimen atoms it will the knock electron out of the shell and create
secondary electrons. These secondary electrons have energies generally $\ll 50$ eV. Due to the low energy, only electrons which are close to the surface (2-5 nm) have enough energy to escape and collected to form an image. The secondary electron current is representative of a very small region on the specimen surface and used in high resolution surface imaging. Even a single electron from the beam can produce thousands of secondary electrons to knock them from the shell. This type of collision called inelastic and occurs due to inelastic scattering. When electrons are knock out from specific orbits of an atom in the specimen, X-rays are emitted. With an energy dispersive detector (EDS) these X-rays can be detected to give elemental information about the atom from which they originated due to the energy and wavelength of the X-ray. When few electrons collide with the nucleus of the specimen atoms, it bounces back out of the specimen as a backscattered electron. This is the elastic type of collision. The incident electrons are backscattered with little or no loss in energy and can be scattered to angles between $0^\circ$ to $180^\circ$. These electrons are also high in energy and specimen of high density will create more of these backscattered electron which can provide the information about the specimen density and can form backscattered electron images [114].

3.2.1.1 Imaging and Contrast in Scanning Electron Microscopy

In secondary imaging mode, as the incident beam scans across the sample surface topography, secondary electron are emitted from the sample. If the beam travels into a depression or hole in the sample, the amount of secondary electrons that can escape the sample surface is reduced and the image processing places a corresponding dark spot on the screen. Conversely, if the incident beam scans across a projection or hill on the sample, more secondary electrons can escape the sample surface, and the image processing places a bright spot on the screen. In backscattered imaging mode, as the incident beam scans across the samples surface topography, backscattered electrons are emitted from the sample. A low atomic weight area of the sample will not emit as many backscattered electrons as a high atomic weight area of the sample. In reality, the image is mapping out the density at the surface of the sample. So, the image is bright for the high atomic weight area of the sample and dark for the low atomic weight area of the sample [114].

3.2.2 Secondary Electron-Active Voltage Contrast Technique

Active Voltage Contrast technique is a powerful analytical technique used in isolating problems to a particular circuit or circuit block [120]-[121]. This technique is based on the mechanisms when primary electron beam scans the surface of the sample and generate secondary electrons. The external biasing
is applied to the sample and the secondary electrons are sensitive to the local electrical potentials on the sample. A sample at ground emits more secondary electrons, resulting in a bright contrast. A sample at a positive voltage emits fewer electrons, resulting in a dark contrast [122].

By applying external biasing (from Keithley 2400 source meter) to the sample which is loaded inside the chamber under high vacuum, the image is captured by in-lens detector based on the contrast difference in the image and can determine the flow of charge carriers [123]. The reason to explore this technique is to find out whether the metal electrodes are in contact with the Silicon nanowires or not.

To design the SE-VC set up, a breadboard circuit of size 2.5 cm × 1.0 cm which is half of SEM sample holder shown in figure 3.23 (a). A breadboard circuit is solder with twisted pair cable. This circuit board is soldered with Dual-in-line package and twisted pair which is connected to feed through as shown in the figure 3.23 (b) and (c). The contact pad of 500 µm on the sample are connected to chip carrier through wire bonding see figure 3.23 (d). Chip carrier is placed on the dual in line package which is connected to the twisted pair cables see figure 3.23 (e). The circuit board is set down on the SEM sample holder as shown in figure 3.23 (f).

Figure 3.23: Pictures of the SE-VC Set up (a) SEM sample holder (b) Breadboard circuit solder with twisted pair cable (c) the dual in line package solder on the breadboard circuit with the feed through which is connected to the twisted pair (d) the sample is wire bonded on the chip carrier (e) the sample is connected to dual in line package and (f) mounted on the SEM sample holder.
A photograph of externally biased sample in SEM set-up is shown in figure 3.24. Six contact electrode of Silicon NW is connected to the three twisted pair. One twisted pair is grounded which is connected to the back side of the sample. One electrode is connected to the high voltage (Input/output terminal) of the Keithley all other twisted pair are grounded and connected to the low voltage (Input/output terminal). Back side of the sample is connected to the Keithley to observe any gate leakage and both twisted pair is connected to the high voltage supply while all other electrodes are grounded.

Figure 3.24: A photograph of the SE-VC technique set up combined with SEM.

The background image is taken first by applying zero voltage from the external source. A positive and negative voltage is then applied to the same contact electrode and the change in contrast is observed. This technique helps to identify the issue with the contact electrode. Later with the use of this technique it has been verified that the modified methodology for fabrication of contact electrode was successful. The results are shown in section 4.4.1.
In 1986 Binnig, Quate and Gerber [124] has invented the Atomic force microscopy (AFM). It is an incredibly powerful technique used for visualizing various properties of a surface. It has grown from a simplistic force detection probe to one of the most widely used and versatile microscope systems in modern research. Unlike conventional microscopes which see a surface by focusing a two dimensional projection of a surface onto a screen, the AFM feels the surface with a sharp probe, and in this way builds up a three dimensional map of the underlying features. AFM have some advantages over other microscope such as it has an ultimate limit to the resolving power, the sharpness of its tip, and atomic resolution has been achieved with remarkable results. Also, surface of the sample and outside environment does not affect the measurement as significantly as in scanning tunneling microscopy (STM). An insulating surface can therefore be imaged in ambient atmosphere, just as a conducting sample may be imaged in ultra-high vacuum, or a biological sample. Although most AFM systems cannot operate at the same speeds as an electron microscope, the ability to operate in multiple environments and measure multiple properties of a surface makes AFM an invaluable tool in the field of nanoscience.

AFM operates by scanning a sharp tip on the end of a cantilever across a surface in a raster pattern. The movement of the tip is measured with extremely high accuracy using an optical lever system. A laser is reflected off the back of the cantilever onto a four-quadrant photodiode which measures the change in the position of the tip as it passes over cantilever perpendicular to the surface as shown in figure 3.25. A typical optical lever can resolve movements on the order of picometers in the z-axis. Each pass of the AFM tip takes a 2-D profile of the surface, completing a 3-D image as the raster pattern builds. The ability to take high resolution topographical images is just one of many uses for the AFM. Asylum MFP-3D Infinity AFM has been used in this work which has a vertical resolution of $\ll 1$ nm and scanning range of 80 $\mu$m. There are many modes such as contact, non-contact and tapping mode in which the AFM can operate, each revealing a particular property of the underlying surface imaging. Tapping mode is used in this work is discussed below.

Tapping Mode AFM is developed as a method to achieve high resolution without inducing destructive frictional forces by having the tip touch the surface only for a short time, thus avoiding the issue of lateral forces and drag across the surface. With the Tapping Mode technique, the very soft and fragile samples can be imaged successfully. This potent technique allows high resolution topographic imaging of sample surfaces that are easily damaged, loosely hold to their substrate, or difficult to image by other AFM techniques. Tapping mode overcomes problems associated with friction, adhesion, electro-
static forces, and other difficulties that a plague conventional AFM scanning methods. Tapping mode imaging is implemented in ambient air by oscillating the cantilever assembly at or near the cantilever’s resonant frequency using a piezoelectric crystal. The piezo motion causes the cantilever to oscillate with an amplitude of 1 V when the tip is not in contact with the surface. The oscillating tip is then moved toward the surface until it begins to lightly touch, or tap the surface. During scanning, the vertically oscillating tip alternately contacts the surface and lifts off, generally at a frequency of 0.80 Hz. As the oscillating cantilever begins to intermittently contact the surface, the cantilever oscillation is necessarily reduced due to energy loss caused by the tip contacting the surface. The reduction in oscillation amplitude is used to identify and measure surface features. We have used the tip Tap 300 Al-G (Silicon AFM Probe) of resonant frequency 350 kHz and Force constant 40N/m the tip is used for tapping mode. The two most common materials used for AFM cantilevers is silicon nitride (Si₃N₄) and silicon (Si). When the tip contacts the surface, the high frequency makes the surfaces stiff (viscoelastic), and the tip-sample adhesion forces is greatly reduced. Tapping Mode inherently prevents the tip from sticking to the surface and causing damage during scanning. Another advantage of the Tapping Mode technique is its large, linear operating range. This makes the vertical feedback system highly stable, allowing routine reproducible sample measurements [126]. We have used this technique to measure the thickness of the silicon nanowire before etching and after etching process see section 4.2 in Chapter 4.
3.2.4 Transmission Electron Microscopy

The first transmission electron microscope (TEM) is developed in 1931 by Ruska and Knolls [127]. It is the first electron microscope to be invented. TEM is fundamentally different from SEM in rather than using backscattered and secondary electrons, it relies on transmitted electrons to build up an image. For electrons to be able to pass through a specimen, it must be very thin (≤100 nm thick). Detectors on the opposite side of the specimen collect these electrons which contain information about the specimen. A specimen must often be removed from a supporting substrate to be examined. If the specimen of interest can be suspended in a solvent, it can be drop cast onto a TEM grid or it may have to be prepared by lamella preparation. This involves the use of a focused ion beam (FIB) to cut out a section of a sample and thinning techniques to reduce its thickness down to less than 100 nm (see section 3.2.4.1 for FIB). The resolution of the final image is related to how the electron beam interacts with the sample and how much transmits through to the detector. This can be affected by sample thickness, accelerating voltage, atomic number of the atoms in the sample, crystallinity and sample density. Generally, accelerating voltages used are between 50 keV and 300 keV. Increasing the accelerating voltage can improve the resolution but it also increases the risk of the beam damaging the specimen. Therefore, sample preparation is crucial to ensure an adequate resolution. The ultimate resolution of TEMs is determined by the quality of the electromagnetic lenses and their ability to interact with the beam. Figure 3.26 shows a schematic of the column of a TEM. There are two main operating modes of the TEM: imaging and diffraction.

To create an image, a beam of electrons is generated at the electron gun and is focused into a small, thin, coherent beam by the condenser aperture which excludes high angle electrons. By changing the strength of the intermediate lens and adding or removing the objective aperture it is possible to change between imaging mode and diffraction mode. By inserting the selected area diffraction (SAD) aperture a specific part of an image can be chosen from which to generate a diffraction pattern. This diffraction pattern can be used to examine crystal orientations or crystal defects. The principle advantage of TEM over other electron microscopy techniques is its resolution. By applying classic Rayleigh criteria for a 100 kV accelerating voltage, the wavelength is 4 pm. So theoretically a resolution of 2 pm should be achievable. However, this is not possible due to imperfections in the lenses [129].

3.2.4.1 Focused Ion Beam Milling

FIB is similar to an SEM, except that the beam which is rastered over the sample is an ion beam rather than an electron beam. FIB used for TEM sample preparation. In most commercial systems
gallium ions are used as their sputtering ability allows precise machining of samples. Unlike electron microscopes FIB is inherently destructive to the sample. This is due to momentum possessed by the gallium ions as they strike the surface. The interaction of an ion beam with a surface is more complicated than the equivalent interaction of an electron beam due to the greater momentum involved. There are many different interaction processes that can occur when an impinging Ga ion strikes the surface. When the high-energy ions strike the sample, they sputter atoms from the surface. There will also be implantation of gallium ions of few nanometres on top of the surface. Secondary electrons are also generated by the interaction of the ion beam with the surface which helps in imaging. It used to deposit material when used in conjunction with a gas injection system. The main use of FIB is the controlled removal of substrate material which allows features to be defined on a sub-micron scale. Most modern FIB instruments supplement the FIB column with an additional SEM column so that the instrument becomes a dual beam platform for imaging, material removal, and deposition at length scales of a few nanometres [130].
In this work the FIB used is a dual beam Carl Zeiss Auriga with GIS control for metal deposition. To deposit the Platinum metal, aperture is 30 µm with a 5 kV accelerating voltage. For FIB cutting of NWs, a beam current of 1 nA is used. The FIB is used in order to prepare the sample for TEM characterization. The image taken from this technique is shown in Chapter 4 and 5 (see figure 4.11 and figure 5.6).

3.3 Measurement Technique

The electrical characterization of devices is the primary investigative method used in this thesis. Both AC and DC electrical measurements are performed on single Silicon NWs in chapter 5, while solely AC transport methods are used to study the Hall effect on Silicon NWs in chapter 6. This section shall focus on the equipment and methods used to perform these measurements.

3.3.1 Electrical Measurement

The electrical set-up used for the electrical characterization of silicon nanowire in this work is shown in the figure 3.27. This set-up is designed for room temperature measurement only. It consists of two source-measure units (SMUs) and one multimeter. The system is controlled by Labview software via GPIB connection to a central computer. The nanowire are of high impedance in MΩ range-3MΩ so, source meter Keithley 6430 is used with multimeter 2000 for measuring the voltage drop across the nanowire. Keithley 2400 is used for applying the gate voltage from the back of the sample. Figure 3.27 (a) shows the image of the set-up, images (b) and (c) shows the connection made to the set up and (d) shows the chip carrier connected to the set-up. The sample is wire bonded to chip carrier. Coaxial cables are used to provide the connection between the electrical set-up and Keithleys. The source-drain is connected to the Keithley 6430 and Voltage V1/V2 is connected to the multimeter 2000 and Keithley 2400 to the gate voltage. The grey colored box, as shown in the figure 3.27 is used to provide the electrostatic shielding.

Applying a DC bias across a sample provides a relationship between the voltage and the current response. This response can be Ohmic or non-Ohmic, for Ohmic contacts it follow Ohms law, i.e 
\[ V = IR \], where \( R \) is the total resistance of the circuit or for non-Ohmic it could be Schottky contacts. In case of Ohmic, when Schottky barrier height, is zero or negative between silicon and metal, Then carriers are free to flow in or out of the silicon so that there is a minimal resistance across the contact. In case of non-Ohmic contact when Schottky barrier height is positive, then carriers cannot flow directly to silicon they have to jump through the barrier or tunnel it. The detailed calculation and
Figure 3.27: Photo image of the design Electrical set up. (a) the box is drilled to create holes and put the co-axial connector. We used 5 co-axial connectors, one for Source-Drain and 2 for voltage measurement across the sample, one is gate and other one is ground. (b) 350 MHz cable shielded 4 Twisted Pair is used for connecting gate, voltage V1 and V2, gate and ground (c) shows the other box where source-drain is connected to the twisted pair cable (d) shows the image when the chip carrier is wire bonded to the sample and is attached to the set up for the room temperature measurement.

are given in chapter 5 in section 5.3.

Resistance measurements may be performed in either a 2-probe geometry, or a 4-probe geometry. 2-probe measurements employ a single SMU to drive either current or voltage across a sample, determining the resistance by the ratio of the voltage supplied to the current measured or vice versa. For single nanowire measurement using 2 probe method the contact resistance will also contribute to the resistance for the nanowire measurement as given in the equation 3.4,

\[ R_{2\text{point}} = R_{nw} + R_c \]  \hspace{1cm} (3.4)

where, \( R_{2\text{point}} \) total resistance, \( R_{nw} \) nanowire resistance and \( R_c \) contact resistance.

For accurate measurement, avoiding all unnecessary contact resistance and lead resistance etc., 4-probe measurement are made. The schematically illustrations for the 2-point and 4-point configuration is shown in the figure 3.28. By sourcing current across the outer most contacts, and measuring the corresponding voltage drop across the inner contacts, the contact resistance can be effectively removed in 4-point method.
Power dissipation is limited to 0.1 mW. Power dissipation, $P$ is $I.V$, on 2-point measurement applied to the current/voltage. Calculate the resistance from ohm’s law, use the formula, $I = \sqrt{\frac{P}{R}}$ to find out the upper current limit, for the given sample.

The resistivity $\rho$ of the material may then be calculated as given in the equation 3.5,

$$RA = \rho.l$$  \hspace{1cm} (3.5)

where, cross sectional area of the material, $A$, $A=wt$, $w$ is the width and $t$ is the thickness of the sample and the distance between the inner electrode contact is, $l$.

For nanowire measurements of resistivity, it is appropriate to take the value of $l$ to be the distance from the inner edges of the inner contacts, [131] as shown in figure 3.29.

For the measurement of sheet resistance $R_s$, of thin films, 4-point probe system supplied from Alessi industries is used for the resistivity measurement of the silicon device layer.

$$R_s = \frac{\rho}{t} = 4.532\frac{V}{I}$$  \hspace{1cm} (3.6)

Using the above equation 3.6, the sheet resistance $R_s$ can be measured for the doped thin film [132].
3.3.2 Physical Properties Measurement Systems

Hall measurements on single NW has been performed in Quantum Design Physical Property Measurements System (PPMS) with a superconducting solenoid with maximum applied magnetic field of $\mu_0 H = 14$ T [133]. The PPMS is a highly versatile cryostate with measurement capabilities like Vibrating Sample Magnetometry (VSM), Heat Capacity, Thermal Transport, DC and AC (magneto-) transport with a possible rotation option. In this work, AC Transport with rotation probe is used (see figure 3.30). The sample chamber itself is made of stainless steel in order to reduce thermal loss between the cold bottom and the warm top of the system. Only the bottom-most $\approx 10$ cm of the sample chamber is made of copper, so that the sample is in good thermal equilibrium with the cooling annulus. This system is installed with an electromagnet which is a type of magnet in which the magnetic field is produced by an electric current. The magnetic field disappears when the current is turned off. Electromagnets usually consist of insulated wire wound into a coil. A current through the wire creates a magnetic field which is concentrated in the hole in the center of the coil. The wire turns are often wound around a magnetic core made from a ferromagnetic or ferrimagnetic material such as iron; the magnetic core concentrates the magnetic flux and makes a more powerful magnet. However, instead of using ferromagnetic materials, use superconducting windings cooled with liquid helium, which conduct current without electrical resistance. These allow enormous currents to flow, which generate intense magnetic fields of 14 T. The popular superconductor magnet NbTi alloy embedded in copper is used for cryogenic system. The magnet is used for high field so the the helium level is
required to maintain above 60% if charging the superconducting magnet and it is always immersed in liquid helium. If there is not sufficient helium in the dewar, the top of the magnet can warm and thus make a quench more likely. Furthermore, a quench from high fields in the absence of sufficient cooling by the helium can heat the magnet and cause severe damage to it [133].

![Figure 3.30: Figure (a) and (b) show the photo image of the horizontal rod and the chip carrier on which the sample is connected (c) schematic configuration of the AC circuit for nanowire.](image)

There are two modes for the magnet that is the persistent mode and the driven mode. The persistence switch is a small heater on the magnet wire that drives a section of the magnet non-superconducting. The persistence switch allows the magnet controller to be switched into the magnet circuit so that the magnetic field can be changed. When the heater is turned off, the entire magnet can superconduct, which eliminates the need for a current source during constant field operation. This state is referred to as the persistent mode of the magnet. The magnet can also be operated in driven mode, which retains the current source in the magnet circuit in order to drive the current. Field changes can be made more quickly in driven mode, but the resulting field is much noisier [133]. For 14 T longitudinal magnets, the magnetic field is centered 5.4 cm above the surface of an installed sample puck, but the field uniformity varies.

### 3.3.3 AC Transport Measurement Set-up

A general methodology for measuring the AC Hall effect on low mobility silicon nanowire is presented in this thesis. The AC Hall measurements have been carried out using two approaches: one with ramping the magnetic field within ±14 T with the rate of 133.33 Oe/s and other by rotating the sample in \(xz\) plane from -5° to 365°, keeping the magnetic field constant. This approach minimizes the use of liquid Helium resources, while shortening substantially the acquisition time and therefore improving the susceptibility towards thermal drift without compromising the accuracy of measurement.
For AC transport measurements, a very small current of 20 nA peak-to-peak, with no offsets, is applied to the source and drain electrodes, from an AC/DC current source Keithley 6221, at a 1.23 kHz. As of the low signal-to-noise ratio, a filtering amplifier SR560 is used to condition the voltage pick up. A DSP lock in Amplifier (Stanford Research Systems, SR 830), source digitally triggered, is used to demodulate and low-pass filter the signal from the pre-amplifier, which in-turn is proportional to the voltage drop across the nanowire. These scheme is capable of detecting very small AC signals all the way down to a few nanovolts. Additionally, the phase sensitivity of the lock-in detection allows for the capacitance or offsets, akin to low mobility samples to be filtered out efficiently. The output of the lock in amplifier (LIA) is represented in two in phase X and quadrature Y components [135]. The schematic diagram of the set-up is shown in figure 3.31. The measurement is controlled by the PPMS controller software package for AC Magneto-Transport [136]. This software, supercedes the standard PPMS MultiVu, allowing for extended device control and real time data acquisition.

For the pre-processes and fitting of the transport data, a custom routine written for Mathcad\textsuperscript{TM} has been implemented, allowing for the asymmetric and symmetric with respect to field components of the pick-up to be extracted together with their magnitude, phase, as a function of field magnitude, angular orientation and temperature. For reducing and fitting the pre-processed data for each of the measured samples, a mathcad model [136] is utilized for both measurement approaches i.e. when the magnetic field sweep at \(\pm 14\) T and other approach, when the sample is rotated at constant magnetic field of \(+14\) T. The detailed explanation of the model is given in the Appendix A and B. The measurement results of Hall effect on silicon nanowire are given in chapter 6 in section 6.4.
3.4 Conclusions

To conclude, the working principle of hardware tools and measurement techniques used in this work has been described in details. These techniques play an important role in fabricating the single silicon nanowires and further their characterization and measurement. The following chapter 4, describe the optimization process for negative resist HSQ and formation of contact electrodes.
Chapter 4

Optimization of Silicon Nanowires

4.1 Introduction

To study the transport properties of the NWs, fabricating single Si NW using top down approach is a challenging task as it involves several critical steps such as Electron Beam Lithography (EBL), dry etching and metal contact formation. EBL is a well-known technique for nanostructure patterning. It is a controlled process, can provide better resolution, low throughput and limit the use of photomask [104]. The nanoscale pattern is achieved by negative-tone based electron beam resists such as HSQ. It can improve the attainable feature sizes due to its high resolution and small edge roughness of patterns compared to other negative tone resists [104]. The HSQ resist is patterned down to sub-20 nm width, 40 to 50 nm in thickness and up to 6 μm in length. The Si NW is then realised by an etching-step in RIE-ICP. The NWs are used as a shadow mask to fabricate the contact electrodes to measure transport properties. The performance of the device is normally hampered due to the presence of oxide and contamination during ICP etching [107, 108] at the outer edges of the silicon. Apart from these issues, a major drawback occurs at the junction of metal and semiconductor, known as Schottky barrier. Both of these issues has been overcome by use of Ar$^+$ etching prior to metal deposition without annealing the contacts. The SE-VC characterization is performed on these Si NWs to verify the contact electrodes formation (see section 4.4.1).

In this chapter, we report on the optimization of different processing parameters such as nanoscale patterning of HSQ electron resist using EBL process on SOI substrate. Optimization of ICP-RIE etch process is discussed next using HSQ, which acts as a mask for dry plasma etching. Further, for device fabrication, metal is deposited at the side wall of the NWs utilizing them as a shadow mask. Also
the results of our attempt to use other electron resist such as PMMA (Poly (methyl methacrylate)) is discussed. The main objective of this chapter is to fabricate the NWs. Channel resistance, contact resistance and mobility as a function of the nanowire dimensions have been investigated and are discussed in chapter 5.

4.2 Top-down Approach for Fabricating Silicon Nanowire

SOI wafers provided by Intel are used, with a device layer thickness of 45 nm, having nominal resistivity of 0.006 Ω-cm and a buried oxide of 150 nm. The device layer is \( n \)-type Phosphorous-doped Si and substrate is \( p \)-type Boron-doped Si. The photoresist (positive resist) S1813 is spin coated to pre-patterned alignment markers by using photolithography technique followed by metal deposition of Ti/Au with a thickness of 5/35 nm. The process details are given in section 3.1.1. These mark alignments are used during EBL process to locate the exact desired location on the substrate to draw pattern, which is performed using a Zeiss Supra 40. HSQ (Fox-15 Flowable liquid oxide from Dow Corning) is diluted with the solvent MIBK (4-Methylpentan-2-one) in a ratio of 1:9. This resist solution is spin coated at 5000 rpm for 45 seconds resulting in a thickness of 50 nm, which is measured with AFM. The exposure is carried out immediately in order to get the high sensitivity of the resist [137].

4.2.1 EBL Process for Resist Patterning

In this section, the lithography process has been discussed in details. The overall process for the device fabrication has been shown in the figure 4.1.

![Figure 4.1: Schematic diagram of overall process to fabricate device. The highlighted red box shows lithography process.](image)

From section 3.1.2 we know that there are a few parameters in EBL process which play a major role in defining the resist pattern. The parameters considered for optimization in this work are:
- Step size,
- Accelerating Voltage,
- Type of developers,
- Developing Time,
- Effect of pre and post baking.

We have used two types of electron beam resist in this work i.e. HSQ and PMMA. HSQ is a negative tone inorganic electron beam resist and its chemical structure is based on caged oligomers, which open during curing to form a three-dimensional network structure [138]. It has a small molecular size of average weight $1.1 \times 10^4$ g/mol [139]. Due to its three-dimensional framework, size of aggregates reduces and they do not entangle with one another, hence, do not become large in solution unlike linear polymer [140, 141]. Thus, the proximity effect in HSQ is smaller compared to any positive resist. Therefore, HSQ resist can provide better resolution. It also reduces the roughness of the pattern drawn because the aggregate is of higher density compared to the surroundings. Therefore, these effects strongly influence the resolution of the resist [140]. In addition, the resolution is also influenced by the electron scattering (both in resist and substrate) during EBL. An ideal electron beam resist layer should be very thin in order to minimize the forward scattering of the primary electron beam. The molecular size of resist has almost equal size of definable pattern [142]. The sidewall of EBL patterns are only slightly exposed by the tail of the electron beam profile as well as by the forward and back-scattered electrons [138].

For the use of negative resist HSQ, an adhesion layer of HMDS (hexamethyldisiloxane) is required to be spun first, but HMDS normally leaves lots of residue after developing process, due to this an additional step is required to remove them (see figure 4.2). To avoid the use of HMDS we have pre-heated the substrate at $200^\circ$C before spinning the HSQ [104]. This has been observed to improve the adhesion of the electron resist HSQ as well as provide residue free, clean surface after developing.

In HSQ, line edge roughness depends on number of factors including resist pre-bake temperature, exposure dose and strength of developer. On pre-baking the HSQ prior to electron beam exposure could damage the overall HSQ film and its granularity [143]. Hence, the pre-baking of HSQ film is avoided.

In EBL process, the exposure takes place when number of electrons hit the sample within that area called area dose and line dose, more details are given in section 3.1.2. We have tried both type of doses and kept step size 8 nm for both of them. We have observed that there will be more fluctuation
Figure 4.2: SEM images of the use of HMDS after developing process. These images show that, lots of residue is left on the surface after developing process. There might be a requirement of additional step to remove this residue. The pattern shown in these images are of 100 nm width.

for line dose at the line-edge roughness compared to area dose. See figure 4.3 for line dose and figure 4.4 (a) to (c) for area dose.

Figure 4.3: SEM images of exposed HSQ resist pattern for line, step size is 8 nm. (a) Highest dose is 4000 µC/cm$^2$, the pattern is of 50 nm (b) Lowest dose is 1600 µC/cm$^2$, the pattern is of 36 nm.

Step size also plays a huge role in defining the line-width of the pattern, line-edge roughness increases for large step size and at small step size the roughness reduces but it increases the line-width due to proximity effect. In this work, we have compared two step sizes namely 4 nm and 8 nm. Figure 4.4 (a) and (b) shows the exposure of the resist with the highest dose whereas (c) to (e) are the lowest exposure dose which always plays a significant role in line-edge roughness. On an average the line-edge roughness for 8 nm step size is $>1.5$ nm (see figure 4.4 (a)), similarly for 4 nm step size the line-edge roughness is very low, almost not visible (see figure 4.4 (d)).

The optimization of the exposure dose is carried out by varying the dose in the range of 1600 µC/cm$^2$ to 4000 µC/cm$^2$ as shown in figure 4.5. The best parameters to expose the patterns on HSQ resist were determined to be: acceleration voltage of 20 keV with a 10 µm aperture and the beam
current of 33 pA. The best area dose for 100 nm line width were optimized at 2500 $\mu$C/cm$^2$ with 4 nm step size and dwell time is 36.3 $\mu$s, for beam spot size of under 10 nm.

![Figure 4.4: SEM images of exposed HSQ resist pattern, (a) to (c) are of 8 nm step size. (a) Highest dose, the pattern width is 87 nm. (b) Lowest dose, the pattern width size is 35 nm and (c) underexposed, due to lack of sufficient energy to expose. (d) to (e) HSQ resist pattern are of 4 nm step size. (d) Highest dose is 100 nm (e) Lowest dose is 55 nm.](image)

The minimum line-width of about 23 nm in HSQ resist pattern has been achieved with low roughness on edges as shown in figure 4.6 (a). Similarly, the HSQ pattern of different dimensions ranging from 23 nm to 250 nm are exposed on SOI substrate.

Although HSQ resist is able to provide high resolution, it is very expensive and difficult to work with. So as an alternative we have also tried positive resist PMMA as a negative resist by overexposing the PMMA resist [144]. In table 4.1 we have compared the parameters for PMMA as a positive and as a negative resist. Although we have been successful in achieving the resolution comparable to HSQ (figure 4.6 (b)) the chemical composition of PMMA as a negative resist is observed to be unstable during dry etching. Hence, cannot be used as a mask for dry etching. Also, it has resulted in large line edge roughness and inability to provide good quality nano-scale structures which could be a problem for metal deposition and later for device fabrication process.
Figure 4.5: HSQ line-width as a function of electron beam exposure dose. The range for 100 nm wide pattern drawn with the step size of 4 nm on SOI substrate by using HSQ resist, the values we got from exposed dose is $\frac{35 \text{nm}}{2000 \mu \text{C/cm}^2}$.

Figure 4.6: SEM images (a) HSQ resist pattern (b) PMMA resist pattern as an alternative to HSQ.
To continue the use of HSQ resist pattern as an etch mask, a combination of above mentioned EBL-parameters and a strong developer with low post-baking temperature is favorable for achieving the highest possible resolution and stable etch resistance. In this study, to enhance the contrast of the HSQ pattern, two types of developers are investigated such as:

- Hydroxide based developer 25% wt., TMAH (tetramethylammonium hydroxide)
- Salty developer, 1% wt. NaOH with 4% wt. NaCl with 95% wt. of de-ionized (DI) water

The optimization of developing time for both types of developers is carried out by keeping all other resist parameters the same. After each development, the samples are rinsed in DI water for 150 seconds, and then dried by blowing with Nitrogen gas. The developing time is varied from 90 seconds to 210 seconds, see figure 4.7. It has to be noted that on the use of TMAH developer for 90 seconds, HSQ residue is all over the surface of the substrate, see figure 4.7 (a). On increasing the developing time to 150 seconds for TMAH developer, it does not improve the quality of the process, there is still residue present on the substrate although the pattern edges are more definite (figure 4.7 (b)). However, at this nanorange device fabrication more definite pattern is required. On further developing for longer duration, the surface still has residue left on the surface due to TMAH developer self-limiting nature, see figure 4.7 (c). On comparing TMAH with salty developer, there is residue present at the edges of the exposed patterns, with salty developer used for 90 seconds duration, see figure 4.7 (d). The salty developer is found to show the best performance with minimum edge roughness and enhanced contrast for development time of about 150 seconds (see figure 4.7 (e)) [145, 146]. Whereas, TMAH developer does not show a great modification in the development process for longer times. After developing the resist in salty developer for longer duration, in the range of 180-240 seconds, the edges of the HSQ patterns are observed to be rough and the contrast has been very poor, due to the high reactivity of the salty developer. The HSQ exposed patterns start dissolving in the salty developer for longer durations of development, see figure 4.7 (f). The main risk of using this strong developer is, when
writing nanostructures, thin sections of the patterns may be washed away and only heavily exposed areas may remain on the substrate [139, 147–149], as shown in figure 4.7 (f).

Figure 4.7: SEM images of exposed HSQ resist pattern at step size 4 nm, with comparing developer timing (a)-(c) TMAH and (d)-(f) Salty developer. In (a) and (d) both sample develop at 90 seconds. In (b) and (e) both sample develop at 150 seconds. In (c) and (f) both sample develop 210 seconds. SEM Image of HSQ resist pattern in (e) of sub 23 nm, salty developer shows a uniform edge roughness and enhances the contrast of HSQ. During the development process, the salt has the role of modifying HSQ by breaking network bonds [150]

The HSQ resist has been successfully patterned down to sub-20 nm width, 40 to 50 nm in thickness and up to 6 µm in length. Si NWs with high dimensional accuracy and low sidewall roughness have been realized (see figure 4.7 (e)). It is apparent from comparing the results of the process that a particular combination of parameters, such as a strong developer with low post-baking temperature, is indeed favorable for achieving the highest possible resolution and contrast including stable etch resistance.
Our observed electron resist development behavior could be explained on the basis of proposed model by Joel K. W. Yang et al [151]. It is proposed that during development of the lightly-exposed resist pattern, surface becomes negatively charged due to the presence of ionized Si-O\(^-\) groups belonging to molecules on the resist surface. The positively charged anions are then attracted to the surface to screen the surface charges. The TMA\(^+\) ions are less mobile due to which they are less effective at charge screening. Furthermore, they might cause steric hindrance, thus reducing the access of the resist to OH\(^-\) ions. As a result, the ionized Si-O\(^-\) groups have increased opportunity for cross-linking, which would further slow-down the development. On the other hand, Na\(^+\) ions are smaller, more mobile anions that are effective in screening the negatively charged resist surface, hence allowing the negatively charged OH\(^-\) ions to approach and completely develop the resist pattern. The effect of adding NaCl to the NaOH developer is to therefore increase the concentration of Na\(^+\) ions, and improving the charge screening to further increase the development rate in the low exposed dose pattern. The effects of the Cl\(^-\) ions are currently unclear. This high initial development rate is beneficial for high resolution EBL in thin films because it results in a rapid removal of reaction products of unexposed pattern. Hence, providing a clean surface by washing away of the unexposed HSQ residue on the substrate.

In order to continue the comparison study of the HSQ resist developers, i.e. TMAH and salty developer, two samples are taken and exposed under EBL. While keeping the conditions same, one is developed in 25\%TMAH and another in salty developer. Both these samples are etched together in ICP-RIE etcher. After EBL exposure, the sample is heated at 115\(^\circ\)C for 2 minutes before ICP-RIE etching in order to improve the thermal, chemical and physical stability of the resist structures [145]. This is the post-baking step of the process which is explained in details in section 4.2.1.1. Figure 4.8 shows the improved performance of salty developer as compared to the one developed in TMAH.

In addition to the above, we have observed spikes on the surface of substrate after etching, when TMAH developer is used, as shown in figure 4.8 (a). This is possibly due to the presence of HSQ residue on the surface resulting in non-uniform etching of the substrate. On the other hand, using salty developer a clean substrate surface is observed after etching (see figure 4.8 (b)). This is one more reason to switch to the usage of salty developer. Using hydroxide based developer may cause the formation of an insoluble layer of HSQ on the surface of the substrate [152]. This insoluble layer consists of siloxane based network bands [146, 152]. We conclude that the addition of salt contributes in the development and may result in a modification of the chemical state of HSQ [151, 152]. The salty ions continue to react on the surface of HSQ with the developing time, hence break the network bonds more effectively. On the other hand, TMAH stops this reaction after a certain period of time and
hence, this obstructs the contrast improvement. Whereas, salty developer continues to react with the resist, which provides minimum edge roughness and hence, this improves the HSQ contrast [146, 152].

**Figure 4.8:** SEM images of (a) HSQ resist pattern developed by using 25% of TMAH developer, showing spikes on the surface. This is due to the property of pure hydroxide developer to stop the reaction after certain period of time and hence, HSQ resist is not completely removed from the substrate, whereas, (b) HSQ resist pattern developed by using salty developer after etching, shows a clean surface. Using salty developer thins down the pattern and longer development time cleans the substrate surface.

### 4.2.1.1 Post-Baking Step

An additional step of post-baking is required for more definite pattern to fabricate Si nanowire (see figure 4.9). This has been discussed in this section.

**Figure 4.9:** Schematic diagram of overall process to fabricate device. The highlighted red box shows post-baking process.

To define the silicon nanowire on SOI substrate, the other important process used is dry etching, where HSQ resist pattern acts as a mask. It is crucial for the HSQ resist pattern to be chemically resistant to any subsequent wet and dry etch processes. After development, HSQ can be cured further for improved etch resistance, which is a useful property of HSQ in addition to those mentioned above [150]. Both thermal processing and electron beam exposure lead to a transfer from cage-like resist
structure to network structure. Additional baking affects the HSQ structure more strongly, causing a partial transition of its polymers into a more stable network structure and the formation of network clusters [138]. As the Si-H bonds present in HSQ are more easily dissociated in comparison to stronger Si-O network bonds in SiO$_2$, and the porosity of the cage like structure in non-hard-baked HSQ makes it easier for fluorine ions to tetrahedrally surround Si atoms on the resist surface and to form volatile SiF$_4$. In fact, baking can be considered as a kind of post-exposure of the whole HSQ resist pattern by which the sensitivity is enhanced but the contrast is reduced [145]. The effect of baking is shown in the figure 4.10, which clearly illustrates that the post baked HSQ resist pattern has a good stability and etch resistance during dry etching.

During lithography process cage like oligomers HSQ ($H_8Si_8O_{12}$) are converted into unstable silanols Si-OH, these are crosslinked into network polymer like Si-O-Si bonds. Thus, EBL converts HSQ into SiO$_2$ [150]. This chemical behavior is supported by the IR spectra studies carried out by Namatsu et al [137]. The observed peaks in IR spectra at 1130 cm$^{-1}$ and 1080 cm$^{-1}$ represent the asymmetric stretching of Si-O bonds in silsesquioxane molecules and largely cyclic Si-O bonds, respectively [137]. The existence of both the strong peak at 1130 cm$^{-1}$ and the weak peak at 1080 cm$^{-1}$ indicates that this material is an incompletely closed and crosslinked cage structure. After the e-beam exposure the intensities of the Si-H peaks and Si-O peak at 1130 cm$^{-1}$ decreases, whereas the intensity of the Si-O peak at 1080 cm$^{-1}$ increases. This indicates that the crosslinking proceeds via Si-H bond-scission. The unexposed HSQ easily dissolved in alkaline solution in bubble formation on the surface of the substrate. However, when the crosslinking is slightly produced by the e-beam, the
dissolution rate of HSQ decreases remarkably because the bonds become more stable as a result of the highly three-dimensional network formation resulting from the crosslinking [139, 141].

Similar conclusion has been made by Yang et al [150] using FTIR (Fourier- Transform Infrared Spectroscopy) and XPS (X-ray Photoelectron Spectroscopy) studies. At high doses of electron beam lithography, the FTIR spectra became similar to that of amorphous structure of SiO₂. In our case we performed TEM analysis to investigate the presence of SiO₂ on top of Si NW, formed due to curing of the HSQ resist, as shown in figure 4.11. The presence of this insulating layer on top of Si NW avoided the shorting of Hall contact electrodes from the top of the NWs [3].

![Magnified TEM image from cross-sectional view showed the insulating layer of 2-3 nm on top of the silicon nanowire. This is the silicon dioxide which has been formed by curing the HSQ.](image)

4.2.2 ICP-RIE Process for Silicon Nanowire

As discussed earlier in section 3.1.3, it is clear that there are several etch parameters which play a major role in defining the NWs of desired shape and size with smooth side wall surface during dry etch process. Here in this section (see figure 4.12) we discuss the results of our optimization process of ICP etching carried out to achieve desired Si NW structures.

![Schematic diagram of overall process to fabricate device. The highlighted red box shows etching process.](image)
Few parameters considered for optimization are:

- Gas flow ratio,
- Passivation Gases,
- Chamber Pressure and temperature,
- RF power,
- Etch rate and Selectivity.

Silicon can be etched with any Halogen containing gas such as CF$_4$, SF$_6$, SiCl$_4$ and BCl$_3$. These gases are chemically reactive and produce enormous amount of radicals which are the primary source of etching and often mixed with a passivation gas to improve the etch profile. Fluorine (F) based gases result in isotropic etching, whereas chlorine (Cl) based are known to etch anisotropically. Etching process seems to be dominated by ions. Therefore, the etch rate and selectivity is higher with Flourine compared to Chlorine based gases [4]. Most of our results are based on Fluorine chemistry only, this is due to the availability of Fluorine based etch system in our facility.

To etch the nanoscale devices, very smooth and vertical side walls are required with good etch rate and selectivity. For this, we have employed the continuous mixed mode of CHF$_3$/SF$_6$ etch chemistry. For silicon etching SF$_6$ is used and for passivation CHF$_3$ is used [153, 154]. This continuous mixed mode of gases is preferred because it can avoid scallops and achieve highly vertical nanowires with smooth side walls. Also mixed mode allows etch and passivation at the same time. F radicals from SF$_6$ react at the silicon surface and form volatile SF$_{x+}$ species to initiate the etching. Meanwhile CHF$_3$ is used for passivation, and deposits a very thin layer of fluorocarbon polymer (CHF$_y$)$_n$, similar to Teflon, onto the substrate which is being etched horizontally by the directional bombardment of energetic ions (SF$_{x+}$). Whereas, side walls remain protected from being etched further [155] (see section 3.1.3).

In ICP RIE process, the ICP source provides high density plasma and RIE source provides DC bias. A DC electric field is required to keep the plasma neutral by repelling electrons from the walls by applying the bias of 88 V. This DC bias also provides anisotropic etching by applying negative supply to substrate so that ions (positive) can attract to the substrate directionally. High etch rates are achieved by high ion density, high radical density and high conductance pumping port which provides high gas throughput for fastest etch rates. Wafer clamping and Helium cooling with the flow rate of around 5.7 sccm, is found to provide excellent temperature control. To etch a silicon layer, the
substrate is loaded in the chamber where CHF$_3$/SF$_6$ gas flow is maintained at particular flow rates with the substrate holder at 100°C with 1.3×10$^2$ Pa He backside pressure. Using optimized ICP/RIE power, the etching process is carried out at desired etch rate and time. Normally 20% over-etching is done in dry etching to ensure complete etching of the silicon layer to avoid any left over.

In this work, we optimized the etch process by stabilizing the etch and passivation gases flow ratio, RIE power, ICP power and chamber pressure with approach to achieve moderate etch rate and selectivity with minimum possible platen power to minimize plasma induced damages. The SF$_6$ gas flow rate is maintained at 15 sccm and CHF$_3$ varied from 100 sccm to 80 sccm, see table 4.2, in a chamber of approximately 50 volumes. The chamber pressure controls the amount of gas for ionization and the mean free path of the particles decreases with increasing chamber pressure, which results in more electron-ion interactions, hence reducing the plasma density. In other terms the concentration of F radicals decreases as chamber pressure increases and results in low etch rate, see table 4.3.

The RIE power is optimized to minimize the plasma-induced sidewall damages. The DC bias voltage builds up as a result of applied platen power which controls the directionality of the ion bombardment perpendicular to the etching surface, this results in anisotropic etching. Ion bombardment helps to remove the passivation from the etching surface while retaining the passivation onto the sidewalls. The DC bias voltage is calculated as an average over the total etch duration. A higher bias voltage causes intense ion sputtering onto the etching substrate which enhances the efficiency of bond breaking and formation of etch products, thus increases the overall etch rate. Typically, higher bias voltage results in significant percentage of plasma induced sidewall damages, so the etch processes are optimized with a view to keep the bias voltage as low as possible.

Depending upon the process, high density plasma generated in the chamber allows to achieve high etch rates but requires higher RF power which increases the bias voltage and hence accelerates the high energy ions from the plasma towards the substrate to etch. However, it may introduce trap states on the surface of substrate which is the major cause of plasma induced sidewall damages, termed as sidewall depletion in nanowires, which increases the contact resistance by limiting the performance of the devices. These damages increase with higher RF power. The use of ICP-RIE allows the generation of high density plasma at low bias voltages. The term "damage" refers to any effect of the etch process, this could lead to damages such as disruption of the lattice structure, creation of dangling bonds on the interface, contamination of etched surface with polymer passivation layer and heavy metals, which result in deep traps for charge carriers and hence, deteriorates the electrical characteristics of the nanowires. These damages can be reduced by optimizing the process parameters to etch the substrate with low bias voltages, the averaged DC bias voltage of the process is 88 V. For low damage etching,
the platen power is lowered to 30 W, this ensures high quality pattern transfer which reduced the etch rate to 4 nm/sec. For more details on their working principle, see section 3.1.3.

<table>
<thead>
<tr>
<th>CHF$_3$(sccm)</th>
<th>SF$_6$ (sccm)</th>
<th>DC bias (-V)</th>
<th>RIE power (W)</th>
<th>ICP Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>15</td>
<td>88</td>
<td>30</td>
<td>1200</td>
</tr>
<tr>
<td>80</td>
<td>15</td>
<td>88</td>
<td>30</td>
<td>1200</td>
</tr>
</tbody>
</table>

Table 4.2: A comparison of the etch processes optimized for Si nanowire etching

<table>
<thead>
<tr>
<th>Chamber Pressure(Pa)</th>
<th>Etch rate (nm/sec)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>3</td>
<td>Isotropic etching with positive tapered profile</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>Stable Anisotropic etched</td>
</tr>
</tbody>
</table>

Table 4.3: A comparison of the etch rate optimized for Si nanowire

The SEM image in figure 4.13 shows that the profile is tapered positive, indicating the polymer level is high resulting in undercut profile. This outcome has suggested to reduce CHF$_3$ to 80 sccm without changing other parameter. Hence, the resultant etch profile is anisotropic and vertical with smooth side wall, see figure 4.14.

![SEM image of resist pattern showing isotropic etching profile of recipe used.](image)

It is observed that the sidewall profile changed dramatically from undercut to slightly tapered (positive) to vertical smooth profile with decrease in the flow of SF$_6$ and CHF$_3$. The selectivity is defined as the ratio of the Si etched over the remaining HSQ resist. Reducing the flow of CHF$_3$ from 100 sccm to 80 sccm results in optimum balance between etching and passivation gas flow ratio. The
passivation on the bottom of the nanowire is more preferentially removed as compared to sidewalls, forcing Si nanowire to etch anisotropically, see figure 4.14 and AFM image in figure 4.15. The tip radius used in AFM measurement is 10 nm.

Figure 4.15: AFM measurement of Si NW showing anisotropic etching profile. In a graph, the profile of thickness vs width is showing for one point and the other graph is showing the same profile for 4 more points on the Si NW. (a) Structure of the Si NW along the thickness, and the rough surface shows the presence of SiO$_2$ layer on top. (b) the thickness of Si NWs is uniformly shaped along the length of NW of 6 $\mu$m.
The SOI substrate used in this study consists of silicon device layer of thickness 45 nm and 150 nm buried oxide layer underneath. The exposed HSQ in EBL process results in the thickness of 30 nm measured with AFM. The RIE-ICP etch for 15 seconds with the etching rate of 4nm/sec results in total etch of 60 nm which is confirmed by the measurement as shown in figure 4.16 (a). The silicon surface has some non-uniformity after dry etching as can be seen from the 3D view of AFM image of Si NW in figure 4.16 (b). From these, AFM thickness measurement can conclude that the thickness of the exposed HSQ converted into SiO₂, on average is 12 nm. This is confirmed by cross-sectional SEM images as shown in figure 4.17. The ICP etching process has etched the Silicon completely from the surface, as shown in figure 4.17 (a) and (b).

![Silicon Dioxide](image)

**Figure 4.16:** (a) Schematic illustration shows the thickness of Si NW is 45 nm and average thickness of silicon dioxide is 12 nm (b) 3D images of Si nanowire and silicon dioxide show the total thickness of 60 nm.

![SEM images](image)

**Figure 4.17:** SEM images of cross-sectional view of the SOI wafer (a) before etching (b) after etching and successfully etched approximately 60 nm thickness of Silicon.

Roughness of the pattern is due to unequal dose distributions which make the cross-linking in
the pattern inhomogeneous. The observed roughness of HSQ pattern after development could be responsible for this non-uniformity (see SEM image in figure 4.18). This could be solved by Oxygen plasma treatment and HF etching. For Oxygen plasma treatment Oxygen atoms in the plasma diffuse into siloxane film such as HSQ and can oxidize the whole film [139]. However, in our case we have not used Oxygen plasma treatment because it would oxidize the side wall of the nanowire where metal deposition is required for Ohmic contact. Also etching of the sample in HF solution is not possible without putting the BOX (Silicon dioxide) etching at risk. The thin insulating layer on top of silicon nanowire and even silicon nanowire itself can be damaged as well (see section 3.1.4) during any further chemical treatment. Also, since our focus is to fabricate the contact electrode at the side wall of the Si NW we have not paid much attention to the surface roughness of the Si NW and continued the process of fabrication.

Figure 4.18: SEM image of HSQ after ICP-RIE etching shows the rough surface on the top of the Si NW. This is the exposed HSQ which is thermally cured into Silicon dioxide.

Based on the above optimization carried out for different dry etch parameters, the optimized etch parameters used in this investigation to achieve the etching of 45 nm device layer are given in the following table 4.4.
Table 4.4: Parameters optimized to etch Si layer

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICP source Forward Power</td>
<td>1200 W</td>
</tr>
<tr>
<td>RIE power</td>
<td>30 W</td>
</tr>
<tr>
<td>Reflected Power</td>
<td>22 W</td>
</tr>
<tr>
<td>CHF₃ Flow rate</td>
<td>80 sccm</td>
</tr>
<tr>
<td>SF₆ flow rate</td>
<td>15 sccm</td>
</tr>
<tr>
<td>Chamber pressure</td>
<td>2 Pa</td>
</tr>
<tr>
<td>Substrate Temperature</td>
<td>10⁹°C</td>
</tr>
<tr>
<td>Etch rate</td>
<td>4 nm/sec</td>
</tr>
<tr>
<td>Selectivity</td>
<td>0.23</td>
</tr>
<tr>
<td>Helium Flow</td>
<td>5-7 sccm</td>
</tr>
</tbody>
</table>

4.3 Top Contacts on Silicon Nanowire

After optimizing the fabrication process for the silicon nanowires, the contact electrodes are defined for electrical measurement (see figure 4.19).

![Figure 4.19: Schematic diagram of overall process to fabricate device. The highlighted red box shows fabrication of contact electrode process.](image)

To fabricate contact electrodes, the electron resist PMMA is used. Standard PMMA-parameters for spin coating, pre and post-baking are discussed in section 4.2.1. Carl Zeiss Supra 40 SEM combined with Raith Lithography System tool is used for exposure. To expose PMMA a beam current of 25 pA, area dose of 300 µC/cm² is used with an acceleration voltage of 15 keV (table 4.1). The samples are developed in MIBK: IPA (1:3) for 40 s (see section 3.1.2). This is followed by deposition of Ti/Au with a thickness of 5/65 nm (see section 3.1.4) as shown in the SEM image in figure 4.20 (a). SEM image taken after the measurement of the nanowire and contact electrode is shown in figure 4.20 (b). Au contacts at the top of Silicon nanowire have been burned out because they were poorly adhered to Si NW top surface, with the slight heating of the electrode during biasing, they broke. This failure may also get accelerated due to the presence of oxide layer on top and edges of the nanowire. The measured 2-point I-V characteristics of these nanowire result in a back to back Schottky barrier [156]
at 300 K, see figure 4.20 (c). It shows a non-Ohmic behavior with low level of current (nA) which clearly suggests poor quality of contact to Si nanowires mainly due to metal not being in direct contact with Si nanowires or there being an oxide layer between metal and semiconductor.

The current is limited by the poor contact, the value of the resistance is 2 MΩ and the value of resistivity is 0.15 Ω-cm.

The observed high contact resistance could be mainly due to contamination at the metal/semiconductor interface and damaged semiconductor surface after dry etching. The contamination can occur during RIE-ICP etching. The reaction occurring during the silicon etching process can cause damage due to ion bombardment, radiation induced bonding changes and charge build up [107]. If these damages
are not removed, they can also create traps in insulators and gap states in semiconductors [107, 108]. It will also lead to contamination which increases the contact resistance [107]. The contamination can have two forms: residue layers and permeation. The residue layers are ultrathin films of reaction products that can coat surfaces, whereas the permeation is the implantation, or diffusion, of impurities. These impurities are from a range of metals, whose source is the process chamber. If these damage are not removed, then residues can interfere with subsequent processing such as oxidation and presence of hydrogen can cause increase in contact resistance [107, 157]. Impurities, if not removed, can have a range of detrimental consequences such as modified carrier lifetimes [108]. Hydrogen, in particular, can affect materials in a number of ways including modifying doping activation [108, 157]. This can affect both n and p types Silicon. Recent work suggests that Hydrogen is amphoteric in Silicon and can move as a positively charged species in p-type Si and as a negatively charged species in n-type Si [158]. X. C. Mu et al [108] investigated spreading resistance profiling (SRP) and found that the permeation of hydrogen caused by dry etching can result in doping deactivation in silicon and, hence, this will change carrier concentration. Fortunately, doping deactivation can be removed by annealing [108, 158]. However due to dry etching the Hydrogen, present in materials, can collect at SiO$_2$/Si interfaces and at metal/silicon interfaces [157].

There are few post etching cleaning methods, which are proven to be helpful in removing this contamination. Under wet process one can use HF (Hydrogen fluoride) dip, 1:1 H$_2$SO$_4$/H$_2$O$_2$ (Sulfuric acid/Hydrogen peroxide) acid, also known as piranha solution, and combination of both Piranha solution and HF dip. Even after removing the contamination caused during ICP etching the contact resistance is still high. Under dry process Oxygen plasma treatment is also one of the methods which is found to be not suitable for our application [107, 108]. In this work, we have tried the wet etching but it damaged our substrate. Further, wet etching is not a controlled process as mentioned earlier in section 3.1.4.

The presently known conventional methods to remove these contamination and native grown Silicon oxide on Silicon are not helpful to improve the contacts between metal and silicon. John Degrave et al [3] have presented a new methodology to make an intimate contact between metal and silicon nanowire. Lift off process in combination with angled evaporation have been used for intimate contact formation. We have used a similar approach for contact electrode fabrication, see the section 4.4 below.
4.4 Nanowire Used as a Shadow Mask

Using the angled evaporation technique [3] contact electrodes have been fabricated. For this fabrication step, used PMMA electron resist for metal lift off. After electron beam exposure and resist developing, Ti/Au-10/60 nm have been evaporated using electron beam evaporation keeping the plane of the substrate at an angle of 70° with respect to the e-beam emission source prior to this Ar+ ions have been used to remove the contamination (see figure 4.21 (a)). The substrate is flipped by 180° for the second evaporation after EBL process and repeated the same steps for opposite side of electrodes (see figure 4.21 (b)). In this case the nanowire structures have been used as a shadow mask simultaneously depositing the metal on the opposite side walls of the nanowires [3] due to the use of this process there will be an offset at transverse contacts (see figure 4.21 (c)). The detailed process is given in section 3.1.4. The metal is supposed to form an intimate contact with Si NWs’ sidewall as shown in figure
4.21 (d) and the presence of SiO$_2$ on top of Si NWs to prevent the Hall electrode from shorting is shown in figure 4.21 (e). Completely fabricated contact electrode geometry structures are shown in figure 4.21 (f).

The SEM images of the successfully fabricated silicon nanowire device, 30 nm in width, is shown in figure 4.22 and for 200 nm in width is shown in figure 4.23, for better understanding of sidewall contact formation image is taken at an angle. Imaging under SEM also affects the resistance of the nanowire. The prolonged electron irradiation can reduce the initial value of resistance by creating traps [2]. This contamination occurs mainly by hydrocarbons during extensive imaging on Si NW device. In order to avoid the deposition of contamination during SEM imaging, they should be taken after measurement.

Figure 4.22: Top view biased SEM image of 30 nm Silicon nanowire with 5 electrodes. The arrow indicates $<100>$ direction of Si crystal.
Figure 4.23: SEM image of Silicon NW of width 200 nm taken at an angle showing the side wall contact formation.

From the SEM images, we concluded that the angled metal deposition methodology is successful. However, there is no information about the electrical contact formation, between metal contact electrode and Si NWs. In order to investigate this further Secondary Electrons-Voltage Contrast technique is used (for detailed methodology see section 4.4.1).

4.4.1 Secondary Electrons-Active Voltage Contrast Characterization

Secondary Electrons-Active Voltage Contrast Characterization technique is performed on the fabricated device to inspect the contact formation with Si NW on Hall device. The detailed methodology of this characterization technique is given in section 3.2.2. The image of the Hall test structure captured through SEM is shown in figures 4.24 (a) and 4.26 (a). We first applied 0 V external bias followed by different polarities. It can be seen that with a positive or negative external bias applied to the contact electrode, it appears darker or brighter compared to the other electrodes. To further, enhance the contrast effect, a custom routine written for Mathcad\textsuperscript{TM} has been used, the SEM images have resolution of 1024×768 pixels. Each pixel is represented by a number which is directly proportional to the number of SEs collected at that point. The background image, which has been taken at 0 V externally applied bias, is subtracted from all the following images obtained when particular electrodes are biased positive/negative. Due to the large and non-uniform charges’ distribution created by the biased electrodes, the collected images have to be corrected for lateral offset and quadratic warping during the SEM imaging, these images need to be corrected for further analysis. This is done by
selecting a set of four matching reference-points on both the background image and the image that needs to be dewarped. This corresponds to a set of eight algebra equations for six independent (three for each axis) and if necessary, up to two mixed axis coefficients. The system is solved by least squares error minimization to yield the set of parameters for optimal dewarping. Hence, after this process the resulting overlaid image has a much enhanced contrast relative to the difference charge drainage and non-morphological features.

All electrodes of the device are analyzed together, the contact electrodes labeled as 2A, 2B, 4A, 4B and 4C, see SEM image in figure 4.24 (a). Using this technique, investigate if there is any damage at the buried oxide (BOX) and failure of the formation of sidewall contact electrode at the Si NW. The electrode labeled as 2B has a fault which has been confirmed on applying the positive external bias of 2 V. The contrast of the electrode appears dark, the Si NW is also changing the contrast with the electrode and the part of the contact electrode which is not connected to the Si NW also changes the contrast (see figure 4.24 (b)). This could be due to the defects in the device. Similarly, on applying the external bias of -2 V both the contact electrodes and Si NW brighten up confirming the location of defects in the device (see figure 4.24 (c)). The images in figures 4.24 (d) & (e) are Fourier filtered versions of figure 4.24 (b) & (c). Using these images, a quantification of the voltage contrast has been done. The other electrode, 4C, is not in galvanic contact with the Si NW, as on varying the external bias between positive and negative only the electrode changes its contrast from dark to bright and rest of the devices have the same contrast (see figures 4.24 (f) & (g)). This has shown that the methodology for the fabrication of sidewall contact needs to be improved. Figure 4.24 (h) & (i) illustrates the contrast when positive/negative external bias is applied, while the substrate at the back of the sample is connected to the ground. The Si NW and contact electrode contrast is dark compared to the buried oxide (BOX) contrast in figure 4.24 (h), Si NW and contact electrode contrast is bright compared to BOX contrast in figure 4.24 (i), which confirmed that the current is not passing through the BOX and thus, there is no major gate leakage issue. The Si NW used in this characterization is of 100 nm in width.
Figure 4.24: (a) SEM image of Hall device with a Si NW width of 100 nm, with biased electrodes labeled as 2A, 2B, 4A, 4B and 4C. SEM image post-processed in a Mathcad script. (b) Applied +2 V external bias to electrode labeled as 2B (highlighted with yellow square box) which appears dark. (c) Applied external bias of 2 V to the same contact electrode (highlighted with yellow square box) appears bright. (d) and (e) Fourier filtering processed images of (b) and (c). SEM image post-processed in a Mathcad script (f) an external bias of +1 V given to the contact electrode labeled as 4C (highlighted with yellow square box) appears dark; (g) an external bias of 1 V given to the same contact electrode (highlighted with yellow square box) appears bright; (h) an applied external bias of +2 V to the substrate; and (i) an applied external bias of 2 V to the substrate connected to the ground.

A quantification has been performed, using box-averaging of the individual contact electrode areas; see figure 4.25. With respect to errors, which are derived from the standard deviation of the box-selected areas, this graph represents decrement (increment) in intensity of $\approx 0.27(4)$ per volt relative to background, for positive (negative) bias. The unbiased number of electrons ejected from the electrode
area is ≈ 2.5 times that of the background (featureless area of oxide, away from the electrodes) at 0 V external bias.

Figure 4.25: Quantification of images shown in figure 4.24 (a) and (b) in terms of normalized intensity as a function of applied external bias. A decrement of intensity of ≈ 0.27(4) per volt relative to the background (featureless area away from the electrodes) is observed. The electrons emanating from the electrode area are generally ≈ 2.5 times more numerous than the background (oxide-covered areas away from the electrodes) at 0V [159].

The lowest range of Si NW which is analyzed is 70 nm in width, SEM image is shown in figure 4.26 (a). This technique can be easily accessible upto few nanometer scale devices. In Si NW device of 70 nm width, contact electrode labeled as 4A and 4C which is in contact with the Si NW appears darker on applying positive external bias and brighter on applying negative external bias (figure 4.26 (b) & (c)) indicating proper electrical contact behavior of device. The images extracted using SE-VC technique unveil that the set-up can be used for multiple contact electrodes at the same time. This technique has been successfully employed to verify multiple connectivity in devices having nanometer dimensions. This characterization technique has helped us in verification of contact formation and carry out Hall effect measurement on Si NW which otherwise is considered to be very challenging and demanding.
Figure 4.26: (a) SEM image of Hall device with a width of 70 nm NW, with biased electrodes connected and labeled as 3A, 3B, 4A, 4B and 4C. This SEM image has been taken at an external bias of 0V. The electrode areas in contact are bright compared to the parts of the electrodes which are not in contact. This shows the formation of electrical contacts between Si NW and electrodes, along with the fabrication process of angled deposition technique, where Si NWs are used as a shadow mask for the fabrication of contact electrodes. The SEM image is processed in a Mathcad script. (b) Applied external bias of -1 V; (c) applied external bias of +1 V; both show the electrode is in contact with the Si NW.

4.5 Conclusions and Outlook

In conclusions, we have been successful in defining the silicon nanowire on SOI substrate by optimizing the EBL and dry etching parameters. For device fabrication contact electrodes are fabricated by two ways: first one is top contact and second one by using nanowire as a shadow mask for metal deposition. For top contact electrode fabrication, we have achieved proper asymmetric back to back Schottky barrier, this has been verified by 2-point electrical measurement. The contact resistance is also observed to be very high due to the poor contacts and/or presence of thick oxide layer around the top of nanowire or contamination present around the nanowire. This clearly suggested the poor contact between metal and semiconductor or they might not be in direct contact. To overcome this problem, the contacts are made at the side wall of the nanowire. The contamination and oxide layer at the side wall of NW is removed from Ar\textsuperscript{+} etching prior to metal deposition to achieve Ohmic contact.

The linear curves have been achieved by improving the quality of contacts (which is shown in chapter 5). The Secondary electron voltage contrast technique has been used to verify the contacts with or without Ar\textsuperscript{+} etching. This helps to optimize the duration for the use of Ar\textsuperscript{+} etching, to improve the contacts’ fabrication. Hence, by using this technique we have showed that intimate contact has been made between metal and semiconductor. In chapter 5, 2-point I-V characteristic of the devices which were fabricated with the use of Ar\textsuperscript{+} etching is shown and followed by 4-point measurement with improved contacts. These 4-point measurement results have been shown in chapter 5 where linear curve has been achieved. The electrical measurement has been done to compare the bulk and Silicon nanowire of different widths from 30 nm to 500 nm.
Chapter 5

Electrostatics Analysis and Electrical Measurement of Silicon Nanowire

5.1 Introduction

Since the majority of applications for Si nanowires in the area of transistors, photovoltaics, biosensors and optoelectronics depend on the material properties of silicon, the understanding of electron transport in Si nanowires is essential. In addition, the direct measurement of different parameters gives better insight into the phenomenon taking place rather than inferring them from indirect measurement. The specially designed Hall bar type structure has been used to extract resistivity, mobility and carrier concentration in ultra-thin nanowires. As shown in chapter 4, we have optimized process parameters for EBL and dry etch to realize Si nanowires of different widths having minimum plasma induced damage and small side wall roughness. In order to carry out meaningful electrical measurement using the Hall structure, the formation of good quality Ohmic contacts is critical.

In the previous chapter we have optimized the processes used for fabricating contacts between metal and semiconductor. The problems of non-linear I-V characteristics observed between metal/Si NW along with large barrier height encountered after making top contacts to the etched Si NW were discussed. To achieve Ohmic contacts, prior to metal deposition, in-situ etching by Ar\(^+\) ion in the same vacuum environment is carried out to remove any native oxide/contamination present on the surface.
For non-degenerate semiconductors, the depletion approximation allows the side wall depletion width to be determined which reduces the electrical width of any conducting channel. Consistent with the reported results by Mirza et al., we have also observed poor conduction in silicon nanowires below 30 nm, fabricated on SOI substrates and having a carrier concentration around $4 \times 10^{19}$ cm$^{-3}$ [4]. This has been supported by theoretical calculations [43]. In our case where the doping is of the order of $5 \times 10^{18}$ cm$^{-3}$ at BOX to $5 \times 10^{19}$ cm$^{-3}$ at surface the depletion width is expected to be enhanced resulting in poor conduction for 30 nm wide Si nanowires. The non-uniform doping density of Si NWs has resulted in non-consistency in measurements for the fabricated devices.

Systematic experiments are carried out to analyze and solve contact resistance problem in etched Si NWs. This chapter deals with our experimental approach to achieve good quality Ohmic contacts to Si nanowires. The results of electrical measurements carried out on these Si nanowires, having widths ranging from 60 to 250 nm are included. These results obtained on nanowires are compared with measured data on silicon films on SOI substrates.

5.2 Experimental

The top down approach followed for Si NW device fabrication is discussed in chapter 4. We have used an angled deposition technique for electrode deposition in order to contact Si NWs for electrical characterization. In fact, the active doping level in Si NWs plays an important role in the transport of electrons. In view of this, the doping concentration of the device layer on SOI substrates is characterized using SIMS (Secondary Ion Mass Spectrometry). The SIMS profile of the device layer is shown in figures 5.1. The doping level is of the order of $5 \times 10^{18}$ cm$^{-3}$ at BOX to $7 \times 10^{19}$ cm$^{-3}$ at surface and its distribution within the thickness can be seen from the figure 5.1. It is apparent from the SIMS profile that doping is lower towards the Si/Oxide interface and higher towards the surface. Furthermore, although the RIE-ICP etching results in anisotropic etching, the bottom portion of the Si nanowires always have slightly lower dimensions than the top.

The non-ideal I-V characteristics are observed for Si NWs fabricated using conventional fabrication steps (without the use of Ar$^+$ etching step) as shown in figure 5.2. The problem is thoroughly analyzed using Transmission Electron Microscopy and it shows that an additional etch step should be introduced to remove any contamination or native interfacial oxide present at the surface/sidewalls (see figure 5.6). The etch rate using an Ion beam etching process is investigated and optimized. To reduce the re-growth of the oxide, a vacuum environment of $3 \times 10^{-4}$ Torr was maintained in Electron beam evaporator system (Temescal FC 2000), which is equipped with an Ar$^+$ ion gun etcher inside the
chamber (see section 3.1.4). Ar\textsuperscript{+} ions are used to clean the surface before depositing the metal. This process has been observed to result in reducing the oxide barrier. Different metals such as Ti/Au, Al and Ni have also been investigated in order to achieve good quality electrical contacts and interfaces.

5.3 Results and Discussion

The two-point contact DC measurements are carried out on Si NWs having different widths. The non-linear I-V characteristics have been observed for all nanowire widths ranging from 60-250 nm.

A typical example of non-linear I-V characteristics for Si NW having 100 nm width with large energy gap of ± 0.5 V is shown in figure 5.2. The non-linear I-V characteristics in Si nanowires can be attributed to Schottky behavior at the source and drain end of the channel. Similar non-linear I-V characteristics have also been observed by Mirza et.al.[4] on Si nanowires, having widths around 12 nm, with doping concentration of 2\times10^{19} \text{ cm}^{-3} for which the depletion effect becomes significant. In our case the doping level is 5\times10^{19} \text{ cm}^{-3} with nanowires of width >30 nm and this results in non-linear behavior which might not only be due to depletion effects in NWs’ structure but probably due to a large barrier height and a high contact resistance.

Further, it is well known that ICP-RIE works on the principle of polymer inhibitor deposition for the sidewall protection during high aspect ratio etching and is prone to contamination at the surface (see section 3.1.3). Also silicon is known to have a native oxide even if it is exposed to atmosphere only for a short duration. It is concluded that any contamination resulting from dry etching and thin native oxide present at the nanowire surface may be responsible for high contact resistance in our case. In order to remove these contaminations prior to metal deposition for fabricating contact electrodes
Figure 5.2: I-V characteristics show 2-point electrical measurement for (a) two samples (sample 1-green and sample 2-red) of Si nanowire of 100 nm width, the thickness is 45 nm, the metal deposited at the side wall of nanowire is Ti/Au (10/60 nm), the applied voltage is \( \pm 1 \) V (b) fitted data shown in magenta and experimental data is shown in blue i.e. average value of sample 1 and sample 2. The rms value of fit error is 6.57 pA. The data is fitted by using equation 2.53.

In reality, the ideal situation of contaminate-free metal/semiconductor contacts is never reached, because there is usually a thin oxide layer, about <1-2 nm thick, on the surface of the semiconductor. Such an oxide film is referred to as an interfacial layer. However, this layer is so thin that electrons can penetrate it quite easily by quantum-mechanical tunneling [4, 75]. Also there will be a presence of charge on the surface of the semiconductor known as localized surface states. In general, the Fermi level does not coincide with the neutral level, so there will be a net charge in the surface states in addition to a thin oxide layer between the metal and the semiconductor.

By applying an external voltage \( V \), charge carriers can be transported across a Schottky barrier via emission of carriers over the top of the barrier (Thermionic Emission), quantum-mechanical tunneling through the barrier (Field Emission), both processes occurring simultaneously (Thermionic Field Emission). There will be a flow of electrons from the semiconductor to the metal and vice versa \( V \gg 3kT/q \) for forward biasing and \( V \ll 3kT/q \) for reverse biasing [75].

For this study, prior to the use of Ti/Au, alternative metals such as Nickel and Aluminum have been used for fabricating the contact electrodes. Based on equation 2.36 in section 2.6.1 the barrier height, \( \phi_b \), varies for different metals based on their work function. The work function of the silicon (intrinsic) is 4.15 eV which changes with the doping concentration of the carrier. For n-type and highly doped silicon the work function changes to around 4.85 eV [161]. However, it is difficult to conclude an exact number since the work function varies with the sample preparation as well. The electron affinity of silicon is 4.05 eV which does not change with doping, however, it is affected by the
surface properties. The Ni metal has a work function of 5.04 eV- 5.35 eV which is greater than the work function of n-type highly doped Si. So the barrier between the metal and semiconductor will be large (see figure 5.3 shown in red). Thus, the electrons pass from the Si into the metal in order to equalise the Fermi levels, leaving behind a depletion region in the Si, in which the bands are bent upwards. Hence, resulting in a larger width of depletion region. The other metal used in this study is Al which has a work function of 4.06-4.26 eV, which is lower than the silicon work function. However, aluminum oxidises very easily, and therefore tends to modify the chemical nature of any oxide that may be present on the surface of the silicon [75]. This could explain the increase in barrier height in n-type Silicon contacted with an Aluminum electrode as shown in the IV curve, figure 5.3 (in blue). The metal Ti has a work function of 4.33 eV which is more compatible with n-type highly doped Silicon. Using equation 2.36 the barrier height ($\phi_b$) is calculated and found to be 0.28 eV for Ti, 1.0 eV for Ni and 0.23 eV for Al, at room temperature. Hence, we continued the use of Ti/Au metal as the contact electrode to the Si NW which later shows the reduction in barrier height on improving the contact fabrication. However, the contact formation depends on other parameters as well such as Silicon crystal structure, the surface, its defects and impurities. In experiments, it has been found that the barrier height does not entirely depend on the work function of metal [75].

![Figure 5.3: J-V characteristics show 2-point electrical measurement of: 1) Si nanowire of width 50 nm, the thickness is 45 nm, the metal deposited is Ni-70 nm (red). 2) Si nanowire of width 150 nm, of thickness 45 nm and the metal deposited is Al-50 nm (blue). Metal is deposited immediately after Ar$^+$ etching. During this measurement applied voltage is $\pm$ 1 V. We have four samples of Si nanowire out of which two samples are deposited with Al-50nm and two with Ni-70nm, all have same thickness. This graph has been plotted by taking the average values of both samples for Al and Ni.](image-url)
To find the dependence of the barrier height on the width of the Si NW, the barrier height is obtained from 2-point non-linear IV characteristics (measured in 2-point configuration, as of the high impedance of the device) from figures 5.2(a), 5.4(a), (b) and 5.5(a), by fitting in equations 2.51, 2.52 and 2.53 given in Chapter 2 under section 2.7.3. The values of fit parameters shown in the table 5.1 and 5.2 are extracted from the fitted graph shown in figures 5.2(b), 5.4(c), (d) and 5.5(b).

In (c) and (d) at low biases there appears to be a region with low resistance. This is an artifact from the modeling equation 2.53, which does not take some of the parallel current limiting mechanisms into consideration. These do not appear in the actual measured characteristics and the discrepancy can be resolved without adding a large number of free parameters, by introducing a shunt resistance to the model [75].

Figure 5.4: I(V) characteristics obtained in the 2-point configuration, applied voltage is ±1 V, (a) of a Si nanowire width 150 nm, for two samples (sample 1-green and sample 2-red) and the metal deposited is Al-50 nm, (b) for Al the fitted curve is extracted by using back to back Schottky model, magenta shows the fitted data and blue is the experimental data i.e. average value of sample 1 and sample 2, the rms value of fit error is 9.2 nA (c) of a Si nanowire width 50 nm, for two samples (sample 1-green and sample 2-red) and the metal deposited is Ni-70 nm, (d) for Ni the fitted curve is extracted by using back to back Schottky model, magenta shows the fitted data and blue is the experimental data i.e. average value of sample 1 and sample 2, the rms value of fit error is 1.01 nA.

The equations 2.51 and 2.52 in section 2.7.3 show the voltage dependence of the barrier height and the effect of tunneling through the barrier at the interface. There are several reasons why the barrier
Figure 5.5: I(V) characteristics obtained in the 2-point configuration of two samples (sample 1-green and sample 2-red), of Si nanowire of 100 nm width, the thickness is 45 nm, the metal deposited at the side wall of nanowire is Ti/Au-10/60 nm, immediately after Ar$^+$ etching. The applied voltage is ±1 V. In (b) the fitted curve is extracted by using back to back Schottky model, magenta shows the fitted data and blue is the experimental data i.e. average value of sample 1 and sample 2, the rms value of fit error is 0.476 µA. At low biases there appears to be a region with low resistance. This is an artifact from the modeling equation 2.53, which does not take some of the parallel current limiting mechanisms into consideration. These do not appear in the actual measured characteristics and the discrepancy can be resolved without adding a large number of free parameters, by introducing a shunt resistance to the model [75].

There have been two sets of samples with same dimensions, on which same measurements have been performed. From these measurements the average value has been taken and given in the tables 5.1, 5.2 and 5.3.

From the table 5.1, it can be concluded that the barrier height does not depend on the width of the NW and the metal but mainly depends on the preparation method and surface properties.

<table>
<thead>
<tr>
<th>Metal</th>
<th>Thickness (nm)</th>
<th>Width (nm)</th>
<th>$\phi_1$ (eV)</th>
<th>$\phi_2$ (eV)</th>
<th>$\eta_1$</th>
<th>$\eta_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti/Au without Ion etching</td>
<td>70</td>
<td>100</td>
<td>0.48</td>
<td>0.48</td>
<td>1.1</td>
<td>1.1</td>
</tr>
<tr>
<td>Al with Ion etching</td>
<td>50</td>
<td>150</td>
<td>0.26</td>
<td>0.26</td>
<td>1.1</td>
<td>1.1</td>
</tr>
<tr>
<td>Ni with Ion etching</td>
<td>70</td>
<td>50</td>
<td>0.28</td>
<td>0.27</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Ti/Au with Ion etching</td>
<td>70</td>
<td>100</td>
<td>0.17</td>
<td>0.17</td>
<td>1.0</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Table 5.1: These fit parameters $\phi_1$ (eV), $\phi_2$ (eV), $\eta_1$, $\eta_2$ were obtained by fitting the data in figure 5.2, 5.4, 5.5 using equation 2.53. The parameters $\phi_{1,2}$ are barrier heights and $\eta_{1,2}$ are ideality factors of both Schottky barriers.

In view of the above, TEM characterization is carried out on 150 nm wide Si NW fabricated using a NW as a shadow mask. The metal Ti/Au is deposited after 30 seconds of Ar$^+$ etching. The cross sectional view of silicon NWs and metal/nanowire interface is shown in figure 5.6. The magnified TEM image of the interface clearly shows the presence of a barrier layer of silicon dioxide of thickness...
2-3 nm at the interface between the metal and the Si NWs. It clearly shows that there is a requirement to use the Ar\(^+\) ions for a longer duration to remove the barrier layer to achieve intimate contact.

![TEM images](image)

Figure 5.6: TEM images (a) Cross-sectional image of Si Nanowire side wall deposition with Ti/Au (b) Magnified image at the interface of Si and Ti showed the barrier layer silicon dioxide of 2 nm-3 nm at the interface.

In an attempt to achieve good quality Ohmic contacts to the Si NWs, the ion beam etching process is optimized to 60 seconds of etching for the removal of native oxide and contamination. Furthermore, in order to cancel out the effect of contact resistance four point electrical measurements are carried out on Si NWs of different widths. The schematic diagram of the test structure is shown in figure 5.7 where the current is pumped at two outer electrodes, source and drain, and the voltage is measured between the two electrodes lying in between.

![Schematic diagram](image)

Figure 5.7: SEM image and schematic diagram of Si nanowire of width \(w\), the thickness is 45 nm, the distance between the contact electrode is \(l\). The four electrodes are contacted at the side wall of the nanowire.

The schematic diagram for the Si NW device and layout used for the DC electrical measurement are shown in figure 5.7. \(l\) is the length over which the electric current is flowing (active conduction channel
length) in 4-point electrical measurement. The active conduction-channel length is implicitly assumed to be lying between the inner edges of the voltage probe electrodes to avoid the effect of contact resistance. So the distance between the inner electrodes were taken to determine the resistivity of the Si NWs [131, 162, 163]. The DC characteristics measured on the Si NWs after the Ar\(^+\) etching process of 60 seconds is shown in figure 5.8. A reduction in the Schottky barrier height is observed after 60 seconds of Ar\(^+\) etching and good quality Ohmic behavior is achieved (see figure 5.8).

![Graphs showing I-V characteristics for different Si NW widths](image)

**Figure 5.8:** I-V characteristics showed voltage drop across the Si nanowire of 60 nm to 250 nm in width, the thickness is 45 nm, the metal deposited is Ti/Au-10/60 nm, immediately after 60 seconds of Ar\(^+\) etching the applied voltage is ± 1 V (a) for the 60 nm width Si NW (b) for 90 nm width Si NW (c) for 250 nm width Si NW and (d) for 200 nm width Si NW.

The four I-V curves shown in the figure 5.8 are voltage drop values across the nanowire. The different graphs represent IV curves for Si nanowires of different diameter. The ±2 V has been applied at the outer electrodes, Source and Drain. In 2-point measurement, current measured across those 2 electrodes, gives us back to back Schottky barrier (see figure 5.9 (a) & (b)). The voltmeter connected across the inner electrodes has measured a voltage drop of ±50 mV. The large difference
in voltage values is due to the barrier properties, i.e. the large contact resistance of the nanowire.

From table 5.1 we can conclude that the barrier height is reduced on using Ti/Au metal after optimizing Ar$^+$ etching duration as this process reduces the insulating layer between the metal and Si NW. Thus, the ideality factor $\eta$ is also close to 1.0 compared to other metals used. Hence, we continued with this methodology and used Ti/Au metal of thickness 70 nm for the contact electrodes.

Figure 5.9 (a), (b) & (c) shows the 2-point IV characteristics of Si NWs. The IV characteristics have been shown of two samples, sample 1 (green) and sample 2 (red). The current (A) average of these two samples has been taken, and used to obtain the fit parameter in figure 5.9 (d), (e) & (f) using equations 2.51, 2.52 and 2.53. Fit is shown in magenta and experimental i.e. current average value of two samples is shown in blue. The rms value of fit error is given in the table 5.2. The value of barrier height is extracted for Si NW of different widths from 60 nm to 250 nm (see table 5.2) on an average the barrier height is found to be 0.2 eV.

<table>
<thead>
<tr>
<th>Width (nm)</th>
<th>$\phi_1$ (eV)</th>
<th>$\phi_2$ (eV)</th>
<th>$\eta_1$</th>
<th>$\eta_2$</th>
<th>fit error</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>0.19</td>
<td>0.19</td>
<td>1.0</td>
<td>1.0</td>
<td>0.62 nA</td>
</tr>
<tr>
<td>90</td>
<td>0.24</td>
<td>0.23</td>
<td>1.0</td>
<td>1.0</td>
<td>11.4 nA</td>
</tr>
<tr>
<td>200</td>
<td>0.24</td>
<td>0.22</td>
<td>1.0</td>
<td>1.0</td>
<td>45.7 nA</td>
</tr>
<tr>
<td>250</td>
<td>0.25</td>
<td>0.24</td>
<td>1.1</td>
<td>1.0</td>
<td>0.51 $\mu$A</td>
</tr>
</tbody>
</table>

Table 5.2: These fit parameters $\phi_1$, $\phi_2$, $\eta_1$, $\eta_2$ were obtained by fitting the data in figure 5.9 using equation 2.53.
Figure 5.9: I(V) characteristics obtained in the 2-point configuration of Si nanowires of thickness 45 nm, the metal deposited is Ti/Au-10/60 nm, immediately after Ar$^+$ etching (a) Si NW is 60 nm wide, (b) Si NW is 90 nm wide (c) Si NW is 200 nm wide. (d), (e) and (f) show the fitted curve extracted by using back to back Schottky model in equation 2.53. At low biases there appears to be a region with low resistance. This is an artifact from the modeling equation 2.53, which does not take some of the parallel current limiting mechanisms into consideration. These do not appear in the actual measured characteristics and the discrepancy can be resolved without adding a large number of free parameters, by introducing a shunt resistance to the model [75].
5.3.1 Comparison between Silicon Films and Nanowires

In order to assess the change in material and transport properties at the nanoscale level with that of the bulk material, the four-point resistivity measurements are performed on the Si film sample at 300 K and 10 K. Using equation 2.4 for resistivity, equation 2.7 for conductivity, equation 2.8 for mobility, equation 2.25 for diffusion coefficient, and equation 2.32 for scattering time, values for Si film and for Si NWs of different width are obtained.

From the obtained value of resistivity for the Si film, from 4-point probe measurement, it is confirmed that the carrier concentration is \( \approx 10^{19} \text{ cm}^{-3} \) [164] (see figure 5.10 (a) and (b)), which also matches well with SIMS results of the same sample given in figure 5.1. At low temperature 10 K, the resistivity reduced to \( \rho=0.005 \Omega\text{-cm} \) and calculated the conductivity mobility to be 122 cm\(^2\)/Vs. The mobility increases at low temperature as phonons freeze out [164]. According to the literature, the mobility for highly doped silicon is 100 cm\(^2\)/Vs for electrons (see figure 5.10 (c)) and 50 cm\(^2\)/Vs for holes [62, 164–166]. The reasons for the low mobility for highly doped silicon are point defects such as excess of vacancies with the formation of neutral or charged E-centres and excess of interstitials. A high dose of implants can also modify the crystalline structure to amorphous and scattering. In highly doped silicon the minority carriers are suppressed by majority carriers [165–168] (see section 2.5 for details on types of scattering). The DC electrical measurements are well matched with the literature for the silicon films.

![Figure 5.10](image)

Figure 5.10: (a) The IV characteristics of 4-point electrical measurement of Si film at 300 K (b) shows the resistivity vs carrier concentration for Si material [62] (c) the calculated value of electron mobility with carrier concentration [169].

For Si NWs, the transport properties are measured and the values for mobility, resistivity, scattering time and diffusion coefficient are obtained, see table 5.3 and 5.4. For these parameters, the effective mass of \( m^* = 0.98 m_e \) [170], where \( m_e \) is the mass of electron. The resistance of these Si NWs, having widths in the range of 60 nm to 250 nm, are obtained from the I-V curves shown in figure 5.8. The obtained values of mobility are very low for these Si NWs perhaps due to the increased probability...
of scattering between states, inspite of the fact that the number of available states to scatter into is reduced. This effect becomes negligible once the effective electrical length of the nanowire reaches to near quasi ballistic transport. We have observed an increase in the mobility for 60 nm wide Si NW, which could be due to the formation of a depletion region resulting in reduced electrical lengths at the interface suggesting quasi-ballistic transport in this case. However, the channel is still conductive due to quantum tunneling at the device scale. Muhammad M. Mirza et al [4] have suggested that the doping density above the Mott criterion [171] depletes the conducting part of the nanowire and would result in reduced dimensionality for electron transport to quasi-1D, which we have observed for sample of 60 nm width. The effect of doping density and NW size on the transport properties is further investigated in section 6.4.

We have considered the effective cross-sectional area for Si nanowire of width <100 nm. Samples of different width 60 nm and 90 nm both with thickness of 45 nm, due to formation of depletion layer, changed to be 50 nm and 82 nm in width and 38 nm in thickness. The formation of depletion layer has been calculated based on the carrier concentration of Si NW, the graph has been plotted in figure 6.15 in section 6.4. 7 nm from the bottom of the Si NW and 4-5 nm from the side wall of Si NW are assumed to be depleted.

<table>
<thead>
<tr>
<th>Width(nm)</th>
<th>Mobility (cm²/Vs)</th>
<th>Conductivity(S/cm)</th>
<th>Resistance (Ω)</th>
<th>l (µm)</th>
<th>Resistivity(Ω cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>film</td>
<td>(100±0.1)</td>
<td>(160±0.1)</td>
<td>(347.1±0.25)</td>
<td>1000</td>
<td>0.006</td>
</tr>
<tr>
<td>250</td>
<td>(4.93±0.05)</td>
<td>(7.89±0.08)</td>
<td>(94±0.9)k</td>
<td>0.834</td>
<td>(0.126±0.001)</td>
</tr>
<tr>
<td>200</td>
<td>(14.87±0.1)</td>
<td>(23.8±0.15)</td>
<td>(32.5±0.04)k</td>
<td>0.7</td>
<td>(0.042±0.001)</td>
</tr>
<tr>
<td>90</td>
<td>(59.52±0.57)</td>
<td>(95.23±0.91)</td>
<td>(21.7±0.2) k</td>
<td>0.643</td>
<td>0.01</td>
</tr>
<tr>
<td>60</td>
<td>(230.13±2.7)</td>
<td>(369.82±4.3)</td>
<td>(12±0.14) k</td>
<td>0.843</td>
<td>(2.7±0.031)×10⁻³</td>
</tr>
</tbody>
</table>

Table 5.3: Summary of the properties of Silicon Nanowire based on width

These values given in the table have been calculated by assuming the value of carrier concentration, \( n \approx 10^{19} \text{ cm}^{-3} \). Using the value of resistance \( R \) extracted from IV characteristics (see figure 5.8 for Si NWs and figure 5.10 (a) for Si film) calculated the value of resistivity \( \rho \), conductivity \( \sigma \) and mobility \( \mu \) using the formula given in equations 2.4, 2.7 and 2.8. The mobility of Si NW changes with the width of NW as shown in figure 5.11. This drop in value of mobility with increasing thickness is entirely due to the formation of depletion regions underneath and on the side of the contacts, which effectively shrinks the thickness of the wire, thus exaggerating the mobility at small nominal nanowire thicknesses. This effect is simply due to the 1/t scaling of the electrical voltage.
Using equation 2.34, the Fermi wavelength is calculated and using these values the mean free path is determined for the film and single NW, see table 5.5. A mean free path or scattering length for electron velocities corresponding to the Fermi energy is defined in equation 2.34. This is an average length covered by an electron at the Fermi energy before scattering occurs. This mean free path depends on the doping density of the device layer as seen in table 5.5.
5.4 Conclusions and Outlook

In conclusions, we have been successful in fabricating and characterizing Si NW devices having different widths. For the formation of good quality Ohmic contacts Ti/Au are used and observed to be better than Ni and Al. Ion etching is optimized to remove inter-facial oxide and/or contamination without side wall damage resulting in a reduced barrier height of Schottky contacts. From 4-point electrical measurements the transport properties are calculated for 60 nm to 250 nm wide Si NWs and it has been found that 60 nm wide Si NW could have a reduced electrical length as it has changed its dimensionality to quasi-1D, which results in higher mobility compared to the Si film. To further investigate the transport properties of the single Si NWs Hall measurements are performed. However, the DC Hall measurement of low mobility samples can result in poor signal-to-noise ratio and suffer from additional problems, whereas AC Hall effect measurements are employed to extract the transport behavior in Si NWs with an ability to measure low mobility sample with greater resolution.

For Si NWs Hall measurements are a challenging task. Chapter 6 will discuss the effect of external magnetic field on Si NWs of different widths. It should be noted that the scattering mechanisms in the presence of a magnetic field are different and the measured Hall mobility can differ from the mobility extracted from field effect measurements.
Chapter 6

Transport in Silicon Nanowires using Hall Effect Measurements

6.1 Introduction

In the previous chapter, we reported on the measurement of the conductivity and mobility in silicon NWs. We also mentioned that our electrical measurements have some drift, resulting in variations in the measured results in some of the samples. Given this situation, it is important for us to use a robust measurement approach in order to get accurate data on the transport properties of single silicon NWs.

To investigate the transport properties of the material the most commonly used techniques are field effect and Hall effect measurement. The field effect technique has been widely and successfully utilised, but there are some limitations to this technique [7]. The first of these are the limited accessible measurement geometries, which have many inherent uncertainties, of which the estimation of gate capacitance is of primary concern and presents serious technical challenges [1]. The second problem with this technique is that it is often carried out without considering the contact resistance, possibly leading to an overestimation of the carrier concentration [2]. In addition, the depletion region consists of only a small volume in the vicinity of the gate electrode, and since measurements rely on modulation of the source drain current, which flows in a depletion region and it is only this volume which is available for characterization [7]. Hall effect measurements are a more direct measurement of the carrier concentration in nanowires and do not rely as heavily on estimations of critical input parameters, resulting in higher accuracy [7]. The Hall voltage depends on the carrier concentration
in the entire cross-section of the nanowire. Hall effect measurements are therefore the most promising method to determine the transport properties of highly doped semiconductors, and also of single nanowire [1–7]. From the Hall measurement one can determine the mobility, type and concentration of charge carrier of the material [38].

In this chapter, we report our findings on the carrier transport in silicon single NWs having widths in the range of sub 30 to 500 nm, using Hall effect measurements. The results are compared with the data obtained from silicon films on SOI substrates and µm-sized silicon bar for validation. The Hall voltage of NWs must be measured accurately and with minimized systematic uncertainty, caused, for example, by thermal effects. Therefore, AC Hall effect measurements are employed to extract the transport behavior in Si NWs. The main advantages of employing AC Hall effect measurement are the ability to measure low mobility samples with greater resolution, reduced Joule heating and the elimination of some slow thermal effects. The DC Hall measurement of low mobility samples can result in poor signal-to-noise ratio [44, 45] and cause additional problems such as enhanced electromigration, thermal gradients, thermoelectric effects and Seebeck voltages. Out of these factors, the ones that increase both the random and systematic uncertainty errors in the Hall measurement are particularly unpleasant, [46, 47] therefore here AC current sourcing has been used to minimize these problems. The AC measurement have been carried out using two distinct options: 1) Magnetic field sweeping in the range of ±14 T and 2) Sample rotation under a constant magnetic field at +14 T [172]. The effect of NW width on the transport parameters such as mobility, carrier density, resistivity, and Hall coefficient is hereby presented in this chapter.

6.2 Hall Measurement on Film

The Hall effect, measured on gold leaf, was first discovered by Edwin Hall in 1879. In 1958, Leo J. van der Pauw introduced the method of calculating the properties of materials of irregular shaped samples without knowing the current pattern [173, 174]. The contacts are required to be small, uniform, and formed at the corner of the sample for more accurate measurement as shown in the figure 6.1. In our case the sample is roughly 0.6 mm by 0.6 mm. The contacts are made at the 4 corners using Indium metal soldering. The following parameters of the material have been extracted by combining Hall effect measurements with Van der Pauw method:

- The resistivity of the material.
- The doping type (i.e. whether it is a p-type or n-type material).
• The sheet carrier density of the majority carrier (the number of majority carriers per unit area).

• The mobility of the majority carrier.

Resistivity value has been extracted from Van der Pauw method and other parameters are extracted by combining this method with Hall effect [173, 174].

![Figure 6.1: Schematic Diagram of Si substrate, contacted at the edges of the surface of Si film to measure the resistivity, by using Van der Pauw technique.](image)

The measurements on silicon film on SOI wafer are carried out at constant current of 2 mA at temperature 300 K and at 10 K. The magnetic field applied is ±14T. By applying the current in horizontal and vertical direction, the voltage drop across the other two contacts is measured. After taking the average value of measured resistance, the sheet resistance is calculated. Standard formulas given in the following equations 6.1, 6.2, 6.3 are used to calculate the resistivity, sheet carrier concentration (the number of majority carriers per unit area), and mobility of Si films.

Resistivity,

\[ \rho = R_{sh}.t \]  

(6.1)

Sheet carrier concentration,

\[ n_s = \frac{B.I}{V_H q} \]  

(6.2)

Hall mobility,

\[ \mu_H = \frac{1}{qR_{sh}n_s} \]  

(6.3)

Using the above equations parameters of the Si film of thickness 45 nm are calculated. These parameters are given in the following table (6.1):
In addition to above, temperature dependence of mobility and other electrical parameters is also investigated and reported in the following in order to understand the scattering mechanisms taking place inside the Si film.

The carriers moving through a semiconducting channel undergo a variety of interactions with it and the nature of these interactions can be determined from the mobility of the channel. To determine the scattering mechanism which limits the mobility in the conducting channel, the temperature dependence of experimental Hall mobility is compared to a number of theoretically calculated values for specific scattering mechanisms. Also included are the measurement results on Si films, bars and nanowires.

The effect of temperature on the resistance, mobility and scattering has been measured on Si film, as shown in figure 6.2. Consistent with bulk properties of highly-doped semiconducting material, having doping concentration of $5 \times 10^{19} \text{ cm}^{-3}$ at surface, the resistance decreases with temperature and behaves like a metal at low temperature. However, a hump is observed at 25 K, which is known as degeneracy temperature, it increases again at 10 K indicating behavior like an impure metal (see figure 6.2 (a)). This hump may be caused by some sort of resonance in scattering by impurities [168], [175]-[176]. The increase in mobility at low temperatures, consistent with heavily doped bulk Si properties can be seen from figure 6.2 (b). The semiconductor material properties are highly affected by the ionized and neutral impurities or defect scattering process [176]. Lattice scattering dominates at high temperature and impurity scattering dominates at low temperature [176]. In highly doped silicon the increase of effective carrier velocity occurring as a result of the Fermi degeneracy could cause the low mobility at room temperature and high mobility at low temperature [168]. With increasing temperature, phonon concentration increases and causes increase in scattering. Thus, lattice scattering lowers the carrier mobility more and more at higher temperature [168]. Theoretical calculations reveal that the mobility in non-polar semiconductors, such as silicon, is dominated by acoustic phonon interaction. The resulting mobility is predicated to be proportional to $T^{-3/2}$. But from our results it is observed to be proportional to $T^{-0.25}$ which is different than predicated. This
Figure 6.2: Temperature varies from 300 K to 10 K for silicon device layer (a) Resistance vs temperature (b) Mobility plotted against temperature (c) log-log plot of temperature vs mobility.

indicates, that the phonon scattering is not relatively dominated at high temperature as expected (see figure 6.2 (c)).

6.3 Hall Measurement on Silicon Hall Bars

To measure the transport properties of any material accurately from Hall effect, Hall bar geometry design is critical but known. The Hall bar geometry on SOI substrate used in this investigation is shown in figure 6.3. For the fabrication, we have used negative resist maN-1420 as etch mask for patterning of Hall bar structure. After spin coating at 3000 rpm, it is baked at 115°C for 2 minutes followed by the UV exposure (see section 3.1.1) under vacuum contact for 23 seconds. The exposed resist is developed in ma-535 for 1 minute and rinsed in DI water. After post bake at 100°C for 2 minutes, the pattern is etched using the RIE-ICP etching (see section 3.1.3) process for 15 seconds using same recipe as discussed before, followed by removal of the resist using acetone. The contact electrodes are made using positive resist S1813 and metal lift off process using standard UV litho
steps discussed earlier. To remove any contamination and insulating layer of oxide \( \text{Ar}^+ \) etching prior to metal deposition is carried out and Ti/Au of thickness 10/60 nm is used for metal contact.

![Schematic diagram of Silicon Hall Bar geometry.](image)

The electrical measurement is carried out at applied current ± 0.5 mA at 0 T magnetic field. Both two-point and four-point IV characteristics are measured at RT and at 10 K, see figure 6.4. Ohmic behavior can be seen from the curves except at low temperatures. The carrier concentration is considered to be \( 10^{19} \text{ cm}^{-3} \).

The temperature dependence on resistance of these Si Hall bars is measured and shown in figure 6.5. It follows similar behavior as in the case of Si film showing bulk property except at lower temperatures where a kink is observed. This could be due to the formation of depletion region.

For Hall measurement the applied current is kept constant at +0.5 mA for Silicon Hall bar of 60\( \mu \text{m} \times 10 \mu \text{m} \) and -0.5 mA for 60\( \mu \text{m} \times 20 \mu \text{m} \) and the magnetic field perpendicular to the sample is swept between ±14 T (see figure 6.6). The Hall coefficient, longitudinal resistivity and Hall mobility are calculated using the following equations 6.4, 6.5, 6.6 and the results are given in table 6.2.

Hall coefficient \( \text{cm}^3/\text{C} \)

\[
R_H = \frac{V_{H.I}}{B.I} \tag{6.4}
\]

Resistivity \( \Omega - \text{cm} \)

\[
\rho_{xx} = \frac{V_{xx.A}}{I.I} \tag{6.5}
\]

Hall mobility \( \text{cm}^2/\text{V.s} \)

\[
\mu_H = \frac{R_H}{\rho_{xx}} \tag{6.6}
\]

\[
n = -\frac{1}{qR_H} \tag{6.7}
\]
Figure 6.4: IV characteristics of Silicon Hall Bar (a) 60μm by 20μm at 300 K (b) 60μm by 20μm at 10 K (c) 60μm by 10μm at 300 K (d) 60μm by 10μm at 10 K
Figure 6.5: Temperature varies from 300 K to 10 K and recorded the Resistance value across the Hall electrode for Hall bar size 60µm by 20µm. The contacts may have experienced some drift at 80 K which could result in this fluctuation while going down to low temperature, this is due to the silver paste contacts used to bond the sample with the chip carrier.

Table 6.2 contains the data which has been calculated from the Hall measurement performed on Si Hall bar devices of two different sizes 60µm by 10 µm and 60µm by 20 µm in the temperature range of 300 K to 10 K. The value of Hall voltage $V_H$ and longitudinal voltage $V_{xx}$ has been extracted from the Hall measurement. In figure 6.6 the examples of measurement have been shown for both devices at two different temperatures 300 K and 10 K.

<table>
<thead>
<tr>
<th>Hall bar(µm²)</th>
<th>Temp(K)</th>
<th>Hall Coefficient(cm³/C)</th>
<th>Mobility(cm²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 by 20</td>
<td>300</td>
<td>0.171</td>
<td>183.8</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>0.186</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>0.2007</td>
<td>230</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>0.2097</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>0.2268</td>
<td>270</td>
</tr>
<tr>
<td>60 by 10</td>
<td>300</td>
<td>0.3213</td>
<td>214.2</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>0.3232</td>
<td>230.8</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>0.3213</td>
<td>267.75</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>0.2745</td>
<td>290.4</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>0.2925</td>
<td>300</td>
</tr>
</tbody>
</table>

Table 6.2: Hall measurement on the silicon Hall bar

It is apparent from the table 6.2, that the mobility is observed to increase as the width of the Hall
Figure 6.6: Hall measurement of Silicon Hall Bar (a) 60µm by 20µm performed at 300 K, the magnetic field swept from 0 T to +14 T to -14 T, due to contacts the graphs shows the blue tail for longitudinal resistance measurement (b) 60µm by 10µm performed at 300 K, this has the same reason but in this case the contacts are more stable (c) 60µm by 20µm performed at 10 K (d) 60µm by 10µm performed at 10 K. $V_{xy}$ denotes transverse voltage and $V_{xx}$ denotes longitudinal voltage.

bar is decreased at a given temperature. Also the mobility increases as the temperature varies from 300 K to 10 K. The observed increase in mobility at low temperature is mainly due to the freeze out of phonons, which reduces the scattering events.

**Carrier concentration of Si Hall bar:** Carrier concentration for Si Hall bar has been calculated using equation 6.7, and it is in range of $1.93 \times 10^{19}$ to $3.65 \times 10^{19}$ cm$^{-3}$. The carrier concentration for Si Hall bar is also in agreement with measured surface doping level of Si film (see figure 5.1).

**Magnetoresistance of Si Hall bar:** The resistivity, $\rho_{xx}$ (Ω-cm), for a Hall bar of dimensions 60µm by 20 µm is $9.3 \times 10^{-4}$ Ω-cm at 300 K which changes to $8.4 \times 10^{-4}$ Ω-cm at 10 K. On further reducing the dimension of Hall bar to 60µm by 10 µm, the resistivity is $15 \times 10^{-4}$ Ω-cm at 300 K and $9.75 \times 10^{-4}$ Ω-cm for 10 K.

At room temperature, the value of longitudinal voltage is $\sim 0.32$ V for a Hall bar of dimensions 60
μm by 20 μm, on applying the magnetic field from 0 to 14 T the voltage changes by 1.7 mV. For Hall bar of dimensions 60 μm by 10 μm, the longitudinal voltage is ~ 1.0 V and the change with respect to magnetic field is 5.5 mV. This measurement is smooth and reproducible at room temperature whereas at low temperature, 10 K, a substantial thermal drift is also present in the measurements. At low temperature, the values of longitudinal voltage have been slightly reduced to ~ 0.29 V for the Hall bar dimension 60 μm by 20 μm with respect to the magnetic field, and the change in voltage is 4 mV. For the Hall bar dimension with 60 μm by 10 μm the longitudinal voltage is ~ 0.65 V, with respect to the change in magnetic field the change in voltage is 8 mV. The dependence is quadratic, as expected.

The mean free path is compared for film and Hall bar based on the above mobility values and considering the carrier concentration to $10^{19}$ cm$^{-3}$. This is given in the table 6.3 below.

<table>
<thead>
<tr>
<th>Shape</th>
<th>mean free path (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>film</td>
<td>5.9</td>
</tr>
<tr>
<td>Hall bar size-60 μm by 20 μm</td>
<td>10.89</td>
</tr>
<tr>
<td>Hall bar size-60 μm by 10 μm</td>
<td>12.75</td>
</tr>
</tbody>
</table>

Table 6.3: Effect of shape on mean free path

In order to investigate further the effect of size on the transport properties of highly doped silicon, the nanowire from 30 nm to 500 nm in width were fabricated and side contacted for Hall measurement (see section 4.2 and 4.4). The obtained results are mentioned in the next section 6.4.

### 6.4 Hall Measurement on Silicon Nanowire

In this section, we report the result obtained from Hall measurements carried out on Si NWs of different widths, ranging from 30 to 500 nm, with magnetic field swept from ± 14 T. It is apparent from our earlier measurements that our silicon device layer is of low mobility. Thus, it is difficult to carry out measurement in DC field because the noise signal can dominate easily [177].

To overcome this problem, we have used AC techniques to measure the Hall effect on these silicon nanowires. The use of an A.C field can eliminate the above mentioned issues with D.C field, because it accepts the signal at a particular frequency and rejects signals at all other frequencies and their effect. AC measurement can measure low mobility samples with greater resolution and also reduces electron heating [4]. The additional advantage to switch to AC measurement is the contribution to the transport properties that are not only determined by the majority carrier but minority carrier as well.
We have used AC Hall measurements by using two approaches: one with ramping the magnetic field within \( \pm 14 \, \text{T} \) \cite{45} and other by rotating the sample in the \( xz \) plane from \(-5^\circ\) to \(365^\circ\), keeping the magnetic field constant \cite{172}. This approach minimizes the use of liquid Helium resources, while shortening substantially the acquisition time and therefore improving the susceptibility towards thermal drift without compromising the accuracy of measurement. The Hall measurement set-up is given in details in the section 3.3.3.

The Hall signal of these Si NWs is obtained using Lock-in-Amplifier (LIA), as shown in figures 6.7 and 6.8 (a & b). \( V_X \) in-phase and \( V_Y \) quadrature are raw data (more details of the measurement are given in the section 3.3.3). These are the raw data values which need to be corrected for an offset. This offset occurs due to cable and sample mounting spurious capacitance resulting in phase shifts to the acquired AC signals, which increase approximately linearly with frequency. When \( V_y \) is adjusted to zero, \( V_x \) contains the true value of the Hall signal, at least at sufficiently low frequencies.

Using equation 2.2 value of resistance \( R \) has been extracted and from equation 2.4 value of resistivity has been derived for both anti-symmetric and symmetric resistivity (for more detailed derivations see appendix A, equations A.13, A.14, A.19 and A.20). The Hall resistivity for the anti-symmetric, \( \rho_{XY} \), using equation 6.8 and the symmetric, \( \rho_{XX} \), using equation 6.9 has been derived. These derivations need to be done due to the small offset of opposing transverse contact electrodes, similar symmetrisation and antisymmetrisation operations have been done in \cite{3}.

\[
\rho_{XY}(B) = \frac{\rho(B) - \rho(-B)}{2} \quad (6.8)
\]
\[
\rho_{XX}(B) = \frac{\rho(B) + \rho(-B)}{2} \quad (6.9)
\]

The data in figure 6.7 and 6.8 (c & d) is fitted using non-linear regression with the aid of a standard non-linear least squares regression routine (for more details see equations A.25 and A.26 in appendix A) for symmetric (\( \rho_{XX} \)) and anti-symmetric (\( \rho_{XY} \)) resistivity, thus fitted values have been extracted.

The extracted values of symmetric (\( \rho_{XX} \)) and anti-symmetric (\( \rho_{XY} \)) resistivity are fitted with the conventional multi-carrier band model in order to determine the carriers’ concentrations and lifetimes (see table 6.4). This model is designed for analysis and is based on the standard multi-band model \cite{136}, \cite{178}, \cite{179} and is extended to include field rotation. The \( i^{th} \) band model is assumed for Hall effect and magnetoresistance in silicon nanowire. The transport parameters can be derived as,

\[
\sigma_{xx}^{i} = \frac{\rho_{i}}{\left(\rho_{i}\right)^{2} + \left(R_{H}^{i}B\right)^{2}}, \quad (6.10)
\]

149
Figure 6.7: (a) and (b) Raw data extracted for the Silicon nanowire in width 500 nm at 300 K where the magnetic field swept from ±14 T. Fitted data (c) of transverse resistivity verses magnetic field of a 500 nm Si NW: raw data (red), fitted curve (blue) increases with increasing the magnetic field, the curve is not perfectly linear which shows the contribution of two carriers and (d) longitudinal resistivity versus magnetic field of a 500 nm Si NW: raw data (red), fitted curve (blue) inverse of quadratic, because of the transverse contacts offset. The model used is limited to two independent carriers.

\[
\sigma_{xy}^i = \frac{-\left(R_H^i B\right)}{\left(\rho_i\right)^2 + \left(R_H^i B\right)^2}, \tag{6.11}
\]

\[
\rho_i = \frac{m_i}{n_i \tau_i q_i^2}, \tag{6.12}
\]

\[
R_H^i = \frac{1}{q_i n_i}, \tag{6.13}
\]

\[
\mu_i = \frac{R_H^i \rho_i}{q_i}, \tag{6.14}
\]
\[ \tau_i = \frac{m_i \mu_i}{q_i} \]  

(6.15)

where, \( \sigma_{xx}^i \) is Longitudinal magneto-conductivity, \( \sigma_{xy}^i \) is Hall conductivity, \( \rho_i \) is resistivity, \( n_i \) is total carrier concentration which is always positive, \( \mu_i \) is mobility, \( \tau_i \) is relaxation time, \( m_i \) is the corresponding effective mass and \( q_i = \pm q \) with the sign (+) for electrons and (-) for holes. For these parametrisations, the effective mass of \( m_e^* = 0.98m_e \) and \( m_h^* = 0.49m_e \) [170], \( m_e \) is the mass of electron which is fixed.

The resistivity data (\( \rho_{XY} \) and \( \rho_{XX} \)) of the Si NWs are fitted in the model (see figure 6.7 and 6.8 (c & d)), from where carrier density \( n_i \) and carrier lifetime \( \tau_i \) values have been extracted and the percentage of the Hall voltage picked up by total Hall signal, are shown in table 6.4.

From the corrected data, the carrier density of single Si NWs as a function of width is obtained at room temperature (see table 6.4). A clear trend of reduction in carrier density as the width is reduced is demonstrated by the measured data on nanowires, mainly due to surface depletion. The large distribution in the data can be attributed in part to large geometrical uncertainty and the sidewall contacts, which might have been exacerbated by the varied changes of carrier concentration and scattering of reduced dimensionality.

Additionally, small offsets appear to be mainly due to the geometry of the Hall electrodes which are not precisely opposite to each other due to the nature of the shadow masking technique. It is therefore imperative to take data at both positive and negative magnetic fields and/or perform a field rotation. The exact magnitude of the Hall voltage depends crucially on the temperature and effective carrier concentration.

<table>
<thead>
<tr>
<th>Width(nm)</th>
<th>( n_M \text{ (cm}^{-3}) )</th>
<th>( \tau_M \text{ (s) } )</th>
<th>( n_m \text{ (cm}^{-3}) )</th>
<th>( \tau_m \text{ (s) } )</th>
<th>Hall signal %</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>( 2.67 \times 10^{19} )</td>
<td>( 4.067 \times 10^{-13} )</td>
<td>( 7.57 \times 10^{18} )</td>
<td>( 4.012 \times 10^{-13} )</td>
<td>5</td>
</tr>
<tr>
<td>200</td>
<td>( 8.7 \times 10^{19} )</td>
<td>( 6.5 \times 10^{-14} )</td>
<td>( 5.7 \times 10^{17} )</td>
<td>( 3.219 \times 10^{-13} )</td>
<td>50.5</td>
</tr>
<tr>
<td>150</td>
<td>( 1.4 \times 10^{19} )</td>
<td>( 1.5 \times 10^{-14} )</td>
<td>( 5.4 \times 10^{16} )</td>
<td>( 5.6 \times 10^{-13} )</td>
<td>54.5</td>
</tr>
<tr>
<td>80</td>
<td>( 5.079 \times 10^{19} )</td>
<td>( 8.2 \times 10^{-13} )</td>
<td>( 8.38 \times 10^{18} )</td>
<td>( 1.5 \times 10^{-13} )</td>
<td>7</td>
</tr>
<tr>
<td>70</td>
<td>( 9.23 \times 10^{19} )</td>
<td>( 1.25 \times 10^{-13} )</td>
<td>( 6.58 \times 10^{18} )</td>
<td>( 8.0 \times 10^{-13} )</td>
<td>67</td>
</tr>
<tr>
<td>30</td>
<td>( 7.5 \times 10^{19} )</td>
<td>( 5.6 \times 10^{-13} )</td>
<td>( 7.5 \times 10^{19} )</td>
<td>( 3.86 \times 10^{-13} )</td>
<td>6</td>
</tr>
</tbody>
</table>

Table 6.4: Summary of the carrier concentration and scattering time for electrons and holes

In a second approach, the sample is rotated under constant magnetic field of \(+14\) T (see figure 6.9). This approach has increased the efficiency of the measurement (ramping very large self-inductance superconducting magnets is a slow process - many tens of minutes), additionally, eliminating the problem of accumulated thermal drift.
A Si NW of 150 nm in width has been measured at 300 K using the second approach. The raw data which is obtained using Lock-in-Amplifier (LIA), $V_X$ in-phase components and $V_Y$ quadrature components, is shown in figure 6.10. These raw data values need to be corrected for an offset. $V_y$ is adjusted to zero by varying the phase offset. This maximizes the value of $V_x$, which provides the Hall signal of the measured data. As said before, this offset occurs due to contact capacitance and inductive pick-up by the cryostat wiring etc. This results in phase shifts to the acquired AC signals, which increase approximately linearly with frequency, and need to be corrected. By providing some value to offset $\Theta_{off}$ our goal is to reduce the contribution of the inductive and capacitance effects and obtain the maximum value of measured Hall signal data $V_x$. This has helped the regression analysis within the transport model, it has resulted in $V_y = 0$ and $V_x = R_{data} I$, the maximum value of output. $R_{data}$ is the obtained Hall signal of the measured sample, which is processed in the model and becomes independent of the errors caused due to cables, capacitance and inductive effects during measurement (more derivation details are given in Appendix B).

The model derived to fit the pre-processed rotational data is given below:

$$R_{fit} = R_1 - \left( \frac{1}{\sigma_0 + \sigma_{MR} \cos(\Theta + \theta_0)^2 + \sigma_H \cos(\Theta + \theta_0)} \right)$$  \hspace{1cm} (6.16)

where $R_1$ is the contact resistance of the sample, $\sigma_{MR}$ is Magnetoconductance, $\sigma_H$ is Hall-conductance and $\sigma_0$ is the conductivity of the sample. Also included are field-independent offsets. The nominal x-axis is the one around which the sample holder is rotated. The angle $\Theta$ is formed between the sample holder and the constant applied magnetic field. However, the sample is never perfectly aligned with sample holder and, hence, a small angular offset $\theta_0$ is taken into account.

The sample is rotated in the plane $xz$ and $\Theta$ is the sample rotation angle with respect to the constant magnetic field. Using this value of $x$ in the Mathcad model by fitting into equation 6.16 the important parameters such as Hall conductivity, $\sigma_H$, and magnetoconductance, $\sigma_{MR}$ are extracted.

The data in figure 6.11 is fitted in equation 6.16 using non-linear regression with the aid of a standard non-linear least squares regression routine and $\theta$ is the angle at which sample is rotated at constant magnetic field after removing the offsets.

Figure 6.11 shows that $R_{data}$ and $R_{fit}$, are fitted well for Si NW of 150 nm in width. The same multi-band model defined earlier for field sweep is implemented in Mathcad from which the values of resistivity, $\rho$ (equation 6.12), Hall coefficient, $R_H$ (equation 6.13), carrier concentration $n_i$, mobility, $\mu$ (equation 6.14) and relaxation time, $\tau$ (equation 6.15) are extracted for Si NWs in the range of 40 nm to 150 nm wide. The results are given in the table 6.5. Figure 6.12 shows the Hall mobility variation
of Si NW with the width, which shows a clear trend of increase in mobility as the width of nanowire is reduced.

We have considered the effective cross-sectional area for Si nanowires of width smaller than 80 nm wide. Samples of different widths 80 nm, 70 nm and 40 nm all with thickness of 45 nm, due to formation of depletion layer, changed to be 71 nm, 61 nm and 30 nm in width and 38 nm in thickness. The formation of depletion layer has been calculated based on the carrier concentration within the Si NWs (see figure 6.15). 7 nm from the bottom of the Si NW and 4-5 nm from the side wall of Si NW are assumed to be depleted.

<table>
<thead>
<tr>
<th>Width(nm)</th>
<th>ρ(Ωcm)</th>
<th>μ(cm²/Vs)</th>
<th>n(cm⁻³)</th>
<th>τ(ps)</th>
<th>RH(cm³/C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>1.097 × 10⁻³ (41.56±4.0)</td>
<td>1.368 × 10⁻⁶ (0.024±0.002)</td>
<td>0.046</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>3.034 × 10⁻³ (56.4±5.0)</td>
<td>3.64 × 10¹⁹ (0.032±0.002)</td>
<td>0.171</td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>2.655 × 10⁻⁴ (77±6.0)</td>
<td>4.129 × 10²⁰ (0.032±0.002)</td>
<td>0.012</td>
<td></td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>1.951 × 10⁻³ (209±10)</td>
<td>2.149 × 10¹⁹ (0.085±0.004)</td>
<td>0.069</td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>3.247 × 10⁻⁵ (292±6.0)</td>
<td>1.058 × 10²¹ (0.103±0.002)</td>
<td>0.00258</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6.5: Summary of the resistivity, mobility, carrier concentration and scattering time.

As mentioned above, we have performed two different types of measurement such as field sweep and sample rotation for the same sample of silicon NWs having width 150 nm, 70 nm and 80 nm. The comparison between the extracted transport parameters from the rotational measurement and the field sweep measurement shows similar values and this confirms the correctness of our approach within experimental limits.

The Hall mobility of the 40 nm wide Si NW is 292±6.0 cm²/Vs for electrons which is the highest compared to all other NWs. The film mobility is 100 cm²/Vs for electrons of Si material with the doping level of 10¹⁹ cm⁻³ [62, 164–166]. Previous reported result on Si NW of average 4 nm and doping level of 8×10¹⁹ cm⁻³ has lower Hall mobility of 70 cm²/Vs [4] and drift mobility of 109 cm²/Vs [15]. This is likely due to the geometrical uncertainty of the device [15]. Hence, to increase the accuracy of Hall measurement side wall contact to NW should be preferred.

Hall measurement on 70 nm wide Si nanowire has been performed within a second approach, where sample is rotated at constant magnetic field, the data is recorded at steps of 10 K in the entire interval from 10 to 300 K. The sample is rotated in field, at each fixed temperature value. Raw data obtained using Lock-in Amplifier (LIA), needs to be corrected for an offset. The aim is to reduce, the contribution of the inductive and capacitance effects and obtain the maximum value of measured Hall signal data Vₓ. This has helped the regression analysis within the transport model, it has resulted in Vₓ=0 and Vₓ = V_H, the maximum value of output. V_H is the obtained Hall signal of
the measured sample, which is processed in the model and became independent of the errors occurred during measurement. This is a similar approach as before for data analysis (using equation B.2, B.3 and more derivation details are given in Appendix B).

The effect of temperature on 70 nm wide Si NW has been studied by performing Hall measurement. The Hall voltage $V_H$ has been recorded and using equations 6.4 and 6.7 values of carrier concentration, $n$ ($m^{-3}$) have been extracted. Log of carrier concentration has been plotted against temperature variation which is shown in figure 6.13. A sudden dip in Hall voltage at 70 K with change in polarity can be seen from this figure 6.13 (a) which suggests activation of the impurity-dopants below 70 K. This can be attributed to complete freeze out of $n$-type (phosphorus) dopants and/or perhaps $p$-type dopants from background doping get activated below this temperature resulting in negative polarity of Hall voltage.

The donor activation energy for the nanowire <40 nm is not extractable due to high geometrical uncertainty in determining the carrier density but could also be as a result of change in transport dimension [4].

In our case, the donor activation energy calculated for sample having 70 nm wide Si NW, using equation 6.17, is $26 \pm 3.8$ meV (see figure 6.13 (b)) for temperature above 70 K. And for temperatures below 70 K, it decreases to $5.23 \pm 1.54$ meV (see figure 6.13 (c)).

$$n = \exp \left(-\frac{E_D}{2k_B T}\right)$$ (6.17)

In fact, the dopants’ activation is addressed to be prime issue in unpassivated NW, 15 nm wide, grown from bottom-up approach which has activation energy of 46 meV [180] whereas NW fabricated using top down approach, 12 nm wide, has activation energy of $10.3 \pm 0.6$ meV [4]. On comparing the donor activation energy values calculated in our case as well as observed by other investigators the dopant deactivation energy is observed to be much lower for NWs fabricated using top down approach than the ones grown using bottom-up approach. This is mainly due to the possibility of passivation of Si NW surfaces by SiO$_2$ grown and annealed intentionally or due to the presence of native oxide. SiO$_2$ results in better passivation property due to its high dielectric constant of 3.9 as compared to air of dielectric constant of 1. Further post growth annealing processes are available to yield low density of surface trapped charges at the Si/SiO$_2$ interface resulting in better passivation and lower donor deactivation energies [181]. In our case Si NWs are passivated on top by SiO$_2$ deposited through oxidation of HSQ resist as compared to thermally grown oxide by Mirza et.al [4] which is known to yield better Si/SiO$_2$ interface. Higher density of trapped charge in our case may be the reason for
slightly higher dopants’ activation energy.

The Si device layer used in this study is heavily phosphorous doped having the activation energy of $E_D=45$ meV [62]. Using the equation 6.17 at room temperature having thermal energy of 25 meV suggests that only 40% of dopants are activated, other 60% are neutral, majority of dopants are neutral which affects the transport by absorbing energy and producing heat. Thus, the neutral scattering is dominating compared to other scattering. The scattering mechanisms which are limiting the mobility of these Si NWs are determined from the direct comparison of experimental Hall measurement with a number of differently theoretically calculated values. The comparison of our data on Hall signals with reported theoretically calculated values seems to suggest that neutral impurity scattering dominates which limits the mobility in Si NW fabricated using top down approach [4]. The interface roughness scattering is found to be insignificant as compared to the neutral impurity scattering and other scattering mechanisms [4]. Similar results are obtained for heavily doped Si measured at low temperature, neutral impurity scattering found dominating above 30 K and probably ionized impurity scattering below 30 K [182].

Mirza et al [4] found that Si NW <30 nm in width, with doping density $2 \times 10^{19}$ cm$^{-3}$ has poor or no conductivity due to Schottky barrier at the source/drain end of the channel or device has a Coulomb gap. The SOI substrate used in this study is non uniformly doped throughout the thickness of the device layer from $5 \times 10^{18}$ cm$^{-3}$ at BOX to $7 \times 10^{19}$ cm$^{-3}$ at surface. For Hall electrode fabrication angled deposition technique is used and its details are given in section 4.4.

As we go down on the nanoscale to sub-30 nm the IV characteristics shows poor conductivity, see figure 6.14. This increase in resistance could be due to large depletion width formed between metal and semiconductor interface. Depletion region can be calculated using Poissons equation, based on assumptions that there are no free carriers within this region, this equation is useful for finding the electric potential distribution when the charge density is known. Due to the formation of junction at the interface there will be an electric field generated under equilibrium conditions and contact potential is created. The depletion width, $x_d$ under equilibrium condition can be written as equation 6.18,

$$x_d = \sqrt{\frac{2\varepsilon_0\varepsilon_s\phi_b}{qN_D}}$$  \hspace{1cm} (6.18)

where, $\varepsilon_0$ is electric constant also known as vacuum permittivity, $\varepsilon_s$ is the dielectric constant and its value is 11.9 for Si, this is also known as relative permittivity, $\phi_b$ is the barrier height and $N_D$ is the carrier concentration of Si material.
From the equation 6.18, it is clear that depletion width is dependent on carrier concentration of the sample. Yonatan Calahorra et al [43] have observed that exponential doping profile has a significant effect on NW electrostatics which can effect the NW contact and transport properties. Also Muhammad M. Mirza et al [4] have predicted that the depletion formation in Si NWs varies with the doping density of material. It showed the depletion formation of $\sim$30 nm at doping density of $2 \times 10^{19}$ cm$^{-3}$ for Si NW width $<$30 nm, resulted in poor or no conduction. On increasing the doping density to $4 \times 10^{19}$ cm$^{-3}$ the Si NW width $<$7 nm, results in linear conduction due to quasi-ballistic transport.

There is definite trend of increase in mobility with decreasing NWs' width which is consistent with other reported results [4]. Mirza et al [4] have reported increase in mobility for Si NWs having width below 12 nm with doping concentration of $8 \times 10^{19}$ cm$^{-3}$. Above this width, bulk like behavior with three dimensional carrier flow is predicted. In our case even Si nanowires with width around 40 nm and doping level $5 \times 10^{19}$ cm$^{-3}$ show increasing trend in mobility. This is due to reduced dimensionality of electron transport in nanowires, caused by depletion effect [43]. The depletion region formation results in reduced effective physical width of nanowires. Our device layer has non-uniform dopant distribution profile, which is approximately one order of magnitude lower at the bottom of NWs. Given this situation, the depletion width along the height of Si NWs has changed depending on the position of the side wall contact. A theoretical calculation using the equation 6.18 has been done, the graph for depletion width with respect to the doping concentration of Si NWs has been shown in figure 6.15 [183]. A full depletion is developed due to the width of the NWs $<$30 nm, which is very narrow and hence there is very little charge available for transport. Since our device layer have non uniform doping distribution, the formation of depletion width also might have varied accordingly.
Figure 6.8: (a) and (b) Raw data extracted for the Silicon nanowire of width 30 nm at 300 K where the magnetic field swept from ±14 T. Fitted data of a 30 nm Si NW: raw data (red), fitted curve (blue) (c) of transverse resistivity versus magnetic field, which is linearly dependent indicating a single type of charge carrier and (d) longitudinal resistivity versus magnetic field, which is quadratic as expected.
Figure 6.9: Schematic diagram of the measurement set up where sample is rotated with respect to the constant magnetic field.

Figure 6.10: Raw data of 150 nm Si NW at 300 K extracted from rotation in constant magnetic field.
Figure 6.11: Fitted data of 150 nm Si NW: raw data (red), fitted curve (blue). This data is the phase corrected version of figure 6.10.

Figure 6.12: Hall mobility variation with the width of Si Nanowire, trend shows the increase in values of mobility. This graph has been plotted from the values extracted from the table 6.5.
Figure 6.13: (a) log carrier concentration (m$^{-3}$) vs temperature for nanowire of 70 nm width. (b) log of carrier concentration (m$^{-3}$) vs inverse of temperature (1/K) which is showing extracted dopant activation energy for 70 nm width nanowires above 70 K. (c) log of carrier concentration (m$^{-3}$) vs inverse of temperature (1/K) which is showing extracted dopant activation energy for 70 nm width nanowires below 70 K.
Figure 6.14: IV characteristics of Si nanowire width 30 nm, thickness is 45 nm, the metal deposited is Ti/Au 70 nm, the applied current ± 100nA.

Figure 6.15: Dependence between doping density and depletion width formation. To achieve high conduction, and eliminate the contact problems in ultra-thin NWs, it is necessary to dope them to quite degenerate carrier concentrations, \(8 \times 10^{19} \text{ cm}^{-3}\) at least [4].
6.5 Discussion

The results presented above clearly indicate broad agreement within measurement errors between the electrical parameters measured for the Si film, bar and nanowires which have large dimensions’ suggesting bulk like behavior. Some scatter in the data for nanowires (table 6.5) could be seen which is mainly due to the inherent limitation of uncertainty in the NW geometry and side wall contact formation using the shadow mask process used in this investigation. Relying on measured data obtained from different widths of nanowires from 500 nm to 30 nm, there is a definite trend of increase in mobility with decreasing NWs’ width, which is consistent with other reported results [4]. Mirza et al [4] have reported an increase in mobility for Si NWs having widths below 12 nm with a doping concentration of $8 \times 10^{19}$ cm$^{-3}$. Above this width, bulk like behavior with three dimensional carrier flow is predicted. In our case even Si nanowires with widths around 40 nm and doping level of $5 \times 10^{19}$ cm$^{-3}$ show increase in mobility. This is due to confinement of electron transport in nanowires, caused by the depletion effect [43]. The depletion region formation results in a reduced effective physical width of nanowires. Our device layer has a non-uniform dopant distribution profile, which is approximately one order of magnitude lower at the bottom of NWs. Given this situation, the depletion width along the height of Si NWs changes depending on the position of the side wall contact. A full depletion is developed due to the width of the NWs <30 nm, which is very narrow and hence there is very little charge available for transport. Since our device layer has a non-uniform doping distribution, the formation of the depletion width also varied accordingly.

For validation of our measurement data, figure 6.16 shows mobility vs NW width obtained using both the approaches i.e. four-point and Hall effect measurement. Very good agreement between both measured data could be seen from the figure 6.16. Also, some scatter in mobility data measured could be seen. This could be due to the change in the dimensionality of nanowires into quasi-1D, which reduces the effect of scattering and hence increases the mobility.
6.6 Conclusions

Hall measurements are performed on single Si NWs having widths in the range from 30 nm to 500 nm fabricated using a top down approach. A heavily non-uniformly doped sample is used for this study. Due to high noise-to-signal ratio AC measurements are carried out using two approaches, 1) Magnetic field sweeping in the range of ±14 T and 2) Sample rotation under a constant magnetic field of +14 T. The second approach, has increased the efficiency of the measurement (ramping very large self-inductance superconducting magnets is a slow process - many tens of minutes), additionally, eliminating the problem of accumulated thermal drift. The Hall contacts are made at the side wall of the NW resulting in the Hall electrodes not being precisely opposite to each other. Thus, Hall voltage signal is extracted from longitudinally offset electrodes.

Nanowire widths <30 nm have resulted in poor conductivity due to the formation of a depletion region larger than the width of nanowire, because of the non-uniform doping density. The mobility values varied from 292±6.0 cm²/Vs for 40 nm wide Si nanowires to 41.56±4.0 cm²/Vs for 150 nm wide Silicon nanowires at room temperature. The effect of silicon nanowire width on transport properties clearly demonstrates increase in mobility as the width of nanowire is reduced. The use of high
magnetic field of 14 T has played a major role in suppressing the surface scattering by creating a diffusive localization of electrons in Si NWs and this effect observed in 40 nm by 45 nm dimension. The carrier density is observed to be in the range of \(5.4 \times 10^{16}\) to \(9.23 \times 10^{19}\) cm\(^{-3}\). The uncertainties of the values obtained for the carrier concentration and Hall mobility are due to the depletion effect which is observed to be significantly reduced for broader Silicon nanowires. This leads to ideal I-V characteristics when the contacts are on the top part of the side walls of nanowire which have the higher doping level.

On varying the temperature from 300 K to 10 K the measurement for the 70 nm wide Si NW is performed using the second option of the Hall effect measurement, all other samples have deteriorated during the measurement. From this sample it shows that the donor deactivation takes place at 70 K and the dominant scattering is neutral impurity scattering compared to any other scattering mechanisms.

Hall effect measurements on Si NW are compared with the data obtained for the device layer using Hall bar structures having different dimensions at room temperature and at low temperature, 10 K. The observed values show the increase in mobility on reducing the width of the bar. For a Si film we calculated the mobility to be 100±0.1 cm\(^2\)/Vs, for the Hall bar dimensions of 60\(\mu\)m × 20\(\mu\)m it is observed to be 183 cm\(^2\)/Vs and for 60\(\mu\)m × 10\(\mu\)m is 214.2 cm\(^2\)/Vs. At 10 K, for the Hall bar dimensions of 60\(\mu\)m ×20\(\mu\)m, mobility is observed to be 270 cm\(^2\)/Vs and for 60\(\mu\)m by 10\(\mu\)m is 300 cm\(^2\)/Vs. These results suggest that reducing the dimension can result in better transport of carriers.
Chapter 7

Conclusion & Outlook

7.1 Conclusions and Future Work

In this thesis, the results of an investigation into the optimization of top-down fabrication processes and the transport properties of Si NWs have been presented. Although NWs with diameters as small as < 1 nm can be grown on many substrates with high aspect ratio using bottom up approach, it has serious limitations related to lower yield to be economical for mass manufacturing. In addition, there are other problems such as mechanically transfer of NWs to the substrates, positioning of individual NW and formation of Ohmic contacts associated with this process. In view of this, a top down approach of using Electron Beam Lithography and ICP RIE etching has been used here to fabricate Si NWs.

The optimization of all the three important processes EBL, ICP RIE dry etch and passivation layer using HSQ has been carried out. The dependence of negative tone HSQ resist thickness, exposure electron dose, concentration and developing time for nm patterning of resists has been established and an optimized set of conditions for patterning are presented. Etching of nanometric structures with vertical and damage-free sidewalls involved the optimization of gas chemistry, chamber pressure, RF power and bias voltage in order to achieve nanowires having widths in the range of 30 to 500 nm are discussed in Chapter 4. An alternative approach for forming side-wall contacts and its effect on transport behavior has also been investigated. The etched patterns have been used as a shadow masks for the side wall contacts’ formation. Side-wall contacts are shown to minimize the geometrical uncertainties in Hall measurement on Si NWs.

Further, using the above optimized processes for EBL, dry etching, passivation and side wall
contacts, Si NWs devices with different widths have been fabricated on Silicon On Insulator (SOI) substrates having phosphorus non-uniformly doped 45 nm thick Si as the device layer. Also, electrical measurements are carried out on blanket film and µm-structured samples of the same substrate for an explicit validation. Comparison of theoretically calculated characteristic lengths i.e. mean free path for different dimensions of transport with physical widths and it has predicted 3D transport for NWs having widths above 30 nm.

It has been observed that the sidewall contacts are easy to fabricate for nanowires with a large width to thickness ratio. Once the nanowire size is less than 50 nm, which is the thickness of the nanowire, the side contact fabrication of the electrode becomes difficult because the NW are used as a shadow mask for the contact electrode fabrication.

Measuring extremely small Hall voltages of the order of µV has been a challenge. Both DC and AC Hall effect measurements are performed to extract the carrier density and mobility. The Hall voltage is required to be measured accurately, which relies on the width of voltage probes rather than the width of the channel. Hall bar devices have been fabricated with 200 nm voltage probes for all NW width to reduce the access resistance and prevent any electron heating.

The substrate used in this work, is non-uniformly doped as verified by Secondary Ion Mass Spectroscopy with the device layer doping in the range of $8 \times 10^{18}$ cm$^{-3}$ at BOX to $5 \times 10^{19}$ cm$^{-3}$ at surface for Hall measurement. Non-ideal I-V characteristics have been observed in the samples with contacts on the bottom side of NWs (doping level of around $8 \times 10^{18}$ cm$^{-3}$), indicating the formation of a thick depletion layer in the devices. Whereas, for Si NWs having contacts on the top of the side walls of NWs, where the doping level is $5 \times 10^{19}$ cm$^{-3}$, the depletion effect is observed to be significantly reduced. This has also resulted in the uncertainty of the values obtained for carrier concentration and Hall mobility. In addition to that, the Hall electrodes are not opposite to each other, therefore, the longitudinal resistance pick-up had to be taken into account to extract the Hall signal of the NW. The other problem is the ratio of the Hall electrode width to width of the nanowire. The substrates used in this study have a Si device layer of low mobility of 100 cm$^2$/Vs which is close to the reported literature.

The DC Hall measurement of low mobility samples can result in a poor signal to noise ratio [44, 45] and suffer from other additional problems [46, 47]. It has been known that the use of AC current sourcing is able to reduce these problems and has the ability to measure the low mobility samples with greater resolution and it eliminates, the slow thermal effects including reduction in Joule heating effects. The AC Hall effect measurement are used to determine the transport parameter of Si NWs of different with from 30 nm to 500 nm and to perform that two distinct approaches have been employed.
such as magnetic field sweep in the range of ±14 T and sample rotation under constant magnetic field at +14 T. The comparison of the extracted transport parameters shows close correlation between both these measurement methods indicating the correctness of both approaches within experimental errors.

The use of external high magnetic field helps to reduce the surface scattering by diffusively localizing the electrons in the Si channel during the measurement. Here, the dimension of Si NW 40 nm in width and 45 nm in thickness has shown the increase in Hall mobility to 292±6.0 cm²/Vs at 300 K.

The temperature dependence of experimental Hall mobility is measured and compared with theoretically calculated values to determine the dominant scattering mechanism. The scattering mechanism limited the mobility in those NWs where neutral impurity scattering is observed to dominate, as compared to scattering due to roughness or surface defects. The effective carrier density is observed to reduce whereas mobility increased as the width of NW is decreased because of the increased influence of surface depletion effect. Moreover, the geometrical uncertainty in measuring the effective carrier density increased as the width of NW is reduced.

There are few issues, which we came across during the measurements on NWs, which need to be overcome in future. The most important issue is our inability to design the Hall electrode exactly opposite to each other which has led to high errors in measurement and essentially the Hall voltage value which we extracted is from the longitudinal electrodes.

The SOI substrate used in this study is non-uniformly doped and so it is difficult to quantitatively compare the carrier density extracted from Hall measurement. For Hall measurement at nanoscale devices, the device layer should be uniformly and highly doped at least \( \gg 8 \times 10^{19} \text{ cm}^{-3} \) otherwise it would result in non-ideal Ohmic contact and would be challenging to extract the Hall voltages [4]. Alternative method can be adopted to form metal silicide by annealing the sample at high temperature. Annealing can also overcome lots of defects which occur during doping the crystal structure of silicon and during the use of dry plasma etching [4]. For the device fabrication it is required to fabricate the Hall electrode width as small as possible to increase the accuracy of the Hall measurement. For high accuracy, it is important to design the devices to make the contacts as point-like as possible to minimize shunting.

The effect of silicon nanowire width on transport properties clearly demonstrates the increase in mobility as the width of nanowire is reduced. The uncertainties of the values obtained for carrier concentration and Hall mobility are due to the depletion effect which is observed to be significantly reduced for broader Silicon nanowires. This leads to close-to-ideal IV characteristics, having contacts on the top of the side walls of the nanowires, which have the higher doping level. Si NWs of width <30
nm exhibit poor conductivity due to the formation of depletion region larger than the width of the nanowires, because of the non-uniform doping density. Overall, a methodology has been developed for Hall measurements of non-uniformly and non-degenerately-doped SOI top-down NWs, which is applicable down to lateral sizes below 40 nm. As an example, consistent mobility values of $292\pm6.0$ cm$^2$/Vs for 40 nm wide Silicon nanowire and 41 cm$^2$/Vs for 150 nm wide Silicon nanowires, are extracted at room temperature. It is believed that with only minor modifications, the methodology developed here, can be applied for the direct characterization of III-V and II-VI semiconductor NWs, in the near future, opening a route to an efficient down selection of materials and processes for NW device fabrication in the beyond-CMOS world.
List of Publications and Conference Contributions


2. **Publication**- Akshara Verma, Stephen Connaughton and Plamen Stamenov, “Multiple contacts investigation of single silicon nanowires with the active voltage contrast scanning electron microscopy technique”; *Meas. Sci. Technol.* 30, 017002 (2019);


4. **Poster**- “Top-down fabrication and definition of side contacts of InAs nanowires” in ISCP Nanotechnology Conference, Dublin, May, 2014.

5. **Talk**- “Top-down fabrication of nanowires and definition of side-contacts on SOI” EMRS, Warsaw, Poland, September, 2014.


Bibliography


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[78] N. Mott, “Note on the contact between a metal and an insulator or semiconductor,” p. 56X, 1938.


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Appendices
Appendix A

Carrier Transport Measurement Using Field Sweep

The detailed description of the model used for the calculation in chapter 6 of Carrier transport parameter for field scan is given in this appendix A. The data extracted from the lock in amplifier are in X and Y components. These two outputs of lock in amplifier are termed as the in-phase and quadrature components with respect to the input signal. The amplitude R and the phase Θ are easily derived from X and Y by a transformation from Cartesian coordinates into polar coordinates using the relation as shown in equation A.1. Y component extracted from the lock-in amplifier is adjusted to zero by giving appropriate value to Θ_{off}, the Cartesian coordinates expressed in complex number as (X_1, Y_1) are shown in equation A.2.

\[ R = |X + iY|, \]
\[ \Theta = \text{arg}(X + iY) \]  
\[ (A.1) \]
\[ X_1 = R \cos(\Theta - \Theta_{off}), \]
\[ Y_1 = R \sin(\Theta - \Theta_{off}) \]  
\[ (A.2) \]

Our aim is to get symmetric and anti-symmetric values of resistance data, R_{xx} and R_{xy}. So in order to achieve this, the first function was used given in equation A.3. Using the csort function in mathcad returns an array formed by rearranging rows of M until column-0 is in ascending order.
\[ M = \text{augment}(H, X_1) \]
\[ SM = \text{csort}(M, 0) \]  \hspace{1cm} (A.3)

Now using \textit{vlookup} function in equation A.4 arrange the variable \( SM \) which contains the information of field and data. So it first looks in the first column of the matrix, \( SM \), for a given value, \( H \), where, \( H \) is the magnetic field sweep, \( H_{\text{min}} = -13.99 \, \text{T} \) and \( H_{\text{max}} = 13.99 \, \text{T} \) and returns the value(s) in the same row(s) in the column specified, as column-0 and column-1.

\[
CSM = \text{augment}[\text{vlookup}[H_{\text{min}}, SM, 0, "range"], \text{vlookup}[H_{\text{max}}, SM, 1, "range"]] \]  \hspace{1cm} (A.4)

\[ vs = \text{Spline2}(CSM^{<0>}, CSM^{<1>}, n^*) \]  \hspace{1cm} (A.5)

\[ sx(x) = (\text{Binterp}(x, vs)^T)^{<0>} \]  \hspace{1cm} (A.6)

For proper data analysis, the most commonly used function for interpolation is \textit{Spline2} which returns the optimal set of order \( n^* \) B-spline knots to interpolate on data \( CSM^{<0>} \) and \( CSM^{<1>} \). The vector returned becomes the second argument of \text{Binterp} which is \( vs \) here. Now, in equation A.5 the \text{Spline2} function used an integer \( n^* \) equal to 1, 2, or 3, indicating the degree of the individual quadratic \( (n^* = 2) \) and cubic \( (n^* = 3) \) polynomial-fits used in the B-spline.

Equation A.6 is \text{Binterp} function which returns a B-spline interpolated \( CSM^{<0>} \) value corresponding to \( CSM^{<1>} \) using the output vector, \( vs \), of the \text{Spline2} function, along with the first, second, and third derivatives. Here \( x \) is the value of the independent variable at which we evaluate the interpolation curve. For best results, \( x \) should be in the range encompassed by the values of \( CSM^{<0>} \).

\[
n = 1000 \quad i = 0 \ldots n-1
\]

\[ h_i = H_{\text{min}} + (H_{\text{max}} - H_{\text{min}}) \frac{i}{n - 1} \]  \hspace{1cm} (A.7)

\[ osh_i = H_{\text{max}} \frac{i}{n - 1} \]  \hspace{1cm} (A.8)

\[ sx = SX(h) \]  \hspace{1cm} (A.9)
\[ \text{symx} = 0.5(sx(osh) + sx(-osh)) \]  
(A.10)

\[ \text{asymx} = 0.5(sx(osh) - sx(-osh)) \]  
(A.11)

Exported the symmetric \( \text{symx} \) and anti-symmetric \( \text{asymx} \) data from equations A.10, A.11 as augment function which was later used to fit in the data in the model to extract the information of carrier concentration.

These values are still in rms form so by using current 20 nA and the given gain-value \( G \) from low noise amplifier which varies from sample to sample for measurement. The data is modified to resistance, \( R_{xy} \) and \( R_{xx} \) given in equation A.13, A.14.

\[ SH = \text{Data} \]  
(A.12)

\[ SR_{XY} = \frac{\text{Data}}{IG} \cdot \sqrt{2} \]  
(A.13)

\[ SR_{XX} = \frac{\text{Data}}{IG} \cdot \sqrt{2} \]  
(A.14)

\[ \sigma(B, m, n, \tau) = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} \\ -\sigma_{xy} & \sigma_{xx} \end{pmatrix} \]  
(A.15)

1. \( B \) is the magnetic field from 0 to 14 T,
2. \( m \) is the effective mass of the carriers,
3. \( n \) is the carrier concentration and
4. \( \tau \) is the carrier life time.

Using the equation A.15, Conductivity tensors corresponding to the individual carrier types can be written as matrix or 2-D array.

\[ i=0 \text{ to } N-1 \text{ here } N=2, \]

\[ S(B) = \Sigma_i \sigma(B, m_i, n_i, \tau_i) \]  
(A.16)

\[ Q(B) = S(B)^{-1} \]  
(A.17)
Equation A.17 contains the value of resistivity.

Now defining the fit function for the model lets say

$$\text{Fit}(x,p)= y \leftarrow x \text{ if } x > 0$$

(-x) otherwise

for $i \in 0 ... N-1$

$$f_i \leftarrow p_i (100 \text{ cm}^{-3})$$

$$g_i \leftarrow p_{(i+N)\text{.8}}$$

$$S \leftarrow \sum_{i=0}^{N-1} \sigma(y,T,m_i,f_i,g_i)$$

$$Q \leftarrow S^{-1}$$

$$r \leftarrow Q_{0,0} \text{ if } x>0$$

$$Q_{0,1} \eta \text{ otherwise}$$

$$\eta = 10^9$$

$$Q(0,T) = \begin{pmatrix} \rho_{xx} & 0 \\ 0 & \rho_{xx} \end{pmatrix}$$  \hspace{1cm} (A.18)

Using the fit functions equation A.18 has the sample resistivity in $\Omega \cdot \text{cm}$.

skip=1, j=0..rows(SH)-1-skip

$$H_j = SH_{j+\text{skip}}$$

$$MR_j = (SR_{xx,j} + \text{skip}) \frac{w\cdot l}{t}$$  \hspace{1cm} (A.19)

$$MH_j = (SR_{xy,j} + \text{skip})t$$  \hspace{1cm} (A.20)

Equation A.19 and A.20 contain the resistivity data, $w$ is the width of the nanowire, $t$ is the thickness and $l$ is the inner contacts distance between the electrodes. $MR_j$ symmetric and $MH_j$ antisymmetric contain the data of resistivity.

$$vx = \text{stack}(H,-H)$$  \hspace{1cm} (A.21)
In equations A.21 to A.23 stack function is used to return an array formed by placing them in stack order. *Genfit* function is designed to model the data by some arbitrary (possibly nonlinear) function *Fit* whose parameters must be chosen. Let’s say *r* has the value of the best approximate of the data in *vx* and *vy*. *vg* contains the value for carrier concentration and carrier life time. Basically its the guess values for the best fit. By using the above value the data is fitted well to *FRj* and *FHj* symmetric and asymmetric fit and also able to find the ratio of the Hall voltage signal is extracted.

Using the formula for mobility and Hall coefficient given in equations below, the Hall mobility for majority and minority carriers can be calculated.

\[
\mu = \frac{1}{q.p.n} \tag{A.27}
\]

\[
R_H = \frac{1}{q.n} \tag{A.28}
\]
Appendix B

Carrier Transport Measurement Using Sample Rotation

The equations used to fit the raw data are given below:

\[ R_{fit} = \frac{-1}{\sigma_0 + \sigma_{MR} \cos(x + \theta_0)^2 + \sigma_H \cos(x + \theta_0)} + R_1 \]  
\[ (B.1) \]

\[ R = |X + iY|, \]
\[ \Theta = \text{arg}(X + iY) \]  
\[ (B.2) \]

\[ X_1 = (R \cos(\Theta - \Theta_{off})), \]
\[ Y_1 = (R \sin(\Theta - \Theta_{off})) \]  
\[ (B.3) \]

where \( R_1 \) is the contact resistance of the sample and \( \sigma_0 \) is the conductivity field-independent offsets. \( x \) is the axis on which the sample holder is rotated. The angle \( \theta \) is formed between the sample holder and the constant applied magnetic field. However, the sample is never perfectly aligned with sample holder and, hence, a small angular offset \( \theta_0 \) is taken into account. \( \Theta \) is the argument given by the phase of the input signal relative to the reference signal. \( \Theta_{off} \), offset occurs due to cable and sample mounting spurious capacitance, causing phase shifts to the acquired AC signals, which increase approximately linearly with frequency, and which need to be corrected. \( X \) and \( Y \) are the two outputs of lock-in amplifier termed the in phase and quadrature components with respect to the input signal. The amplitude \( R \) and the phase \( \Theta \) are easily derived from \( X \) and \( Y \) by a transformation.
from Cartesian coordinates into polar coordinates using the relation as shown in equation B.2. The
sample is rotated in one plane XY, so the Cartesian coordinates are in Cartesian plane and expressed
in complex number as \((X_1, Y_1)\) in equation B.3.

\(X_1\) is the real part of the output signal obtained from the lock in amplifier. \(Y_1\) is the imaginary
part of the output signal obtained from the lock in amplifier.

This equation is used to obtain the maximum output from \(X_1\) and the contribution of the inductive
and capacitance present in the circuit obtained in \(Y_1\). However, this contribution will never be ideally
zero so there will be some offset \(\Theta_{\text{off}}\). By providing some value to \(\Theta_{\text{off}}\) our goal is to reduce this effect
and obtain the maximum resistance \(R\).

Important parameters are the Hall conductivity, \(\sigma_H\), and the magnetoconductance, \(\sigma_{\text{MR}}\). The later
parameters are extracted from the angular rotation scan \(R(\theta)\) because they have different symmetry.

By using the \textit{genfit} functions the data extracted is fitted into the above equation B.1. Above
parameter mentioned in equation B.1 was initially a guess value which is later mentioned in \(v_g\) which
is a vector of guess values.

\[
v_g = \begin{pmatrix}
\sigma_0 \\
R_1 \\
\sigma_{\text{MR}} \\
\sigma_H \\
0
\end{pmatrix}
\]  
\text{(B.4)}

\[
V_r = \text{genfit}(\theta, X_1, v_g, R_{\text{fit}})
\]  
\text{(B.5)}

\textit{Genfit} function is designed to model the data by some arbitrary (possibly nonlinear) function \(R_{\text{fit}}\)
whose parameters must be chosen. The parameter given in the equation B.1, B.2, B.3 and B.4 are
defined in \(V_r\) after using the \textit{genfit} functions the best fitted value of the data is given in equation B.5.

\[
V_r = \begin{pmatrix}
V_r0 \\
V_r1 \\
V_r2 \\
V_r3 \\
V_r4
\end{pmatrix}
\]  
\text{(B.6)}

Equation B.6 provides us the value of the parameter used in the equations from B.8 to B.13. I is
the applied current in sine wave form

\[ I_s = I_p \sin(2\pi ft + \Phi) \] (B.7)

where \( I_p \) is 20 nA, \( \Phi \) is zero, \( f \) is the frequency at which input signal waveform is applied and synchronized with the Hall signal \( X_1 \) at the lock in amplifier. \( G \) is the Gain which is used to increase the value of the Hall signal displayed at the lock-in amplifier as \( X_1 \). The value of Hall signal is given in the form of root mean square and \( V_{rms} = V/\sqrt{2} \) is used to extract the amplitude of the Hall signal.

\[ R_0 = \frac{V_{rms}}{V_{r0} \cdot I \cdot G} \] (B.8)

The above equation B.8 provides us the resistance offset value.

\[ R_1 = \frac{V \cdot r_1 \cdot V_{rms}}{I \cdot G} , \] (B.9)

\[ \rho_{approx} = \frac{R_1 \cdot w \cdot l}{l} \] (B.10)

The above equation B.9 provides us the contact resistance of the sample and \( \rho_{approx} \) is the contact resistivity of the sample.

\[ \Delta \sigma_{xx} = \frac{v r_2 \cdot l \cdot I \cdot G}{V_{rms} \cdot w \cdot l} \] (B.11)

\[ \Delta \sigma_{xy} = \frac{v r_3 \cdot l \cdot I \cdot G}{V_{rms} \cdot w \cdot l} \] (B.12)

where \( \Delta \sigma_{xx} \) is the longitudinal conductivity and \( \Delta \sigma_{xy} \) is the Hall conductivity.

\[ \theta = v \cdot r_4 \] (B.13)

As said before \( \theta \) is the angle of rotation of the sample with respect to the constant magnetic field.

\[ \sigma_{xx} = \frac{\rho}{\rho^2 + (R_{H} \cdot B)^2} \] (B.14)

\[ \sigma_{xy} = \frac{R_{H} \cdot B}{\rho^2 + (R_{H} \cdot B)^2} \] (B.15)
\[ \rho = \frac{m^*}{|n|, q^2 \tau} \] \hspace{1cm} \text{(B.16)}

\[ R_H = -\frac{1}{q.n} \] \hspace{1cm} \text{(B.17)}

\[ \mu = \frac{1}{q.p.n} \] \hspace{1cm} \text{(B.18)}