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Quantum point contacts and resistive switching in Ni/NiO nanowire junctions

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Metal oxide devices that exhibit resistive switching are leading candidates for non-volatile memory applications due to their potential for fast switching, low-power operation, and high device density. It is widely accepted in many systems that two-state resistive behavior arises from the formation and rupture of conductive filaments spanning the oxide layer. However, means for controlling the filament geometry, which critically influences conduction, have largely been unexamined. Here, we explore the connection between filament geometry and conductance in a model resistive switching system based on the junction of two nickel/nickel oxide core/shell nanowires. Variable temperature current-voltage measurements indicate that either wide metallic filaments or narrow semiconducting filaments can be preferentially formed by varying the current compliance during electroformation. Metallic filaments behave as a conventional metallic resistance in series with a small barrier, while semiconducting filaments behave as quantum point contacts. The ability to tune filament geometry and behavior through the electroforming process may open avenues for enhanced functionality in nanoscale memristive systems. *Published by AIP Publishing.* [<http://dx.doi.org/10.1063/1.4967502>]

Materials that exhibit electrically induced resistive switching are naturally suited for robust and low-power non-volatile memory, where a bit is encoded in either a low (LRS) or high resistance state (HRS) and read out non-destructively.¹ Many implementations of this concept are based on a thin-film dielectric sandwiched between metal contacts. After an initial electroforming process, application of an electric field switches the device's electrical conductivity between a LRS and a HRS. Devices based on transition metal oxides, such as NiO_x,²⁻⁴ TiO_x,^{4,5} HfO_x,⁶ Ta₂O₅,^{5,7,8} and SiO_x,^{9,10} have all demonstrated resistive switching with some devices exhibiting resistance ratios and cycling endurance sufficient for many computational memory applications.^{9,11-16}

Resistive switching in oxide-based systems is thought to arise from the rupture and reformation of nanoscale conducting filaments that span the oxide.^{1,4,13,17-19} A fully formed, intact filament yields the conductive LRS, while a ruptured filament leads to the HRS. These filaments are composed of a chain of oxygen vacancies, with rupture and reformation induced by either electric field- or Joule-heating-induced vacancy migration.^{1,4,20-23} Initial formation of the conductive filament from the pristine oxide requires application of a large electric field that triggers a soft breakdown of the dielectric.^{4,21,24,25} Typically, filamentary conduction is viewed as an all-or-nothing response, where either metallic

(LRS) or insulating (HRS) behavior occurs. While sufficient for basic memory applications, the ability to achieve electronic states beyond these two regimes is desirable both for fundamental investigations of filamentary conduction, as well as device applications.

In this work, we demonstrate a semiconducting LRS, in addition to the typically observed metallic LRS and insulating HRS, by varying the electroformation process in a model resistive switching system based on the junction between two Ni/NiO core/shell nanowires.^{12,21,26,27} While prior studies have explored the impact of electroformation on device performance,^{4,23,28,29} in this work, we present a comprehensive examination of the temperature-dependent electrical characteristics arising from different formation procedures. Based on current-voltage (IV) and temperature-dependent resistance (R(T)) data, the metallic LRS behaves as a conventional metallic resistance in series with a small barrier, while the semiconducting LRS behaves as an atomically thin quantum point contact (QPC).³⁰⁻³⁵ QPC conduction has been previously observed in HfO₂ devices,^{34,36} but has not been documented in NiO systems. These observations suggest that the metallic (semiconducting) LRS derives from wide (narrow) filament constrictions that are preferentially achieved by executing either a single- or multi-step electroformation process. Tuning the filament geometry, and thus the conduction characteristics, therefore introduces an additional variable for functionality in nanoscale memristive devices.

Ni nanowires ~35 nm in diameter and ~10 to 20 μm in length were purchased from a commercial supplier (Nanomaterials.it), drop-cast onto Si/SiO₂ substrates, and

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oriented by a magnetic field. A second drop-cast was performed in an orthogonal field angle, resulting in crossed nanowire junctions. Scanning electron microscope (SEM) images of a device are shown in the inset of Figure 1(a). The NiO layer is self-limited and ~ 4 to 8 nm thick, yielding ~ 8 to 16 nm separation between conducting Ni cores. Electrodes were then patterned via electron beam lithography, with 5 nm of Ti and 150 nm of Au deposited using electron beam evaporation. Devices were loaded into a Lake Shore CRX-VF cryogenic probe station for temperature-dependent electrical characterization. All measurements were performed in vacuum using a Keithley 4200-SCS Parameter Analyzer and were taken at temperatures from 15 to 300 K, with 10 consecutive scans averaged at each temperature.

To achieve varying LRSs of the nanowire junctions, two electroformation procedures were performed at 300 K in vacuum by applying a voltage sweep with different current compliances (I_{CC}). We note that filament formation can occur at the Au-NiO interface as well as the nanowire junction and that, in principle, there is potentially confusion regarding the location of the filament dominating conduction.^{26,27} However, the contact area at the nanowire junction is reduced due to the junction geometry as well as the surface roughness of the nanowires (Figure S1 of [supplementary material](#)) when compared to the Au-NiO interface, while the oxide is twice as thick at the junction. These structural properties imply that filaments will be the last to form in the junction and that these filaments will dominate transport characteristics. This was confirmed by comparing two- vs four-terminal devices (where the contacts with the leads can be formed independently) and no observable difference was found. The first formation procedure (Figure 1(a)) used a dual sweep with $I_{CC} = 10 \mu\text{A}$ in voltage steps of 0.025 V (black trace). The dramatic reduction in resistance at ~ 5.1 V indicates filament formation, resulting in a “metallic” LRS based on the low resistance ($4.79 \text{ k} \Omega$ at 0.8 V at 300 K), the linear IV relation at room temperature (Figure 3(a)), and positive temperature coefficient of resistance (TCR). Figure 1(b) shows the second electroformation procedure where four formation sweeps were performed,

starting with $I_{CC} = 0.1 \mu\text{A}$, and increasing by one order of magnitude in subsequent sweeps to end with $I_{CC} = 100 \mu\text{A}$. The resulting filament exhibits a “semiconducting” LRS, characterized by non-linear IVs, higher resistance ($179 \text{ k} \Omega$ at 0.8 V at 300 K), and negative TCR. Subsequent RESET (switching from LRS to HRS) and SET (switching from HRS to LRS) operations occurred at positive bias (unipolar switching), and were reproducible over at least 10 cycles, as shown in Figure 1(c) for a semiconducting LRS. We note that the RESET voltage is larger than the SET voltage in the semiconducting case which is the reverse of prior observations in other NiO resistive switching systems.²³ This behavior has been observed in SiO_x ^{37,38} as well as in devices constructed from ZnO microwires.³⁹ In the latter case, the authors also observed a reversal of SET and RESET voltages compared to bulk ZnO. We speculate that in our system the reversal of SET and RESET voltages originates from the unique transport characteristics of the QPC, but further study and modeling is required to confirm this.

The electroformation procedures shown in Figures 1(a) and 1(b) preferentially lead to metallic or semiconducting states, respectively. However, since breakdown is a stochastic process, linear or non-linear characteristics can occur with either method. We formed 16 devices using the single-step method in Figure 1(a) and found that 8 devices broke during the electroformation, 3 devices exhibited predominantly linear IV characteristics, and 5 displayed non-linear IV behaviors. The multi-step procedure in Figure 1(b) was also used on 16 devices and led to non-linear IVs in 8 cases, linear IVs in 5 cases, and 3 ruptured devices during the electroformation process. Non-linear characteristics are preferentially achieved with the procedure in Figure 1(b); however, our observations do suggest that there is a degree of randomness in the electroformation process that likely depends on the rate of current increase.

While the majority of experimental studies on resistive switching devices have been performed at room temperature, variable temperature measurements can illuminate the mechanism of filamentary conduction. IV characteristics of the semiconducting LRS generated with the multi-step

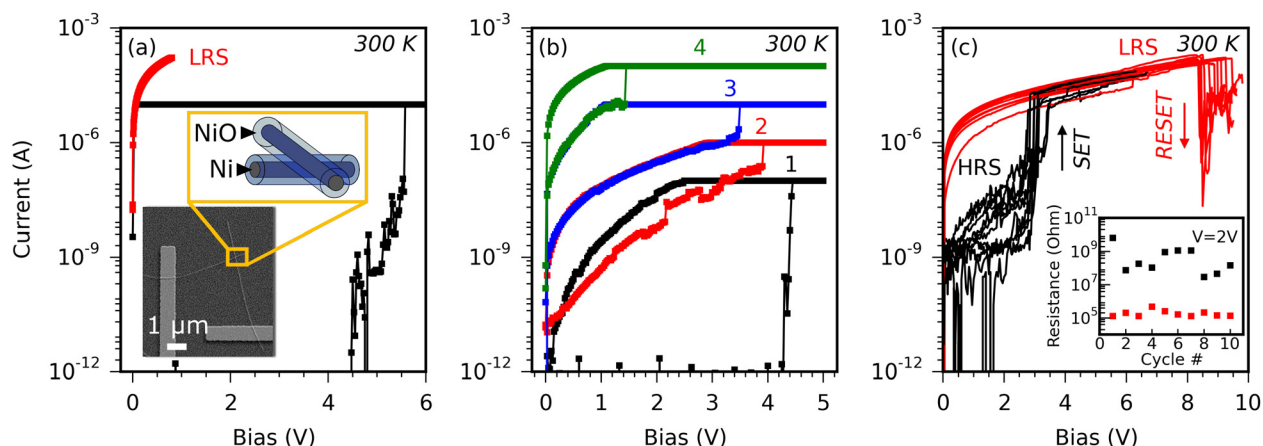


FIG. 1. (a) Formation of a metallic LRS (red trace) in a nanowire junction using a single electroformation sweep (black trace) with a current compliance of $10 \mu\text{A}$. Inset shows a device schematic illustrating the nanowire junction. (b) Formation of a semiconducting LRS using a series of electroformation sweeps with progressively higher current compliances, beginning at $0.1 \mu\text{A}$ and increasing to $100 \mu\text{A}$. The numbers 1–4 reference measurement order. (c) Forward IV sweeps demonstrating repeated unipolar switching between the semiconducting LRS and the HRS for 10 SET/RESET cycles. The inset compares the resistance of the LRS (red squares) to that of the HRS (black squares) over the switching cycles depicted.

electroformation procedure of Figure 1(b) were measured at selected temperatures from 15 K to 250 K and are plotted in Figure 2. The IV relations are nonlinear over the entire bias range (Figure 2(a)) while the R(T) data exhibit a negative TCR (Figure 2(b)), both of which are consistent with semiconducting transport. Interestingly, though most semiconducting LRSs measured were stable with switching (Figure 1(c)), one device exhibited considerable modification of its IV curves in a different RESET/SET cycle, which is discussed in the [supplementary material](#) in Figures S2 and S3.

Non-linear IV characteristics in filamentary conductors have been attributed to a variety of mechanisms, including Poole-Frenkel conduction, thermionic emission, and tunneling.^{19,24,40–43} R(T) data demonstrated by the conventional semiconducting LRS (Figure 2(b)) follow an exponential form, $R \propto \exp(-aT)$, at odds with the expected temperature dependence of each of the above.⁴⁴ However, this behavior is in good agreement with the temperature trends predicted by the QPC model, which describes conduction through an atomically thin bottleneck constriction.^{31,32,35} In this framework, quantum confinement at the constriction results in a local potential barrier, commonly modeled as parabolic in shape, and a series of energy subbands where conduction occurs only through the lowest level.³⁵ The temperature-dependent IV relationship for a QPC with a single conducting channel is given by³¹

$$I(V, T) = \frac{2e}{\alpha h} \left\{ \frac{\exp(-\alpha[\Phi(T) - \gamma eV])}{\text{sinc}(\pi\alpha kT)} [1 - \exp(-\alpha eV)] \right\}, \quad (1)$$

where e is the electron charge, h is Planck's constant, k is Boltzmann's constant, γ is a coupling factor between the external field and the local potential, α is related to the inverse of the potential barrier curvature, and $\Phi(T)$ is the effective barrier height. This barrier is temperature dependent, $\Phi(T) = \Phi_0 - \theta T$, where Φ_0 is the 0 K effective barrier height and the slope θ describes the reduction of barrier height due to increasing atomic vibrations at elevated temperatures.³¹ The result is a current, that varies exponentially with temperature, $I(T) \propto \exp(-\alpha[\Phi_0 - \theta T])$.³² As described by Walczyk *et al.*, $\gamma = \frac{x}{t_{ox}}$, where x is the location of the filament constriction as measured from the carrier-

injecting (cathodic) nanowire and t_{ox} is the oxide thickness.³¹ In NiO thin films, it is suggested that conducting filaments grow from the cathode to the anode,⁴ so we expect the filament constriction to be located within the oxide of the anodic nanowire. Using $\gamma = 1$, we find that the data in Figure 2(a) is fit well by the QPC model over the entire temperature and voltage range (black traces of Figures 2(a) and 2(b)), with the extracted values of $\Phi(T)$ and α summarized in Figure 2(c). Our fits indicate a 0 K barrier of $\Phi_0 = 4.6$ eV and slight temperature dependence in the barrier curvature, as well, with α following the functional form $\alpha = \alpha_0 - \beta T$.

If the barrier $\Phi(T)$ is known, the radius of the filament constriction at its narrowest point can be estimated through the following equation:³⁴

$$r = \frac{hz_0}{2\pi\sqrt{2m^*\Phi(T)}}. \quad (2)$$

Here, $z_0 = 2.404$ is the first zero of the Bessel function and m^* is the electron effective mass. For NiO, m^* has been found to vary between $0.6 m_0$ and m_0 , where m_0 is the free electron mass.⁴⁵ Assuming $m^* = 0.8m_0$, and using the results from the analysis of $\Phi(T)$ and α in Figure 2(c), we estimate the radius of the filament in the semiconducting LRS to be 2.5–3.5 Å, roughly corresponding to 1–2 Ni atoms thick.

Temperature-dependent IV measurements taken on a device set into a metallic LRS using the single-step electroformation procedure of Figure 1(a) are plotted in Figure 3, where the bias was kept below 1 V to avoid resetting the device into a HRS. The IVs reveal two bias regimes that exhibit opposite temperature-dependent behaviors, with a transition at ~ 0.27 V. All IV curves are linear in the high bias regime with a positive TCR, while those in the low bias regime are nonlinear with a negative TCR.

Unlike the semiconducting LRS, the metallic LRS could not be fit by the QPC model in Eq. (1). In fact, the intersection of the IV curves at 0.27 V is difficult to capture with a model that contains only one conduction mechanism and therefore we require two competing mechanisms to account for the observed behavior. Such intersecting IVs are consistent with conduction in a system where small, inhomogeneous barriers are in series with a conventional metallic resistance.^{46,47} low-field, low-temperature behavior is dominated by conduction

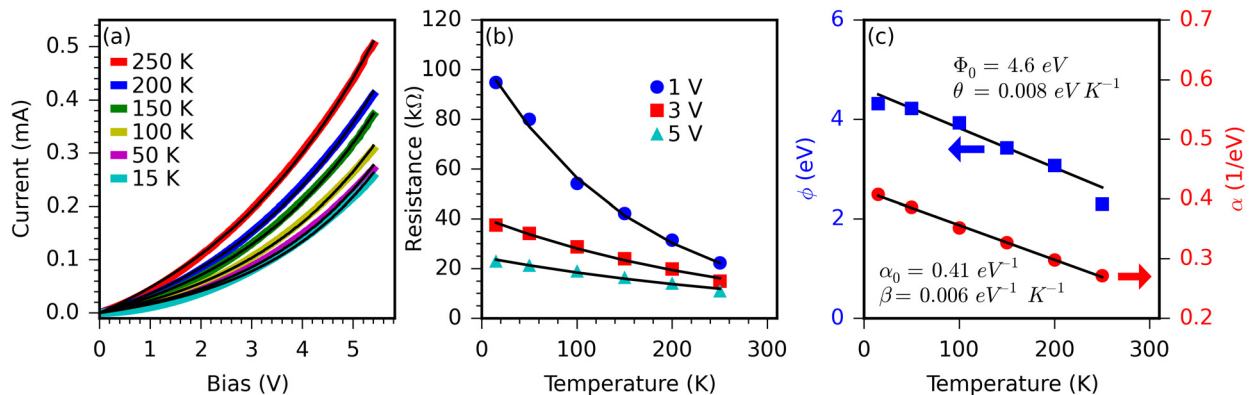


FIG. 2. (a) Temperature-dependent nonlinear IV measurements for a device in the semiconducting LRS formed using the electroformation procedure described in Figure 1(b). (b) R(T) data extracted from (a) at three different voltages. The black traces in (a) and (b) are fits to the QPC model. (c) Extracted parameters Φ and α obtained from QPC model fits to the semiconducting LRS data in (a) and (b). The black lines show the linear fits $\Phi(T) = \Phi_0 - \theta T$ and $\alpha = \alpha_0 - \beta T$.

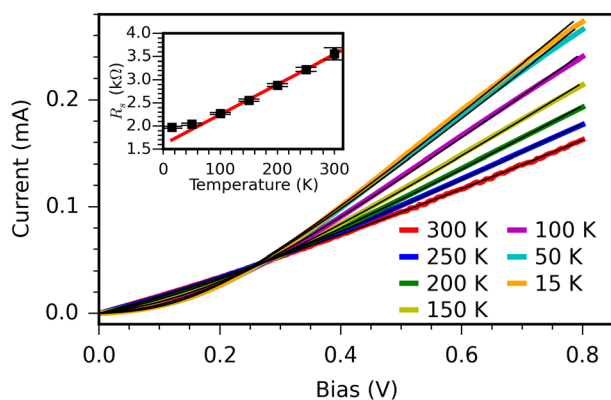


FIG. 3. Temperature-dependent IV curves for a device in the metallic LRS formed using the electroformation procedure described in Figure 1(a). The black traces are fits to Eq. (3). Inset: Temperature-dependent series resistance $R_s(T)$ extracted from fits to Equation (3). The error bars represent a 95% confidence interval.

across the barrier, and high-field, high-temperature conduction is dictated by the series resistance. Therefore, we propose that the single, high-compliance-current formation step generates a spatially non-uniform filament between the Ni nanowire cores. While the filament is sufficiently wide to prevent quantization effects, at some point along its length exists a small potential barrier to conduction. Outside of this barrier, the remainder of the metallic filament and the Ni nanowire cores contribute a series resistance that decreases with decreasing temperature, giving rise to the intersecting IV behavior observed in Figure 3. The IV relationship for this system is given by the relation

$$I(V, T) = A \left(\exp\left(\frac{e[V - IR_s(T)]}{nkT}\right) - 1 \right), \quad (3)$$

where A is a temperature-dependent current prefactor, $R_s(T)$ is the series resistance, and n is a temperature-dependent ideality factor. The data fit this equation well (black traces of Figure 3) and allow for the extraction of R_s at each temperature (Figure 3, inset). $R_s(T)$ is linear above 50 K (red trace of Figure 3, inset), yielding a positive TCR of $\sim 2.2 \times 10^{-3} \text{ K}^{-1}$, which is consistent with recent observations by Iwata *et al.* in the LRS of NiO film devices.⁴⁸ The temperature dependence of the parameters A and n can be found in Figure S4 of the [supplementary material](#).

The variation in temperature-dependent conduction between the two LRSs suggests a path toward control of the filament geometry through the electroformation procedure. The single-step, high I_{CC} process of Figure 1(a) generated a thick filament in series with a spatially inhomogeneous potential barrier that exhibits metallic conduction in the LRS (Figure 4(a)), while the stepped I_{CC} electroformation procedure in Figure 1(b) yielded a filament with an atomic constriction that exhibits QPC-like semiconducting behavior in the LRS (Figure 4(b)). Evidence suggests that switching from either the metallic or semiconducting LRS into a HRS results from an actual rupture of the filament, where conduction occurs through a series of larger, randomly distributed potential barriers.^{4,21,48} In these devices, the HRS shows a very high resistance and variable temperature-dependent IV characteristics (Figure S5 of [supplementary material](#)).

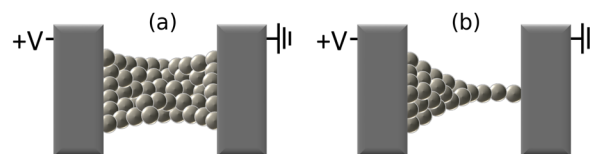


FIG. 4. Schematics of (a) a wide metallic filament formed using a single-step electroformation sweep and (b) a narrow semiconducting filament formed using a stepped electroformation procedure.

In conclusion, we have demonstrated the realization of metallic and semiconducting LRSs in nominally identical Ni/NiO single nanowire junctions. Distinct filamentary structures and electrical behaviors can be achieved by regulating the current compliance during the electroformation step. In particular, a series of sweeps with gradually increasing compliances preferentially leads to a narrow filament with semiconducting characteristics that are well fit using the QPC model for electronic transport through an atomic scale constriction. The variety of filamentary conductive states demonstrates the potential of Ni nanowire junctions for use as multifunctional nanoscale memory devices and as a platform for investigating quantum transport in the one-dimensional limit. We envision that the ability to tune filament geometry through the electroformation process can be made deterministic with additional device engineering and may lead to the on-demand realization of semiconducting or metallic behavior. The ability to control the conducting state in filamentary systems would be potentially useful for combining selector and memristor functionalities in a single device and could also support advanced neuromorphic architectures that benefit from a diversity of device behaviors.

See [supplementary material](#) for a transmission electron microscopy image of a Ni/NiO nanowire, further discussion of the semiconducting LRS, temperature dependence of the extracted parameters from fitting to the metallic LRS, and temperature-dependent IV curves of the HRS.

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