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Characterization of graphene-silicon Schottky barrier diodes using impedance spectroscopy

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We investigate the interface characteristics of graphene-silicon Schottky barrier diodes using dc current-voltage measurements and ac impedance spectroscopy (IS). Diode parameters, including the ideality factor and the Schottky barrier height (SBH), are extracted from the experimental data. In particular, IS makes it possible not only to define the influence of additional capacitive components due to the metal electrode contact area of the device by using a proper equivalent circuit model for the analysis but also to extract a more reliable SBH value. Therefore, we expect that IS could be widely utilized for research on the interfaces of various graphene-based devices.
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Graphene is considered one of the most promising candidates for future semiconductor industry applications because of its extraordinary properties.[1–3] Thus far, it has drawn enormous attention from various research fields and intensive studies on its characteristics have been performed.[4–7] Based on its unique electrical properties, a number of works on electronic device applications[8–12] have been carried out. Furthermore, its high conductivity makes it suitable for replacing traditional metal electrodes in diodes, which results in the formation of a Schottky contact with various semiconducting materials.[13,14] In particular, the graphene-semiconductor Schottky contact structure has recently been employed in graphene-based devices such as solar cells,[15–17] barristors,[18] and sensors.[19] Therefore, the investigation of Schottky contacts between graphene and semiconductors, which is the simplest but one of the most widely used structures in graphene-based devices, can be considered an important topic in graphene device application research. It is therefore essential to define the electrical characteristics of graphene-semiconductor interfaces in order to comprehensively understand the current transport mechanism at the interface.

In this work, we fabricated graphene-silicon (G-Si) Schottky barrier diode (SBD) devices and characterized the interface between graphene and silicon electrically using dc current-voltage (*J-V*) measurements and ac impedance spectroscopy (IS) analysis. IS has primarily been used to study the charge carrier transport mechanism in organic semiconductor devices and solar cells,[20,21] and measured impedance spectra can be electrically interpreted with a proper equivalent circuit model. Recently, we developed an extended equivalent circuit model for the electrical characterization of Schottky contacts between various conductive carbon thin films and silicon.[22] In general, diode parameters, such as the ideality factor and the Schottky barrier height (SBH), are extracted through traditional current-voltage (*J-V*) and/or capacitance-voltage (*C-V*) measurement methods. It is difficult to obtain reliable junction capacitance values from SBD devices using the traditional *C-V* method, particularly when the devices have a series resistance. It has been shown that the existence of series resistance in a diode device can cause considerable errors in calculation of the diode parameters,[23,24] but, in practice, it is not possible to make a SBD device without any series resistance. Here, we used IS to obtain capacitance values at the junction as this gives more reliable values than the traditional *C-V* method, particularly for microscopic systems with varying series resistances. IS has recently been applied to the analysis of the metal-semiconducting nanowire contact and the interface of carbon-silicon SBD devices with series resistance.[22,25] In this study, IS was employed for the investigation of the interface of G-Si SBD devices for an accurate analysis of the Schottky junction and to extract information about the interface between silicon and graphene.

A thermally grown silicon dioxide (SiO_2) layer (150 nm) on an n-type silicon (n-Si) wafer with a dopant (phosphorus) concentration of $5 \times 10^{14}\,\text{cm}^{-3}$ and $\langle 100 \rangle$ orientation was used as a substrate for the device. A part of the SiO_2 layer was completely removed by a wet etching process with 3% diluted hydrofluoric acid (HF) for 10 min, followed by rinsing with deionized water and drying. Using a shadow mask, titanium (Ti) and gold (Au) metal electrodes (Ti/Au = 20/80 nm) were sputtered on the top center of the remaining SiO_2 layer and the exposed n-Si area, respectively, and a good ohmic contact was achieved between Ti and n-Si. Graphene was produced using chemical vapor deposition (CVD) on copper (Cu) foils as described in detail in our previous work.[26] The graphene was then transferred onto the pre-patterned substrate, directly after removing the native oxide layer from the exposed silicon surface with HF, in order to form a direct contact between the graphene and the silicon. One end of the graphene lies on the n-Si surface without touching the metal electrode deposited on the n-Si, and the other end sits on the gold pad on the SiO_2 layer which insulates a direct contact between the metal electrode and the Si substrate.

Raman spectra were obtained with a Witec Alpha 300 R microscope, using an excitation wavelength of 532 nm. *J-V*

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measurements were carried out on a Suss probe station connected with a Keithley 2612A source meter. The metal electrode on the SiO_2 layer was positively biased, and the electrode on the n-Si substrate was negatively biased. IS data were recorded by a Gamry Reference 600 potentiostat, and GamryEchem Analyst software was used for the data analysis. All the electrical measurements were performed under ambient conditions.

A photograph of the fabricated G-Si SBD device and its schematic diagram are depicted in Fig. 1(a). The device has an effective interface area of $\sim$0.2 cm^2 as measured by optical microscopy. Fig. 1(b) shows a Raman spectrum of the graphene on the SiO_2 part of the device which was obtained by averaging over 6400 scans taken over a $20 \times 20\,\mu$m area. It has a large 2D (at 2670 cm^{-1}) to G (at 1580 cm^{-1}) peak intensity ratio (I_{2D}/I_G) which is approximately 3, clearly indicating that the graphene has a monolayer thickness. There is a negligible D-peak contribution underlining the high quality of the graphene. More details on the Raman data are given in the supplementary material.[34]

The dark current-voltage measurement data of the graphene/n-Si (G/n-Si) SBD device are plotted in Fig. 2(a), which shows typical rectifying behavior. The relationship between the current density (J) of the diode and the voltage drop across the junction (V_D) of the Schottky junction can be described using thermionic emission theory and it is given by the following equation:[27]

$$J = J_s\left(\exp\frac{qV_D}{nk_BT} - 1\right), \quad (1)$$

where J_S is the reverse saturation current density, n is the ideality factor, k_B is the Boltzmann constant, q is the elementary charge, and T is the absolute temperature in Kelvin. The reverse saturation current density (J_S) can be expressed as

$$J_s = A^{**}T^2 \exp\frac{-q\phi_B}{k_BT}, \quad (2)$$

where A^{**} is the effective Richardson constant for n-Si and φ_B is the effective barrier height at zero bias. When considering the effect of the series resistance (R_S) of the system, which can stem from the resistance of the graphene and Si substrate, the contact resistances to the metal electrodes and interface states at the junction, V_D of the Eq. (1) can be replaced with the combination of the total voltage drop, V, of the system and the voltage drop due to R_S. Thus, $V_D = V - JR_S$, and for $V_D > 3k_BT/q$, Eq. (1) becomes

$$J = J_s \exp\left[\frac{q(V - JR_s)}{nk_BT}\right]. \quad (3)$$

Cheung and Cheung outlined the extraction of diode parameters, like the ideality factor and the barrier height, using the J-V measurement data from a SBD device with series resistance.[28] Applying this method to our measurement data gives the values of $n = 1.38$ and $q\varphi_B = 0.69$ eV. In general, the ideality factor higher than the unity observed in real SBDs can be attributed to several factors such as the image force lowering effect, additional thermally assisted carrier tunneling

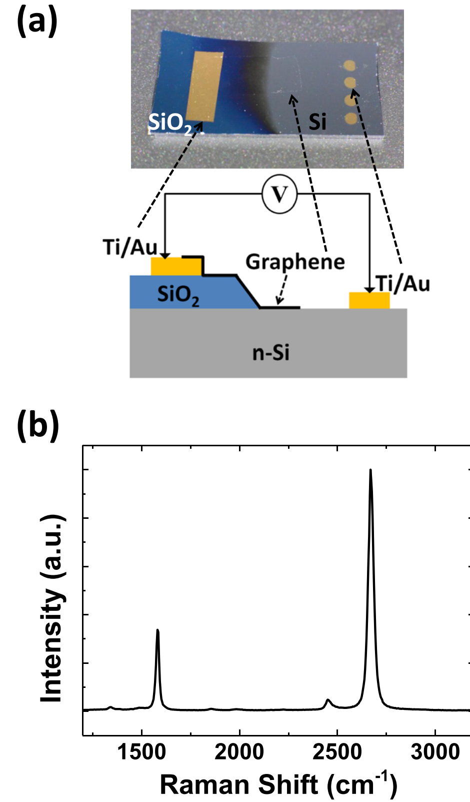

FIG. 1. (a) A photograph of the G/n-Si SBD device (top) and its schematic diagram (bottom). (b) Average Raman spectrum of high quality graphene on the SiO_2 layer of the device.

at the junction, bias dependent SBHs, and Schottky barrier inhomogeneity in the junction area.[29,30] In the case of G-Si SBDs, it is known that charge puddles can be formed unintentionally during the graphene synthesis or transfer process, which causes Schottky barrier inhomogeneity at the interface. These factors can be quantified by calculating the flat band barrier height (φ_{BF}), where the influence of such factors on the evaluation of J-V data does not exist, so it can be used as a fundamental value for the comparison between experimental and theoretical data.[31,32] φ_{BF} can be calculated by using

$$\phi_{BF} = n\phi_B - (n-1)\left(\frac{k_BT}{q}\right)\ln\left(\frac{N_c}{N_d}\right), \quad (4)$$

where N_c is the effective density of states in the conduction band and N_d is the carrier density. Using this equation, the calculated value of $q\varphi_{BF}$ is found to be 0.84 eV, which is larger than $q\varphi_B$ from the J-V measurement data.

Impedance spectra of the G/n-Si SBD device were obtained in the frequency range of 0.1 Hz to 1 MHz with an ac voltage of 10 mV under various dc biases (from -0.6 to $+0.6$ volts with a step of 0.1 V) at room temperature. Figs. 2(b) and 2(c) show Cole-Cole impedance plots of the G/n-Si SBD under forward, zero, and reverse dc bias. The radius of the semicircles, which is related to the total impedance of the device, increases as the dc bias decreases in the forward bias region while it shows a clear upsurge in diameter in the zero and reverse bias regions. This means the impedance value of the device is dependent on the applied dc bias and it has a much larger value under reverse bias than forward bias. The

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nearly semi-circular shape of the impedance spectra over the whole dc bias range indicates that the Schottky junction can be expressed using an equivalent circuit model which is composed of a combination of resistance and capacitance (RC) networks.[33] A typical equivalent circuit model of a Schottky junction consists of a parallel connected RC network and a series resistance which is serially connected to the RC network. The RC network represents the space charge region and the series resistance accounts for the contact and bulk resistance of the device, respectively, showing a perfect semi-circular Cole-Cole impedance plot. However, the plots of Figs. 2(b) and 2(c) do not have perfect semi-circular shapes. This implies that there is more than one RC component in the system where the contact area of each metal electrode can cause extra capacitive components in the

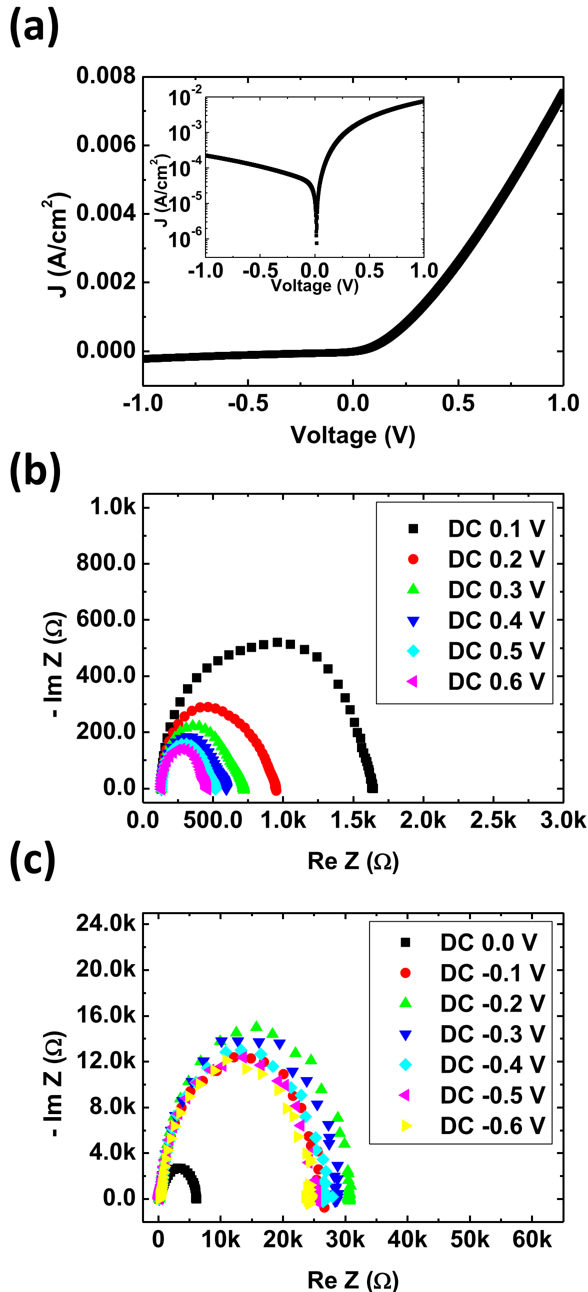

FIG. 2. (a) Dark *J-V* measurement of the G/n-Si SBD on a linear scale. Inset: *J-V* curve on a semi-logarithmic scale. (b) Cole-Cole plots of the G/n-Si SBD under forward dc bias and (c) under zero and reverse dc bias.

device. Therefore, a more complex equivalent circuit model was used for the analysis of the impedance spectra,[22] where the influence of the contacts between the Au pad and the graphene sheet and the Ti/Au electrode and the n-Si substrate are taken into account. The equivalent circuit model is presented in Fig. 3(a). It has three RC pairs in series connected with a series resistance (R_S) and a parasitic inductance (L). C_1, C_2, and C_3 are the capacitances related to the Au-graphene, graphene-Si, and Si-Ti interfaces, respectively, with corresponding shunt resistances R_1, R_2, and R_3. In general, the ac impedance (Z) is expressed by

$$Z(\omega) = Z'(\omega) - jZ''(\omega), \tag{5}$$

where ω is the frequency, Z' and Z'' are the magnitudes of the real and imaginary parts of the impedance, respectively.[33] For mathematical analysis of the equivalent circuit model in Fig. 3(a), Z' and Z'' can be expressed as

$$Z'(\omega) = \frac{R_1}{1+(\omega R_1 C_1)^2} + \frac{R_2}{1+(\omega R_2 C_2)^2} + \frac{R_3}{1+(\omega R_3 C_3)^2} + R_s, \tag{6}$$

$$Z''(\omega) = \frac{\omega R_1^2 C_1}{1+(\omega R_1 C_1)^2} + \frac{\omega R_2^2 C_2}{1+(\omega R_2 C_2)^2} + \frac{\omega R_3^2 C_3}{1+(\omega R_3 C_3)^2} - \omega L. \tag{7}$$

The fitted curves, with experimental data obtained under various dc biases using these equations, are depicted in Figs. 3(b)–3(e), showing a good fit with each other. The resistance and capacitance values extracted from the best fit of the experimental impedance data are plotted in Figs. 4(a) and 4(b) with a semi-logarithmic scale for the G/n-Si SBD device. While the series resistance, R_S, is constant over the whole bias region with an average value of $130 \pm 0.7\ \Omega$, R_2 shows a significant change as the dc bias varies from the forward to reverse region. It has very high values compared to the other resistances in the reverse dc bias region, and it can be conceived that the R_2C_2 component of the equivalent circuit model is related to the Schottky barrier at the G/n-Si interface because R_2 suppresses the current flow at the junction under reverse dc bias. When a forward dc bias is applied, it suddenly drops dramatically with increasing bias voltage. This can be explained by considering that more current can flow through the Schottky junction since the barrier is lowered by the forward bias, leading to a drop in the junction resistance. The other RC network components (R_1C_1 and R_3C_3) of the model, related to the Au-graphene contact (R_1C_1) and the Ti-Si contact (R_3C_3), respectively, show relatively small variation over the whole dc bias region with an averaged contact resistance value of $404 \pm 77\ \Omega$ for R_1 and $88 \pm 20\ \Omega$ for R_3. In the ideal case, the interfaces at the Au-graphene and Si-Ti contacts should not be influenced by the external bias, however, imperfect surface conditions, like possible defects at the interfaces, can give rise to such variation in a practical case. Even though the detailed mechanism which causes the bias dependent behavior at the metal

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electrode contact area of the device is not clearly verified, IS makes it possible to separate the effect of each electrode contact from the whole capacitive component of the device and quantify it using the proper equivalent circuit model.

Using the depletion capacitance (C_2) of the Schottky junction, a Mott-Schottky plot ($1/C^2$ vs. V) can be established and information on the built-in potential (V_{bi}) and the SBH ($q\varphi_B$) of the device at the junction can be derived.[27] The Mott-Schottky plot of the G/n-Si SBD is shown in Fig. 4(c). The V_{bi} can be determined by linear extrapolation of the intercept with the x axis (dc bias), giving values of $V_{bi} = 0.54$ V and a calculated value of $q\varphi_B = 0.82$ eV. The value of SBH obtained from the Mott-Schottky plot is not fully consistent with the value from the previous J-V data ($q\varphi_B = 0.69$ eV), showing an increase of 0.13 eV. This discrepancy may stem from the possible presence of a thin insulating layer at the G-Si interface and/or Schottky barrier inhomogeneity.[17,24,30] The value of SBH from the Mott-Schottky plot is in excellent agreement with the above calculated flat band barrier height ($q\varphi_{BF} = 0.84$ eV), underlining the fact that IS results in a more accurate parameter extraction on the SBH of the device than the dc J-V measurement method. However, it should be noted that while a dc J-V measurement method is mainly utilized to define the current transport mechanism at the junction and the ideality factor representing the performance of diodes, an ac IS measurement method has merit for the characterization of the space charge region at the junction and it can localize the effect of metal electrode contacts from the system; therefore, they are complementary for the study of the interface of SBDs.

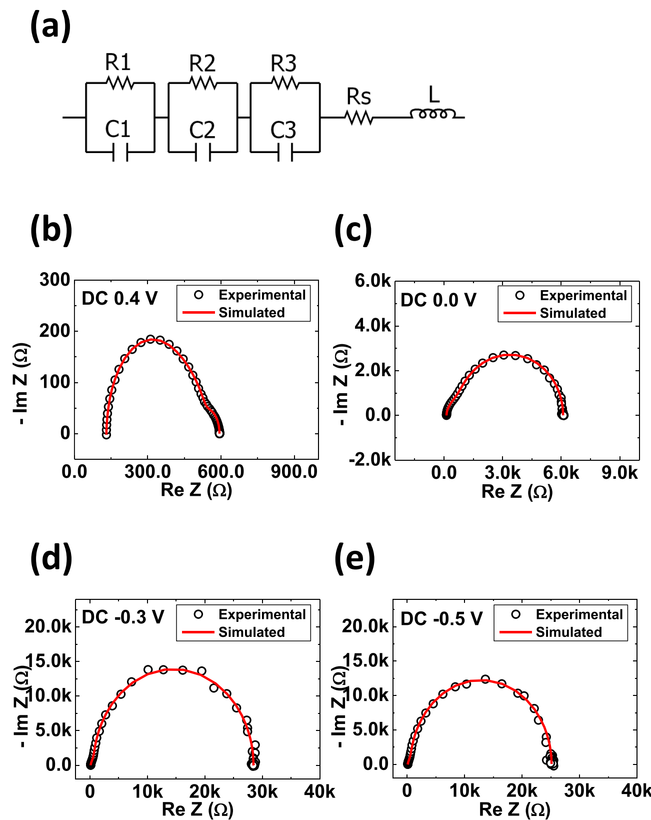

FIG. 3. (a) Equivalent circuit model of the G/n-Si SBD for the IS analysis where R_1C_1, R_2C_2, and R_3C_3 represent the RC networks related to the interfaces of Au-graphene, graphene-Si, and Si-Ti, respectively. R_S is the series resistance and L represents a parasitic inductance associated with the electrical leads. Cole-Cole plots and corresponding fit from the equivalent circuit model on the G/n-Si SBD under dc bias of (a) +0.4 V, (b) −0.0 V, (c) −0.3 V, and (d) −0.5 V.

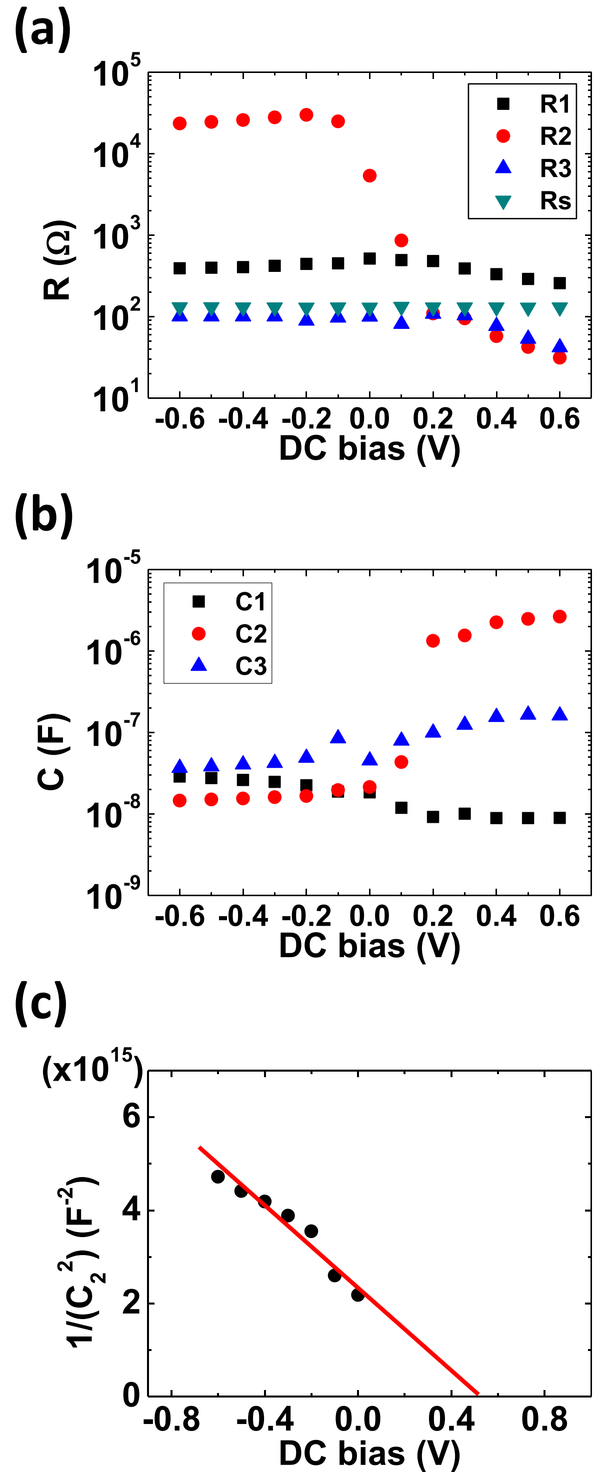

FIG. 4. Semi-logarithmic plots of (a) resistance and (b) capacitance values for dc bias voltages in the range of +0.6 V to −0.6 V achieved from the best fit of the IS of the G/n-Si SBD using the equivalent circuit model of Fig. 3(a). (c) The Mott-Schottky plot ($1/C^2$ vs. V) of the G/n-Si SBD with C_2 values extracted from the simulated results using the equivalent circuit model of Fig. 3(a).

In summary, G/n-Si SBDs were fabricated and investigated using dc J-V and ac IS measurements. An ideality factor of 1.38 and a SBH of 0.82 eV were extracted from the experimental data. In our work, we utilized the IS method to obtain

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a more reliable SBH value using a proper equivalent circuit model for the analysis. It is expected that this kind of approach to the investigation of graphene-based nanoscale devices will allow the interface of the devices to be interpreted in a more comprehensive and detailed way. This is of particular importance because most graphene SBDs are not completely free from the effect of metal electrode contacts and also the graphene-semiconductor interfaces may not be ideal. Thus, this study will facilitate graphene-based device developments, particularly for diodes, sensors, and solar cells.

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[34]See supplementary material at http://dx.doi.org/10.1063/1.4829140 for additional Raman details.

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