

# Design and Construction of an Optoelectronic Crossbar Switch Containing a Terabit per Second Free-Space Optical Interconnect

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(Invited Paper)

**Abstract**—The completed detailed design and initial phases of construction of an optoelectronic crossbar demonstrator are presented. The experimental system uses hybrid very large scale integrated optoelectronics technology whereby InGaAs-based detectors and modulators are flip-chip bonded onto silicon integrated circuits. The system aims to demonstrate (a 1-Tb/s aggregate data input/output to a single chip by means of free-space optics.

**Index Terms**—OE-VLSI, Optical interconnects, smart-pixels.

## I. INTRODUCTION

THE COMPLETED design of a demonstrator system being developed to explore the capabilities of optoelectronic interconnects based on hybrid integrated circuits (III–V semiconductor on silicon-CMOS) and free-space parallel optical connections is described in this paper. A major aim of this paper is to investigate the use of such a technology to provide aggregate input/output (I/O) data-rates to a conventional CMOS chip in the terabits per second domain. Interfaces

working on the scale of terabits per second and above will be required to meet the I/O requirements of future generation integrated circuits and switching systems [1] but calculations have shown [2], [3] that electrical interconnects have fundamental difficulties, arising from the skin effect, in achieving links of these bandwidths over distances of several centimeters. While state-of-the-art CMOS already offers production electronic interface technology with a capacity of 160 Gb/s [4], these limitations suggest that a new technology capable of delivering an order of magnitude more bandwidth—of the order of several terabits per second—is required to meet long-term needs.

In recent years, a technology referred to as optoelectronic very large scale integration (OE-VLSI) technology has emerged as offering a potential solution to this problem. It is based on hybrid integration of surface normal optoelectronic devices with mainstream VLSI electronics using attachment techniques such as flip-chip bonding. A number of experimental demonstrator systems using this technology have been already constructed with terabits per second or near terabits per second optical interfaces [5]–[7], but fully populating these systems has been difficult and complete operation of such an interface is yet to be achieved. In addition, certain issues such as electrical crosstalk and thermal uniformity are unresolved.

In order to fully exercise such an interconnect in a realistic system context, we have chosen to construct a crossbar switch that exploits an optical fan-out of 64 input signals by a factor of 64 to provide the connectivity required by the switch matrix. With a 250-Mb/s targeted data-rate for each signal, the capacity of the internal interconnect is 1 Tb/s, while the system can be fully tested with only 64 input sources. In the course of this design, we have explored the issues that limit the design and have developed the technologies required by such free-space optical interconnects, including micro/diffractive optics, optomechanical packaging, vertical-cavity surface-emitting laser (VCSEL) and modulator fabrication and smart-pixel VLSI design.

Although the prime motivation for constructing this experimental system is to explore the potential of optical interconnect

Manuscript received November 24, 1998; revised March 22, 1999. The project SPOEC was supported by the European Union under the ESPRIT proactive scheme: Microelectronics Advanced Research Initiative (MEL-ARI) Opto-Cluster. The work of M. P. Y. Desmulliez was supported by NATO under Grant CRG 961061.

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Publisher Item Identifier S 1077-260X(99)06060-8.

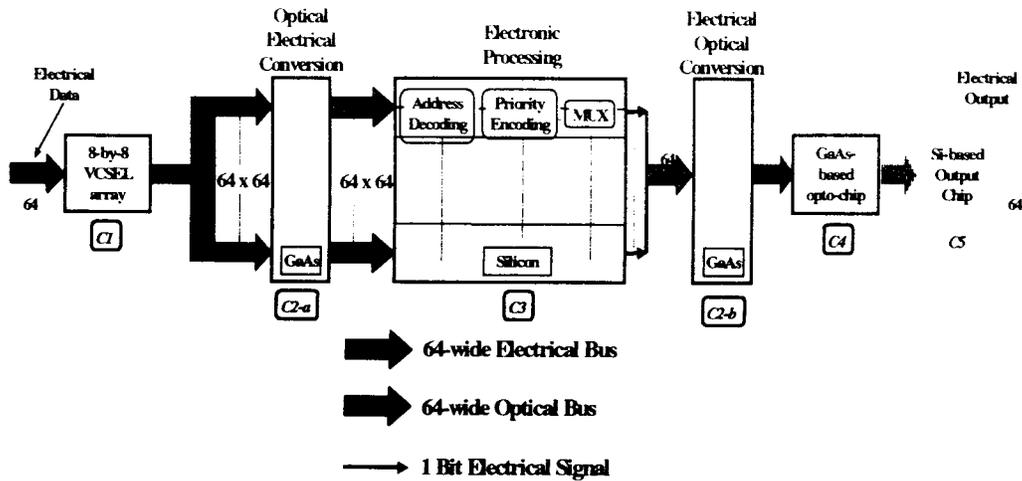


Fig. 1. General architecture of the system demonstrator.

technology, it is nevertheless the case that crossbar switches are a good example of a system that can exploit the high connectivity offered by free-space optics. Thus, although the switch does not fully address the needs of a specific application, it remains a valuable generic architecture for considering how OE-VLSI may be used for routing applications.

In this paper, we describe the design of the system introduced above and report on the initial stages of construction and findings on some of the important issues in the design of terabits per second scale optical interfaces. The overall system architecture is described in Section II. The optical layout of the system and design of the optical demonstrator hardware are discussed in Section III. Descriptions of the VLSI switching circuit and the modulator/detector array with which it is flip-chip integrated are given in Sections IV and V, respectively. The inputs to the crossbar system are provided by a VCSEL array, whose performance characteristics are given in Section VI. General conclusions are drawn in Section VII.

## II. SYSTEM ARCHITECTURE

The demonstrator system, that has been designed as part of the European project Smart Pixel Optoelectronic Connections (SPOEC), takes the form of an optoelectronic matrix-matrix crossbar [8]. The functional schematic of such a system is shown in Fig. 1. Starting from the left-hand side, input electrical data (64 signals) are converted into optical signals by an electrically addressed 8-by-8 VCSEL array (circuit C1). Each of the 64 optical outputs from the array are themselves fanned out 64 times by an 8-by-8 fan-out diffractive optical element (DOE). The resulting set of 4096 optical signals, incident on the InGaAs optoelectronic chip (circuit C2-a) defines a partition of 64 blocks or “super-pixels” at the optoelectronic interface. Each super-pixel receives the full set of 64 optical input signals and converts these into electrical signals which are electrically fanned-in (fan-in of 64-to-1) by the silicon-based 0.6- $\mu\text{m}$  (CMOS) routing chip (circuit C3). The unique output from each super-pixel, which represents one of the original set of 64 signals, is converted back into an optical output by means of a differential pair of multiple-

quantum-well (MQW) spatial light modulators (circuit C2-b). The 64 output optical signals are sent, in this case, to a simple output chip composed of an array of photoreceivers (circuit C4) flip-chip bonded onto a silicon chip (circuit C5) that converts the signals to electrical outputs.

The crossbar system thus includes a  $64 \times 64$  switch matrix with optical inputs and outputs permitting nonblocking one-to-one or unrestricted broadcast connectivity. The target data-rate is 250 Mb/s per channel. The system is designed as a packet switch with the routing chip configured by the packet header, which contains the address information provided as part of the optical inputs. Arbitration between those inputs which simultaneously request access to the same output is handled internally by means of a cyclic priority scheme.

In this demonstrator, a strained InGaAs on GaAs optoelectronic chip implements the optical-to-electrical and electrical-to-optical conversion of the signals, thereby allowing the use of a single chip for the circuits C2-a and C2-b. The interfacing of this chip with the silicon-based routing chip is carried out by solder-bump flip-chip bonding [9]. The specified overall throughput of the switch (i.e., before fan-out) is around 16 Gb/s, corresponding to 62 250-Mb/s data inputs. The two remaining optical inputs are used for the (differential) clock signals which are distributed optically to each super-pixel [10].

It is worth noting why we chose to use a separate, optically-connected, output chip rather than taking the signals directly off the routing chip. Firstly, we wanted to avoid having to drive 62 signals off-chip at 250 MHz. Drivers with this performance consume significant amounts of power and take up more area than we had available on the routing chip. Secondly, this routing chip is partitioned so that the high-speed signals are local to each super-pixel, and thus all the necessary data inputs and the clock are provided optically within the super-pixel area. By providing an optical output we maintain this independent structure and avoid the problem of tracking fast signals across the chip (which can lead to serious cross-talk difficulties). The advantage of optical interconnects is again demonstrated in this context by the simple manner in which the output modulators can be driven directly from the digital

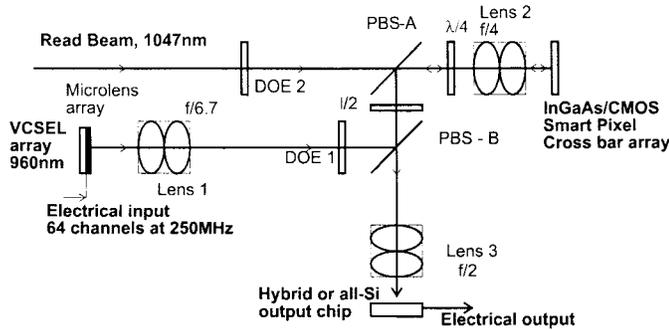


Fig. 2. Optical layout of the system demonstrator.

circuitry. It is also the case that, by avoiding cross-chip high-frequency signals, this partitioning is particularly suited to scaling up in size.

### III. OPTICAL LAYOUT

#### A. Functional Description

The optical system layout [11], shown in Fig. 2, is designed to work at 956 and 1047 nm, the wavelengths of the VCSEL's and modulator readout laser, respectively. The two optical paths through the system are: 1) from the VCSEL array to switching chip (Arm 1 or input arm) and 2) from the readout laser to output chip detectors via the routing chip (Arm 2 or output arm). In the input arm, a square array of 64 optical input signals is provided by the 8-by-8 array of VCSEL's. The output from the VCSEL's is partially collimated (increased in  $f$ /number from 3 to 6.7 at 95% power gathered) using a refractive microlens array. A multi-element bulk lens (Lens 1) collimates the 64 beams. These beams are then fanned-out to form an  $8 \times 8$  array by a diffractive optical element (DOE1) and directed toward the routing chip by two polarizing beamsplitters (PBS-A and PBS-B) which operate as polarization-independent reflectors at the VCSEL wavelength. A second multi-element bulk lens (Lens 2) images the  $64 \times 64$  array of optical signals onto the single-ended detectors of the routing chip. The collimated and polarized beam from the read laser (Nd:YLF) is fanned-out to an  $8 \times 16$  array by DOE2 and passed through PBS-A which is operating as a polarizing beamsplitter at this 1047 nm wavelength. A quarter wave plate ( $\lambda/4$  in Fig. 2) circularizes the polarization before Lens 2 images the read beams onto the  $8 \times 8$  array of differential modulators that form the output from the routing chip. Reflected light from the modulators is collected by Lens 2, converted to a polarization orthogonal to the input by the quarter-waveplate and reflected by PBS-A. To permit PBS-B to be an identical design to PBS-A, a half-wave plate ( $\lambda/2$ ) polarization rotator is inserted between them. Lens 3 images the output beams onto a matching  $8 \times 8$  array of differential detectors on the output chip.

Binary phase gratings are preferred over multi-level gratings for all the diffractive components because they provide very effective zeroth-order suppression despite their lower efficiency. This is essential to avoid optical crosstalk where the zeroth-

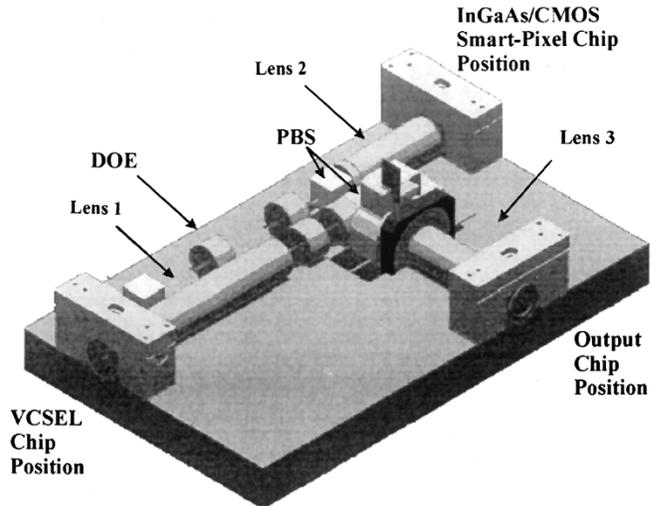


Fig. 3. 3-D rendering of the optomechanical arrangement of the designed system baseplate.

order image of the input signals overlaps with quadrants of the four central super-pixels. The use of diffractive optics in an optoelectronic interconnect requires that critical wavelength stability and array uniformity are maintained to ensure correct alignment of the beams onto the detectors. In this system the uniformity across the VCSEL array needs to be  $\Delta\lambda \leq 1$  nm. The optical components are mounted using the slot-plate approach [12]. A baseplate has been designed with V-grooves in which the barrel mounted components sit. The advantages of this scheme include the ease of focal adjustment combined with good stability. The three circuit boards that hold the VCSEL, routing and output chips are mounted on adjustable brackets for fine angular and positional control. The entire optomechanical system, shown in Fig. 3, fits into a box approximately  $30 \text{ cm} \times 20 \text{ cm} \times 10 \text{ cm}$  in dimension. For compactness, the continuous-wave Nd:YLF laser which provides the modulator read beams is mounted below the optical baseplate.

#### B. Optical Design

A telecentric 4-f imaging system, composed of custom-made multi-element lenses, conveys the signals from the VCSEL array to the InGaAs/CMOS routing chip. A second 4-f relay images the outputs from the routing chip to the output chip. The specifications for the three lenses that make up this system (see Fig. 2) are shown in Table I. Lenses 1 and 2 are five-element telecentric anastigmatic lenses, developed from earlier designs [13] using the CODE V ray-tracing software. A particularly demanding aspect of the optical design is the requirement that Lens 2 has excellent image quality over the wavelength range 956–1047 nm to ensure good performance for both the input (VCSEL) and read (Nd:YLF) beams. The output Lens 3 is an adaptation of Reiley and Sasian's lens [14].

Lens 2 has to be well-corrected over a large field (17.5-mm diagonal). This requirement led us to choose an  $f/4$  lens after working through the trade-offs inherent in compound lens design. Lens 1 was then required to be  $f/6.7$  to demagnify the

TABLE I  
KEY PARAMETERS OF THE MULTIELEMENT BULK LENSES

	$f/\#$	Focal Length (mm)	Field (mm)	Optimised at wavelength(s) (nm)
Lens 1	6.7	100.5	3	956
Lens 2	4	60.0	17.5	956 and 1047
Lens 3	2	30.0	8	1047

data channel separation from the 250- $\mu\text{m}$  VCSEL pitch to the 149.5- $\mu\text{m}$  pitch of the detectors on the routing chip. In turn, a further demagnification is desirable between the switching chip and the output chip to minimize the area of the output chip. The use of microlenses on the VCSEL chip is required since the multimode emission from the VCSEL's contains 95% of the output power in a cone of Numerical Aperture (NA) 0.17. To collect this optical power with a single bulk lens would present challenges to later optical elements so it was decided to split the collimation function between an  $8 \times 8$  array of refractive microlenses ( $f = 880 \mu\text{m}$ , diameter  $162 \mu\text{m}$ ) and the following bulk Lens 1. The fused-silica microlenses are operated at  $f/3$  to reduce the NA of the beams to 0.075 and thus match the NA of Lens 1.

Modeling of the two arms of the system has shown that we can expect spot diameters at the detectors on the switching chip of  $19 \mu\text{m}$  (90% enclosed energy). The expected spot sizes for the read beams at the modulators (80%) are  $26 \mu\text{m}$  and the reflection from these is imaged to  $13\text{-}\mu\text{m}$  (80%) spots on the output chip detectors. All of these dimensions are taken at the extremes of the imaged field. When manufacturing and assembly tolerances are included in the model, the required diameter for these three devices is expected to be 24, 28, and  $18 \mu\text{m}$ , respectively. Following this analysis, and allowing for alignment margins, device diameters of  $35 \mu\text{m}$  have been specified for the modulators and detectors on the switching and output chips.

Discrimination between the two wavelengths used is required within the system. While the 1047-nm beam from the Nd:YLF read laser can be polarization routed, the InGaAs VCSEL array is not polarization controlled. The two beamsplitters therefore need to act as PBS's at 1047 nm and as lossless polarization-independent reflectors at 956 nm to route the VCSEL emission efficiently. In addition, the large number of beams incident on the routing chip, combined with the degree of fan-out, requires that these beam-splitters operate over the relatively wide incident cone angle of  $\pm 7.5^\circ$ . The chosen PBS design is based on an air-spaced construction [15], rather than the usual cemented glass cube configuration, to exploit the inherent asymmetry and thus improve the performance. The materials used for the high/low refractive index coatings are  $\text{TiO}_2$  ( $n = 2.45$ ) and  $\text{SiO}_2$  ( $n = 1.45$ ). 27 layers were coated on a substrate of B270 ( $n = 1.51$ ) resulting in a total thickness of  $4.7 \mu\text{m}$ . Experimental tests of the fabricated beamsplitters have shown a contrast greater than 2:1 between  $s$  and  $p$  polarization reflection at 1047 nm and, importantly, more than 99% reflectivity of both  $s$  and  $p$  polarizations at 956 nm. These characteristics are maintained over a  $16^\circ$  angular

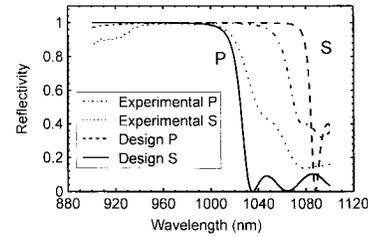


Fig. 4. Theoretical and experimental reflectivity coefficient spectra of the polarizing beamsplitters developed for routing optical signals through the system.

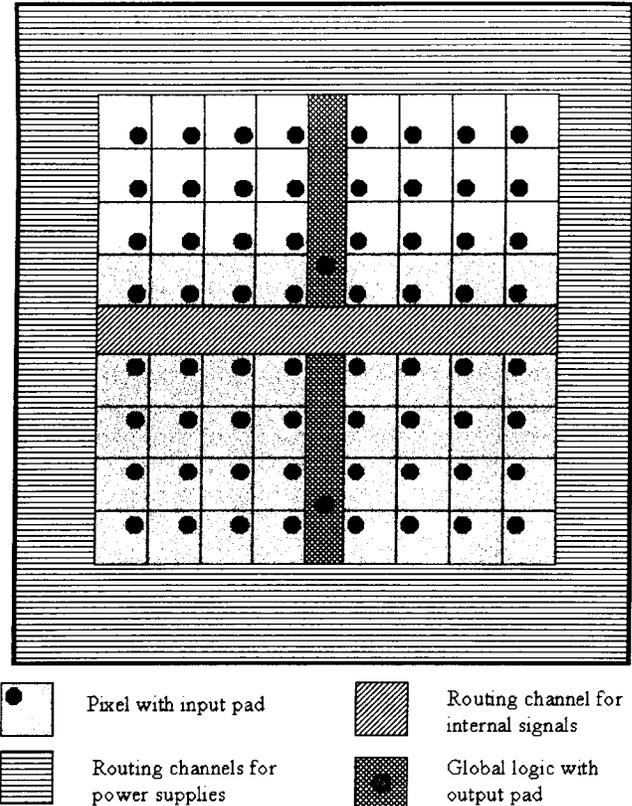


Fig. 5. Physical layout of one super-pixel on the CMOS routing chip.

range centered at  $45^\circ$ . The designed and measured spectral performances are shown in Fig. 4. It should be noted that, on the InGaAs/CMOS routing chip, the modulators in each differential pair are orientated vertically to reduce the influence of nonuniform beam splitter performance as a function of field angle at 1047 nm.

There is scope for significant increase of the density of data channels relayed by optical schemes of the type described here. The spot size predictions above indicate that a receiver array on a pitch of  $50 \mu\text{m}$  could be addressed, allowing data communication rates in the order of 10 Tb/s using the lenses described above. This would require considerably more dense electronic design at the routing chip than currently but indicates the potential of free-space optical relay of data.

### C. Optical Power Budget

A calculated optical power budget for the demonstrator system is shown in Table II. The optical power reaching the routing chip is of critical importance to ensure that sufficient

TABLE II  
OPTICAL POWER BUDGETS IN THE INPUT AND OUTPUT ARMS OF THE SYSTEM DEMONSTRATOR

Arm 1	Efficiency	Power after Element ( $\mu\text{W}$ )
<b>Output of single VCSEL</b>		<b>1250.00</b>
Coupling of VCSEL output by refractive microlens	93%	1162.50
Collimating Lens (Lens 1)	97.5%	1133.44
Risley Prisms (one pair)	98.8%	1119.84
8x8 fanout DOE 1 (division by 64)	1/64	17.50
8x8 fanout DOE 1 (efficiency)	60.0%	10.50
PBS-B (reflection, average of s and p)	98.7%	10.36
Half wave plate	98.0%	10.15
PBS-A (reflection, average of s and p)	98.7%	10.02
Quarter wave plate	98.0%	9.82
Focussing Lens (Lens 2)	97.5%	9.58
Coupling into detectors	90.0%	8.62
<b>Optical Power at detector on InGaAs chip</b>		<b>8.62</b>
External Quantum Efficiency	70%	6.03 $\mu\text{W}$
Ideal Responsivity (A/W)	0.77	4.65 $\mu\text{A}$
<b>Photocurrent expected from Detector</b>		<b>4.65<math>\mu\text{A}</math></b>
<b>Arm 2</b>	<b>Efficiency</b>	<b>Power after Element (mW)</b>
<b>Read beam optical power at 1047nm</b>		<b>500.00</b>
Risley Prisms (one pair)	98.8%	494.00
8x16 fanout DOE 2 (division by 8x8 modulator pairs)	1/64	7.72
8x16 fanout DOE 2 (efficiency)	60.0%	4.63
PBS-A (transmission)	60.0%	2.78
Quarter wave plate	98.0%	2.72
Focussing Lens (Lens 2)	97.5%	2.66
Coupling onto modulators	80.0%	2.12
Differential Modulation by InGaAs chip (30-60%)	30.0%	0.64
Collimating Lens (Lens 2)	97.5%	0.62
Quarter wave plate	98.0%	0.61
PBS-A (reflection)	96.0%	0.58
Half wave plate	98.0%	0.57
PBS-B (transmission)	60.0%	0.34
Risley Prisms (one Pair)	98.8%	0.34
Focussing Lens (Lens 3)	98.0%	0.33
Coupling onto output detector pair	90.0%	0.30
<b>Differential Optical Power at detector pair on output chip</b>		<b>0.30</b>

photocurrent is available for the silicon receivers to operate as designed. In the table, power losses are indicated in the two optical paths shown in Fig. 2. The values tabulated are those at an extreme field angle corresponding to the worst case for beamsplitter performance. Because of the limited output power of the VCSEL's and the large fan-out, arm 1 is the most critical in terms of power budget. Hence, the stringent requirements on PBS reflectivity at 956 nm and the adoption of composite collimation optics for the VCSEL's. The predicted 8.6- $\mu\text{W}$  optical power on each of the routing chip detectors and the resulting photocurrent of 4.7  $\mu\text{A}$ , is expected to permit operation with a satisfactory margin.

#### IV. ELECTRONIC DESIGN

Hybrid OE-VLSI technology imposes a certain number of constraints on the layout of the silicon electronics. For example, the positioning of the photoreceiver circuits, modulator drivers and the solder-bump pads required for flip-chip assembly, puts stringent constraints on the placement of electronic circuits with the two metal layer process chosen for fabrication. In addition the maximum die size permitted by the

silicon process has implications on the degree of smartness of the super pixel. The physical organization of the electronic chip is discussed in this section in the light of these constraints. A description of the transceivers is also given, along with their predicted performance and the key design issues relevant to designing a terabits per second OE interface.

##### A. Digital Circuit Design

1) *Physical Organization of the Super-Pixel:* The physical partitioning inherent in smart pixel technology makes the layout of the super pixel easily recognizable. The CMOS routing chip consists of 64 super-pixels, each of them divided into four blocks of 16 pixels as shown in Fig. 5. The overall dimension of the super pixel is 1614.5  $\mu\text{m}$  in the  $x$  and  $y$  directions with a pixel pitch of 149.5  $\mu\text{m}$ . This leaves a crosslike area into which is fitted the logic global to the super pixel (in the horizontal branch) and routing of internal signals and power cells (in the vertical branch). The input, solder-bump, bond pads have 18- $\mu\text{m}$  diameter and 149.5- $\mu\text{m}$  pitch. The output bond pads for the modulators are spaced at half the super pixel pitch.

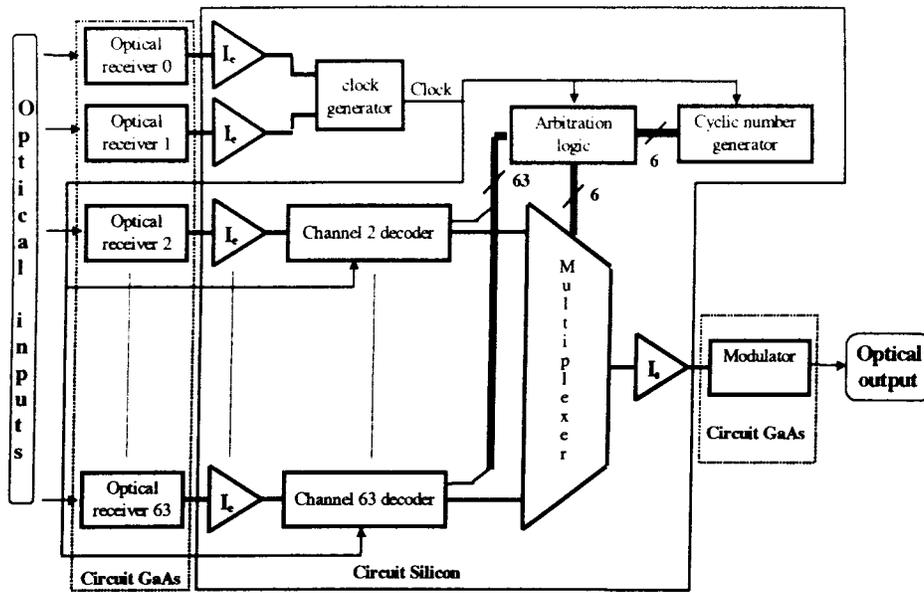


Fig. 6. Functional block diagram of one super-pixel within the CMOS routing chip.

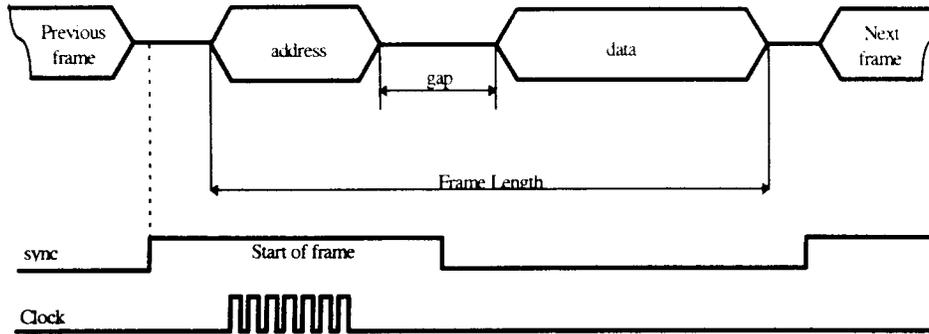


Fig. 7. Timing diagram for the header plus data, and the clock and synchronization signal.

2) *Description of the Super-Pixel:* The functional configuration of one super-pixel is shown in Fig. 6. This architecture encompasses input and output interface circuits ( $I_e$  and  $I_s$ , respectively) an address decoder for each channel, a cyclic priority encoding block piloted by a 6-bit counter and a multiplexer which routes the selected input toward the light modulator acting as the output device for the super pixel. Each super-pixel includes two clock pixels (differential optical signal), 62 input data pixels, two output amplifiers for the modulators, and scan path test logic for monitoring the address decoders and multiplexers. The input and output interface circuits are, respectively, analog receivers and modulator drivers. Because of their importance in optoelectronic hybrid-VLSI technology, they are discussed in more detail in Section IV-B.

Input data at each of the detectors are bit serial and organized into packets of arbitrary but equal length for all the channels. Each packet consists of a header section and a data section. The 7-bit header consists of a flag which specifies a valid address and a 6-bit address ( $A_5 \dots A_0$ ) which identifies the destination of the packet. There is a gap between header and payload (2 clock cycles) to allow additional time for proper multiplexer switching. Each super-pixel has its own address and thus all received packets with an

address that matches are considered for output. However, only the highest priority packet is successfully transmitted to the output modulator. This optically embedded routing mechanism associated with super pixel level arbitration of simultaneous output requests, removes the need for a global electronic control. It also avoids routing over long tracks across the chip and keeps all control signals local to a super-pixel. Another key aspect of this smart pixel architecture is the optical clock distribution to each of the super-pixels. This also avoids global routing across the chip and helps to minimize clock skew, potentially allowing higher clock rates.

The design of the arbitration scheme has been implemented so as not to compromise the performance of the data routing or the address decoding circuitry. An asynchronous arbitration ring, using a cyclic address encoder tree, is chosen over a random priority scheme since it requires less space on the chip and is simpler to test. No provision has been made, on the switching chip, for the buffering of data discarded during arbitration or for feeding back to the input information on the loss of the discarded packets.

A specific external electrical signal (*sync* in Fig. 7) indicates the beginning of an address. It should be noted that it is the only external signal needed to synchronize operation of all the

super pixels. Consequently this signal is distributed over the whole circuit through long tracks but provided the first active clock edge arrives after *sync* has settled at each super pixel there is no problem regarding the propagation delay of this signal. Thus, the frame rate is affected but not the data rate of the payload. Since data transmission is asynchronous, the clock signal is only needed during address decoding phase. This helps in minimizing power consumption of the circuit.

3) *Layout and Packaging of the Chip*: The overall chip ( $14580 \times 15640 \mu\text{m}$ ) has been designed on a  $0.6\text{-}\mu\text{m}$  technology from Austrian Mikro Systems. The core logic of the super pixel is surrounded by horizontal and vertical power supply tracks ( $120 \mu\text{m}$  wide). The chip package is a PGA256 cavity-up carrier. 128 pins are devoted to digital power supply; 18 to digital signals including a global reset signal, a global synchronization signal, and 16 other test signals. 100 pins are devoted to analog power supply and bias signals.

### B. Analog Design of Optoelectronic Receivers

The routing chip uses two types of receiver to amplify the detected photocurrent to a standard digital logic level: a single-ended receiver for the data channels and a differential receiver for the clock channel. The data receiver uses a simple, single-ended, dc-coupled transimpedance design similar to that described in [16]. The data receivers are designed to have a typical power consumption of  $2.5\text{-mW}$  each, giving a total peak power consumption of  $10\text{ W}$  during header decoding. The constraint of a two-level metal silicon process restricted the total width available for power analog supplies to approximately  $40\text{ m}$  per pixel. The voltage drop due to the resistance of the power supply rails between the edge and the centre of the chip placed the primary limit on the receiver supply current. The average power consumption is reduced by selectively disabling receivers during data reception according to whether the packet address matched the super-pixel address.

Electrical tests of a prototype data receiver indicate a minimum sensitivity of  $5\text{-}\mu\text{A}$  peak photocurrent at a data rate of  $100\text{ Mb/s}$  (Fig. 8). The limited operating speed and the pattern-dependent-jitter in the eye diagrams were due to the low transit frequency of the on-chip, long-channel transistor that was used to generate the small input current for electrical testing; calculations predict a roll-off at about  $40\text{ MHz}$ . Simulations indicate that the receiver itself operates to  $200\text{ Mb/s}$ . The receiver sensitivity is limited by the dc offset arising from transistor mismatch rather than thermal noise. Our simulations indicate that the system will operate at a bit error rate as low as  $10^{-12}$ . The design included in the final routing chip was modified to slightly improve sensitivity to  $3.5 \mu\text{A}$ , matching the requirements of the optical power budget.

The clock receiver uses an electrically differential transimpedance receiver (Fig. 9). The two-beam implementation allows a higher bandwidth at the same photocurrent per diode for the clock channel so that it can support a  $250\text{-MHz}$  return-to-zero (RZ) clock waveform (equivalent to a  $500\text{-Mb/s}$  data stream). It also allows the two clock VCSEL's to be biased close to or slightly above threshold to reduce turn-on delay. Two single-ended transimpedance front-ends

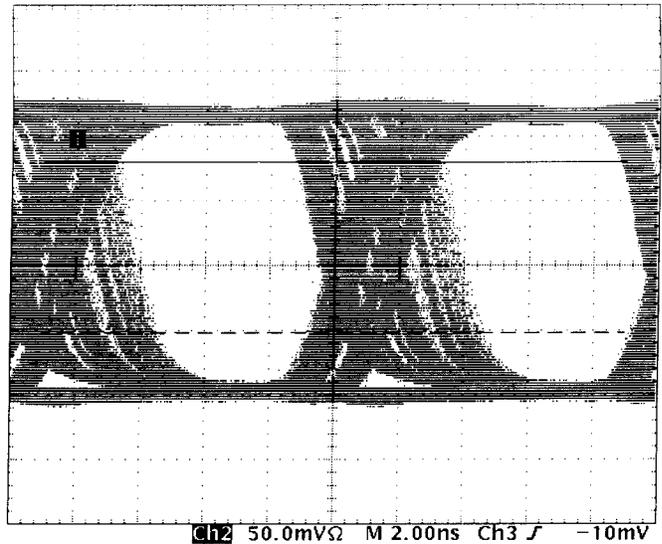


Fig. 8. Eye diagram showing the buffered output of an electrical test version of the data receiver,  $100\text{-Mb/s}$   $5.0\text{-}\mu\text{A}$  peak input current.

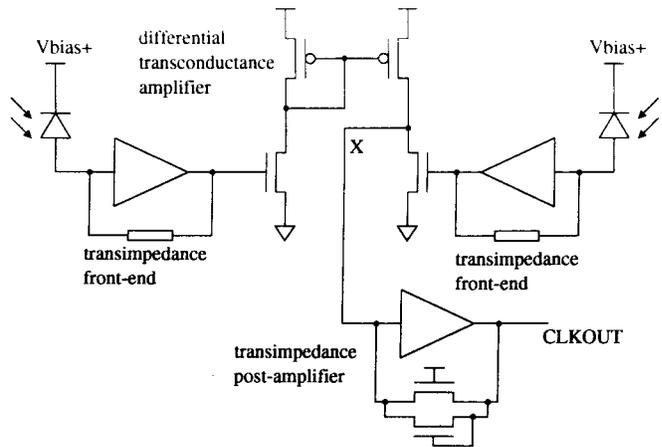


Fig. 9. Simplified schematic of the electrically differential clock receiver circuit with a transconductance-transimpedance postamplifier.

are followed by a differential transconductance amplifier; the currents are subtracted at node *X* and converted to a digital output voltage by a second transimpedance stage. The transconductance-transimpedance postamplifier offers an improved gain-bandwidth product compared to a conventional voltage gain design [17]. A diode-connected clamp transistor [16], in parallel with the feedback resistor of the final transimpedance stage, limits the output swing and prevents the nonlinearity of the feedback transistor from degrading the transient response. The main benefit of the electrically differential approach over the conventional approach to implementing a two-beam receiver [18], which uses two photodiodes connected in series and requires electrically independent n-type and p-type contacts for all photodiodes, is a simplification of the InGaAs fabrication process (see Section V). The receiver circuit also has better immunity to common-mode voltage noise. The cost is a more complex receiver design with higher power consumption and layout area. However, the small

number of clock channels per chip justifies the additional complexity. Simulations indicate operation to 500 Mb/s at a peak photocurrent of  $3.5 \mu\text{A}$  per photodiode but experimental tests were limited in speed by the same problem as the data receiver.

Note that the output chip is clocked using an electrical signal from the word generator (which provides the electrical data input to the system) and that the phase of this signal is adjusted manually to achieve synchronization with the routing chip.

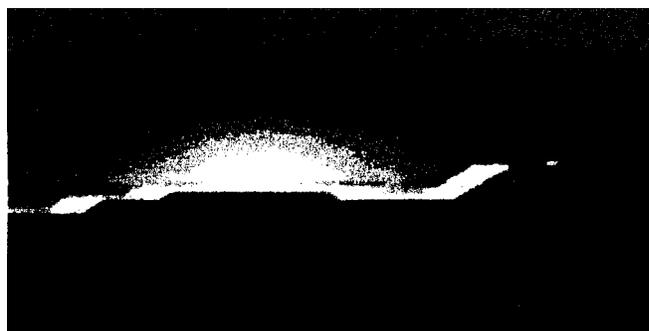
An important design consideration was electrical crosstalk between receivers due to simultaneous switching noise in the analog power supply. Several techniques were used to control crosstalk: approximately 2 pF of gate-oxide decoupling capacitance were included in each pixel to filter the high-frequency supply noise; the decision stage of the receiver circuit, which created most of the switching noise, was given a separate analog power supply to that used by the sensitive front-end and post-amplifier; and a total of 100 external power supply pads were used for the analog supplies to provide acceptably low inductance.

The analog cells have been laid out to fit within a digital standard cell of height  $38 \mu\text{m}$  for ease of integration with the digital logic circuitry. The data receiver occupies a width of  $117 \mu\text{m}$  including flip-chip pads, power supply rails and decoupling capacitors. The clock receiver occupies a width of  $255 \mu\text{m}$ .

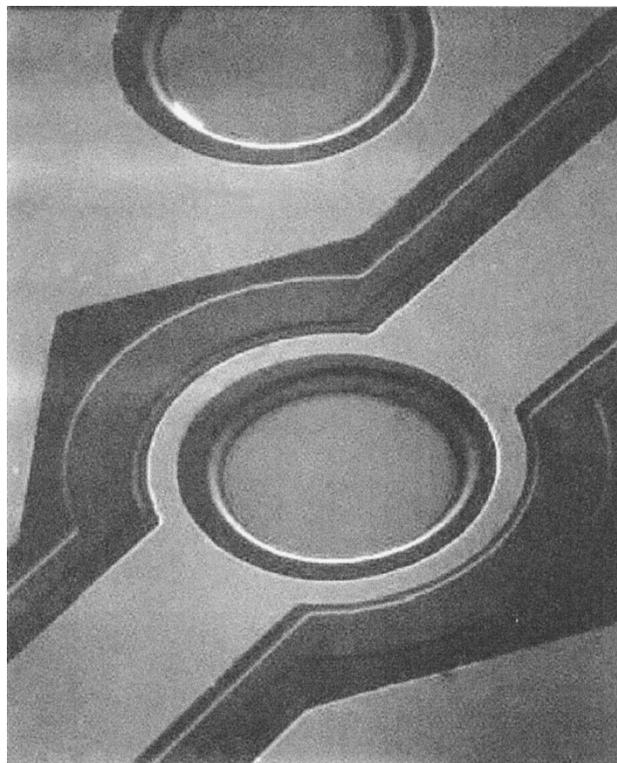
## V. MODULATOR AND PHOTODETECTOR ARRAYS

The III–V semiconductor optoelectronic interface arrays comprise only modulators and detectors. The photodetectors receive the optical inputs and are single ended; that is, a single photodiode is used to detect each channel of information. The optical outputs (modulators) are differential; two diodes are used to “transmit” each channel of information, one carrying the data while the other carries its logical complement. The two diodes in the differential output pair use a common n-type bias voltage and separate digital driver circuits are used to drive the two p-type contacts with the true and complementary data. Compared to the conventional approach of two series-connected modulator diodes, this approach reduces switching noise on the modulator bias voltage, but requires larger silicon driver circuits to sink the total photocurrent through each diode of the pair rather than the difference between the two. The modulator bias voltage is separated from the detector bias to avoid electrical crosstalk and to permit separate optimization.

The arrays are fabricated from In(Al,Ga)As strain-balanced multiple quantum well (MQW) p-i-n structures grown by molecular beam epitaxy (MBE). The structures are deposited on GaAs substrates with an intervening buffer layer  $2\text{-}\mu\text{m}$ -thick containing a linear grade in In concentration. The top p<sup>+</sup>-InGaAs contact layer includes Be  $\delta$ -doping to facilitate the formation of low resistance, nonalloyed ohmic contacts. Fuller details of the MBE grown MQW layers have been described in [19]. The processing of the arrays includes: 1) mesa isolation of the individual devices by a two-step wet chemical etch; 2) liftoff of a sputtered gold film with a bilayer photoresist to form nonalloyed contacts to the detectors and modulators (the



(a)



(b)

Fig. 10. (a) SEM of a section of the finished InGaAs–GaAs optoelectronic device array showing detail of the modulator (see text). (b) Top view of a section of the device array, showing a modulator mesa (center) and one detector (above).

gold film serves the additional purpose of a high-reflectivity mirror on the modulators); 3) trench isolation of the lower n<sup>+</sup> contact layer to disconnect electrically the modulators and detectors; and 4) overall passivation with PECVD SiO<sub>2</sub>. Fig. 10(a) shows a scanning electron micrograph of a cross section through an array. The isolation trench is located on the left hand side of the picture, the n<sup>+</sup> metallization is left of centre, a detector mesa is on the right, while the overall SiO<sub>2</sub> passivation layer is also clearly visible. Fig 10(b) shows a top view of modulator (middle) and detector mesas with the isolation trench clearly visible. Test diodes fabricated as part of an array indicate turn-on voltages around 0.8 V and reverse saturation currents of less than 10 nA for a mesa with a diameter of  $\sim 30 \mu\text{m}$ .

The modulators used in the demonstrator system are designed to operate with the available 5 V. However, there is a clear trend to decreasing voltages being used in the underlying Silicon CMOS, and it would be very desirable to remain compatible with these voltages. Thus modulator design at lower voltages is an important issue, and is also being pursued [20]. The basic physics of the quantum-confined Stark effect determines the electric fields required to change the absorption of a given material (InGaAs MQW's in this case). Thus to reach the same fields with lower voltage requires that the thickness of the region over which the voltage is dropped to be decreased, effectively decreasing the number of QW's. One approach to accommodating this decrease is to make better use of the available absorption by incorporating the active region in an optical cavity [21]. This can be achieved in these devices by incorporating a Bragg mirror stack between the substrate and the diode structure, forming an optical cavity with the back metal mirror. We have modeled the optimum combination of mirror reflectivity and number of quantum wells for different voltages [20]. As the voltage decreases the number of wells is decreased, with an increase in the mirror reflectivity to counteract the loss of absorbing material. The major limitation of this approach is one of device manufacture. For correct operation the wavelength of the absorption peak of the MQW material must be accurately positioned with respect to the resonant wavelength of the optical cavity, which is determined by the cavity length. Modern MBE growth can achieve accuracies of  $\sim 1\%$ . Modeling suggests this would be sufficient to grow devices for the low finesse cavities required for 3.3 V or perhaps 2-V operation, but would be very problematic for operation at lower voltages. To circumvent this problem we are investigating the possibility of postgrowth etching of the cavity thickness to tune the cavity resonance wavelength. More immediately, we are also harnessing this approach to obtain improved modulation performance with the existing 5-V electrical drive.

## VI. VCSEL ARRAY AND PRINTED CIRCUIT BOARD

The demonstrator switching system includes an  $8 \times 8$  VCSEL array to provide the input signals. The fabrication of the array of VCSEL's and their drive circuits are described in this section.

### A. VCSEL Structure

The overall design of the VCSEL's is shown in Fig. 11 and is based on dislocation-free strained AlAs–GaAs–InGaAs heterostructures. The MOVPE-grown VCSEL's are designed for top emission at 960 nm and consist of 30.5 pairs of  $\lambda/4$  thick  $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$  and GaAs layers for the bottom Bragg mirror and 22 pairs for the top mirror structure. In order to reduce the electrical resistance of the Bragg mirror structure, each interface is linearly graded over a region of 30 nm. To reduce the free carrier absorption, the doping level is increased in the region with low intensity of the standing optical wave and decreased in regions of high light intensity. The total length of the cavity is 270 nm including three central 8-nm-wide  $\text{In}_{0.13}\text{Ga}_{0.87}\text{As}$  quantum wells separated by 10 nm wide

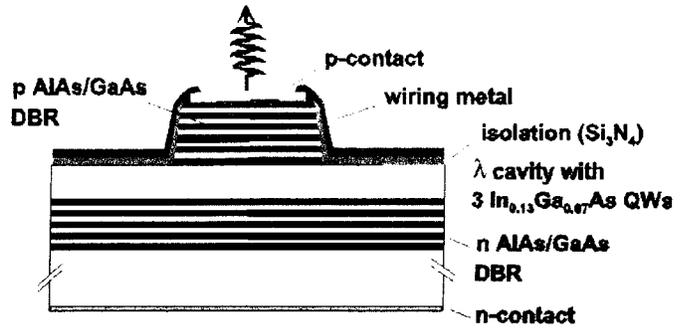


Fig. 11. Schematic cross section of the VCSEL design used for the  $8 \times 8$  optical input array.

GaAs barriers. A  $\lambda/2$  thick GaAs contact layer concludes the structure. The individually addressable  $8 \times 8$  (square) arrays were processed on quarter 2-in. wafers. The pitch is  $250 \mu\text{m}$  and the overall size of each array, including bonding pads, is  $3 \times 3 \text{ mm}^2$ . The VCSEL's have  $10\text{-}\mu\text{m}$  circular aperture diameter. The measured capacitances of the centre VCSEL (of longest wiring) and border VCSEL (of shortest wiring) are calculated to be 3.05 pF and 1.05 pF, respectively.

### B. Electrical and Optical Characteristics

The DC electrical and optical characteristics of the VCSEL array bonded onto their PCB are shown in Fig. 12. The mean threshold current is  $2.6 \pm 0.05 \text{ mA}$ , the mean threshold voltage is  $1.9 \pm 0.01 \text{ V}$  and the output power at 8 mA is  $1.25 \pm 0.02 \text{ mW}$ . The power conversion efficiency is  $6.3 \pm 0.1\%$ . For this chosen array, all the 64 VCSEL's are lasing (100% yield) with an emission wavelength of 956 nm and a maximum wavelength variation across the array of  $\Delta\lambda_{\text{max}} = 0.7 \text{ nm}$  at 8 mA of input current. The additional wavelength variation when all VCSEL's are operated simultaneously is expected to be  $\Delta\lambda_{\text{max}} = 1.1 \text{ nm}$ , which corresponds to an estimated temperature increase of 17 K, that is caused by a dissipated power of around 600 mW. These wavelength variations are within the tolerance acceptable to the diffractive optical elements.

High-frequency operation of the VCSEL array prebiased at 1.9 V threshold, bonded onto the PCB, was tested with data rates up to 500 Mb/s. Fig. 13 shows the resulting eye diagram measured on an HP54750A digitizing oscilloscope. The eye is clearly open which demonstrates that data rates above 500-Mb/s nonreturn-to-zero (NRZ) are possible with this VCSEL/driver/PCB subsystem. Even without any prebias, the transfer of 250-Mb/s signals is possible. In this case the turn-on delay is 1.6 ns with an estimated maximum contribution of 0.7 ns from the PCB/driver subsystem. The electrical crosstalk can be a potential source for errors when many VCSEL's on the PCB/driver assembly are operated simultaneously, however this was found to be negligible. The measured optical intensity fluctuations induced by the modulation of one VCSEL on the output power from a neighboring VCSEL operated at a constant current of 8 mA was measured to be below 10% and further measurements show that the observed crosstalk originates from the parallel

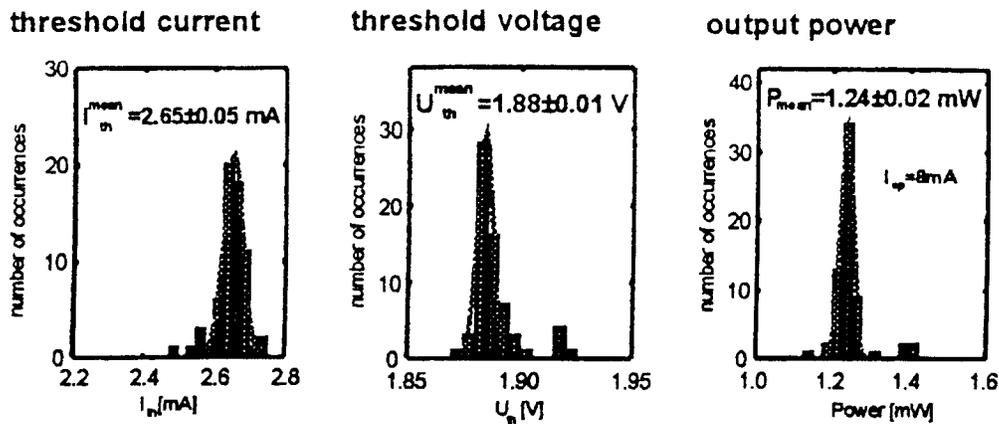


Fig. 12. Electrical and optical characteristics of the VCSEL array, as bonded onto the PCB.

TABLE III  
TARGET SPECIFICATIONS OF THE  $8 \times 8$  VCSEL ARRAY REQUIRED FOR THE DEMONSTRATOR  
AND OPERATING CHARACTERISTICS OF THE ARRAY MOUNTED IN THE PCB/DRIVER SUBSYSTEM

	Target Specification	VCSEL Array for Demonstrator	Best Result
$\Delta\lambda$	< 1%	< 0.1%	< 0.017%
$P_{\max}$	> 1 mW	> 2.4 mW	> 4.5 mW
$I_{\text{th}}$	< 8 mA	2.6 mA	1.0 mA
$V_{\text{th}}$	< 3V	1.9V	1.4 V
$f_{\text{mod}}$	>250 Mbit/s	500 Mbit/s	>3 Gbit/s small signal
yield	>90% within array	100%	100%

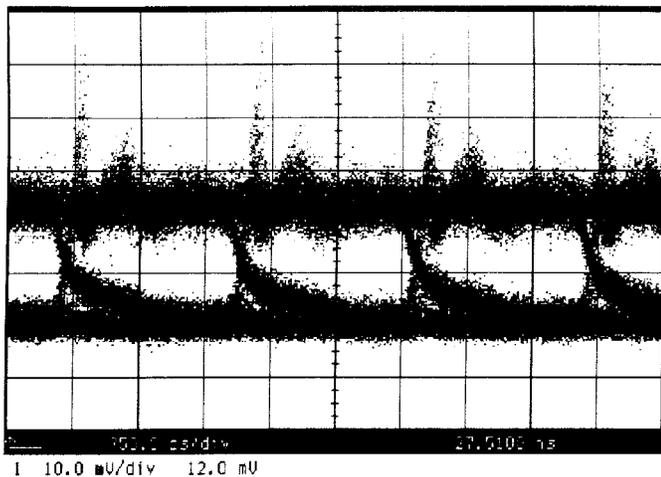


Fig. 13. Eye diagram of the VCSEL/PCB subsystem operated at 500-Mb/s NRZ.

wiring on to PCB. Since the chosen VCSEL had the longest parallel wiring on the driver PCB and VCSEL array, these measurements represent the worst case. Table III summarizes the target specifications and the measured characteristics of the VCSEL array in the PCB/driver subsystem. The assembly exceeds all of the system specifications.

The fabrication of larger, and/or more dense, VCSEL arrays may require close integration with external silicon drive circuits by such techniques as flip-chip bonding to minimize crosstalk between the power lines to each device. Such integra-

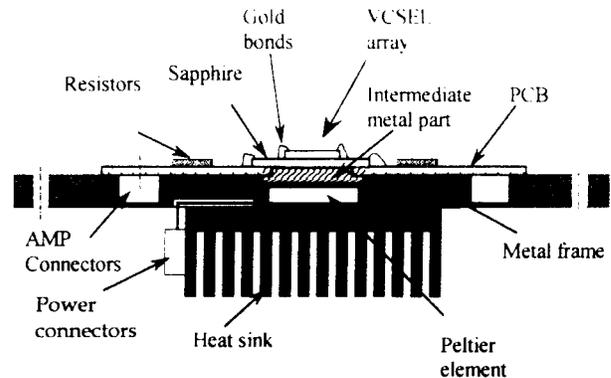


Fig. 14. Cross section showing the VCSEL/PCB subsystem, including the heatsink and mounting arrangement.

tion is being actively explored for possible future exploitation by a number of research groups.

### C. PCB and VCSEL Drivers

The VCSEL array is mounted on an intermediate sapphire substrate, itself fixed on the PCB, as shown in Fig. 14. To design the circuitry on the PCB, the VCSEL is modeled as a  $105\text{-}\Omega$  resistance at the current versus voltage ( $I$ - $V$ ) operating points (2.4 mA, 1.85 V) and (8.0 mA, 2.44 V). Using this model, a simple passive impedance two-port network has been designed to provide a match between the specified  $50\text{-}\Omega$  digital signal generator and the VCSEL load. This gives a compromise between maximum bandwidth and a minimum

sensitivity to the dispersion in the VCSEL characteristics over the array. The PCB is 109 mm long and 62 mm wide and is attached to the slotted baseplate by means of an adjustable mount. If we assume that 0 and 1 have the same probability of appearing in the signals, the heat dissipation is 0.77 W for the VCSEL array and 6.14 W for the PCB (6.91-W total). In the worst case (maximum dissipation, each diode emits all the time) we expect 1.25 W for the VCSEL array and 8.50 W for the PCB (9.75 W total). We have designed a heat sink that locates close to the back plane (= ground plane) of the PCB. A temperature sensor (PT100) is included in order to achieve feedback and be able to regulate the temperature. This is accomplished with the aid of a Peltier element incorporated into the heatsink.

## VII. CONCLUSION

The system demonstrator described here brings together the full set of technologies required to take advantage of the potential of free-space optical interconnects. Detailed designs of all components have been completed and this permits us to draw some important conclusions.

Firstly, we have shown the feasibility of operating an optoelectronic system incorporating an optical input to a single silicon chip in the terabits per second domain. The designed system not only considers the hybrid OE-VLSI chip itself, as has already been investigated by other researchers, but also includes a practical infrastructure whereby the full performance can be demonstrated and assessed. As a design process alone this has proven to be an extremely valuable exercise, in advance of the later phase of this work in which experiments will aim to confirm the predictions of the various simulations.

Secondly, this study has acted as a driver for a number of important optoelectronic and optical technologies. An  $8 \times 8$  VCSEL array capable of providing a 16-Gb/s electronic-to-optical interface has been developed and has been measured as satisfying numerous other system requirements, particularly with respect to array uniformity. New microoptical and diffractive optical elements have been fabricated along with compound lenses designed to handle large arrays of optical signals over the required fields of view ( $\sim 18$  mm). Novel beam-splitters have been designed and successfully tested; and the challenge of providing a compact stable optomechanical assembly has been addressed. The development of our InGaAs modulator arrays has permitted the evaluation of improved (simplified) fabrication processes, suited to arrays of this size.

Finally the various constraints imposed by distributing optical interfaces across a conventional CMOS chip have been addressed. This latter has led to the development of low-power receivers with novel designs and a study of the impact of embedding large numbers of such sensitive analog circuits with digital microelectronics. From this, we have concluded that the major factors limiting the communication capacity of this optoelectronic interconnect system are the constraints associated with the receiver designs. Combining sensitive analog electronics with digital circuitry in such close proximity is always going to be a challenge. In this system, with the

limitation of using only a two-metal silicon process, the need to minimize: 1) voltage drop along the receiver power supply rails and 2) switching noise appearing on the analog power supply has proven particularly problematic. However, these are not fundamental difficulties and the use of present generation CMOS technology, with multiple metal layers and substantially smaller feature sizes, immediately remove these constraints. Another parameter that is greatly improved by the move to silicon with smaller feature sizes is the receiver power dissipation. In the designed system, the power dissipated by each receiver was  $\sim 2.5$  mW, corresponding to an overall power demand of  $10 \text{ W (Tb/s)}^{-1}$ . This was close to the limit of what could be easily dissipated. A study of the impact of size scaling on power consumption [22] has shown that as feature sizes drop toward  $0.1 \mu\text{m}$  so the electrical power consumption of the receivers also drops, giving the prospect for optical input at the level of  $0.3 \text{ W (Tb/s)}^{-1}$  although, beyond this point, physical limitations on transistor performance will limit further improvement in this metric. Similar studies by other authors support this trend [23], [24]. It is worth noting that the operating speed per channel scales in line with the decreasing technology size even if there is no further improvement in photodiode capacitance from the values quoted above. A likely future implementation of a 1-Tb/s interface in a  $0.1\text{-}\mu\text{m}$  technology would be in the form of 256 channels of 4 Gb/s per channel. A system with 4096 channels, such as the one described here, is therefore potentially capable of significantly higher bandwidths. The detailed study referred to above [22] indicates that the performance of the electronic receiver is unlikely to be the limiting factor for bandwidths well in excess of 1 Tb/s. This illustrates one of the attractive features of using optical techniques to solve the interconnect problems of the future.

Another parameter that will increase with time is clock frequency. The SIA Roadmap [1] predicts off-chip data rates for application-specific integrated circuits to rise to over 1.5–3.0 GHz by 2012. This is well within the capability of the optoelectronic interface devices developed as part of this study. The desire to communicate off-chip at whatever clock frequency the silicon is operating can not only be satisfied by these optical methods but becomes progressively easier to satisfy as the silicon technology itself improves.

The system that we have developed as a focus for this research, corresponding to the switching fabric of a crossbar interconnect, is not intended to be a complete architecture in its own right. Nonetheless, the completion of its design and the assessment of the critical components illustrates the manner in which the enormous capacity of free-space optical interconnects might be exploited in realistic high-performance systems of the future.

## ACKNOWLEDGMENT

The authors acknowledge the contributions made by A. J. Waddie, G. R. Smith, and N. Ross to this paper. In addition, the authors would like to thank their colleagues in the other projects of the European Commission MEL-ARI OPTO Cluster for useful discussions.

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Following a year as a Visiting Researcher at Hitachi Central Research Laboratories, Tokyo, Japan, he returned to join the staff of the Hitachi Dublin Laboratories at Trinity College. In 1997, he joined the Dublin Institute of Technology as Assistant Head of the School of Physics where he continues to pursue interests in optical computing, optical interconnects and Fabry-Perot modulators in association with staff at Trinity College.



**Declan Byrne** was born in Carlow, Ireland, on August 11, 1973. He received the B.Sc degree in experimental physics from University College, Dublin, Ireland, in 1996, and is currently working toward the Ph.D. degree in physics from Trinity College, Dublin, and is funded by a Forbairt research scholarship and ESPRIT.

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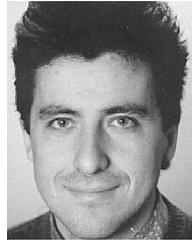
From 1977 to 1980, he was with the Solid State Spectroscopy Group at the University of Wisconsin, Madison. From 1980 to 1986 he was Member of the Technical Staff, AT&T Bell Laboratories, Murray Hill, NJ, where he performed research in optical semiconductors, glasses, optical fibers and magneto-optical waveguides. In 1986, he became Professor of Laser Physics, Trinity College, Dublin, Ireland, where he is also head of Semiconductor Optoelectronics Group. His current research activities include spontaneous emission processes in semiconductor microcavities, optical computing and optical neural networks, excitons in wide bandgap II–VI quantum structures, lasing action II–VI materials, semiconductor diode laser physics and new applications. In 1989, he became Technical Director, Optronics Ireland, the Irish National Research Programme in Optoelectronics and from 1992–1995 served as Head of Department of Physics, Trinity College, Dublin, Ireland. Since 1996, he has been Dean of Research at Trinity College.

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His graduate research work involved the design, processing and characterization of GaInP–AlGaInP DFB lasers.

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After joining the Paul Scherrer Institut, Zurich, Switzerland, he worked on the development of vertical-cavity surface-emitting lasers and integrated optoelectronic integrated circuits for applications in sensors, biochemical analysis, and optical interconnects. His expertise includes epitaxial growth, semiconductor processing and laser physics. Over 50 technical publications and three patents have accompanied this work. He is head of the Optoelectronic Device Section at the Centre Suisse d’Electronique et de Microtechnique SA (CSEM) in Zurich, Switzerland.