

High-Mobility Flexible Transistors with Low-Temperature Solution-Processed Tungsten Dichalcogenides

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ABSTRACT: The investigation of high-mobility two-dimensional (2D) flakes beyond molybdenum disulfide (MoS_2) will be necessary to create a library of high-mobility solution-processed networks that conform to substrates and remain functional over thousands of bending cycles. Here we report electrochemical exfoliation of large-aspect-ratio (>100) semiconducting flakes of tungsten diselenide (WSe_2) and tungsten disulfide (WS_2) as well as MoS_2 as a comparison. We use Langmuir–Schaefer coating to achieve highly aligned and conformal flake networks, with minimal mesoporosity ($\sim 2\text{--}5\%$), at low processing temperatures ($120\text{ }^\circ\text{C}$) and without acid treatments. This allows us to fabricate electrochemical transistors in ambient air, achieving average mobilities of $\mu_{\text{MoS}_2} \approx 11\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, $\mu_{\text{WS}_2} \approx 9\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, and $\mu_{\text{WSe}_2} \approx 2\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ with a current on/off ratios of $I_{\text{on}}/I_{\text{off}} \approx 2.6 \times 10^3$, 3.4×10^3 , and 4.2×10^4 for MoS_2 , WS_2 , and WSe_2 , respectively. Moreover, our transistors display threshold voltages near $\sim 0.4\text{ V}$ with subthreshold slopes as low as 182 mV/dec , which are essential factors in maintaining power efficiency and represent a 1 order of magnitude improvement in the state of the art. Furthermore, the performance of our WSe_2 transistors is maintained on polyethylene terephthalate (PET) even after 1000 bending cycles at 1% strain.

KEYWORDS: electrochemical exfoliation, tungsten dichalcogenides, solution processing, transistors, Langmuir–Schaefer deposition



While electronic devices have traditionally been rigid, there is now a need for electronic components to conform to flexible substrates, while maintaining manufacturability in scale, to address new application areas in the automotive, healthcare, consumer electronics, and wearable electronics sectors.¹ For example, flexible transistors are required for use in active matrix displays, sensors, and integrated circuits in many of these sectors.^{2,3} Solution processing of transistors has emerged as a method to manufacture flexible transistors using semiconducting inks, offering a broad material selection and considerable versatility, alongside low cost and reduced energy consumption over growth-based techniques. Over the past few decades, semiconducting inks of carbon nanotubes, organic polymers, and metal oxides have been studied. However, all have struggled to achieve transistor mobilities (μ) much beyond $10\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at room temperature and in the ambient atmosphere required for digital electronics.^{2,4}

2D flakes such as transition-metal dichalcogenides (TMDs) offer a route to exceed state-of-the-art transistor performances

due to their high intrinsic mobility, $\mu > 50\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, reasonable stability under ambient conditions, and conformability to flexible substrates.^{5,6} Semiconducting inks of 2D flakes can be mass-manufactured by liquid-phase exfoliation (LPE) using techniques such as shear mixing or ultrasonication and deposited into networks of 2D flakes.⁷ However, achieving high- μ networks from LPE is challenging due to their relatively large flake thickness (up to 20 nm) and small lateral size (tens to hundreds of nanometers),⁸ which results in an unoptimized morphology (i.e., poor packing and alignment) on deposition.⁹ Furthermore, despite high mobility in the basal plane of the LPE 2D flakes,¹⁰ the network mobility has typically been limited by the interflake junctions,⁹ which can result in large

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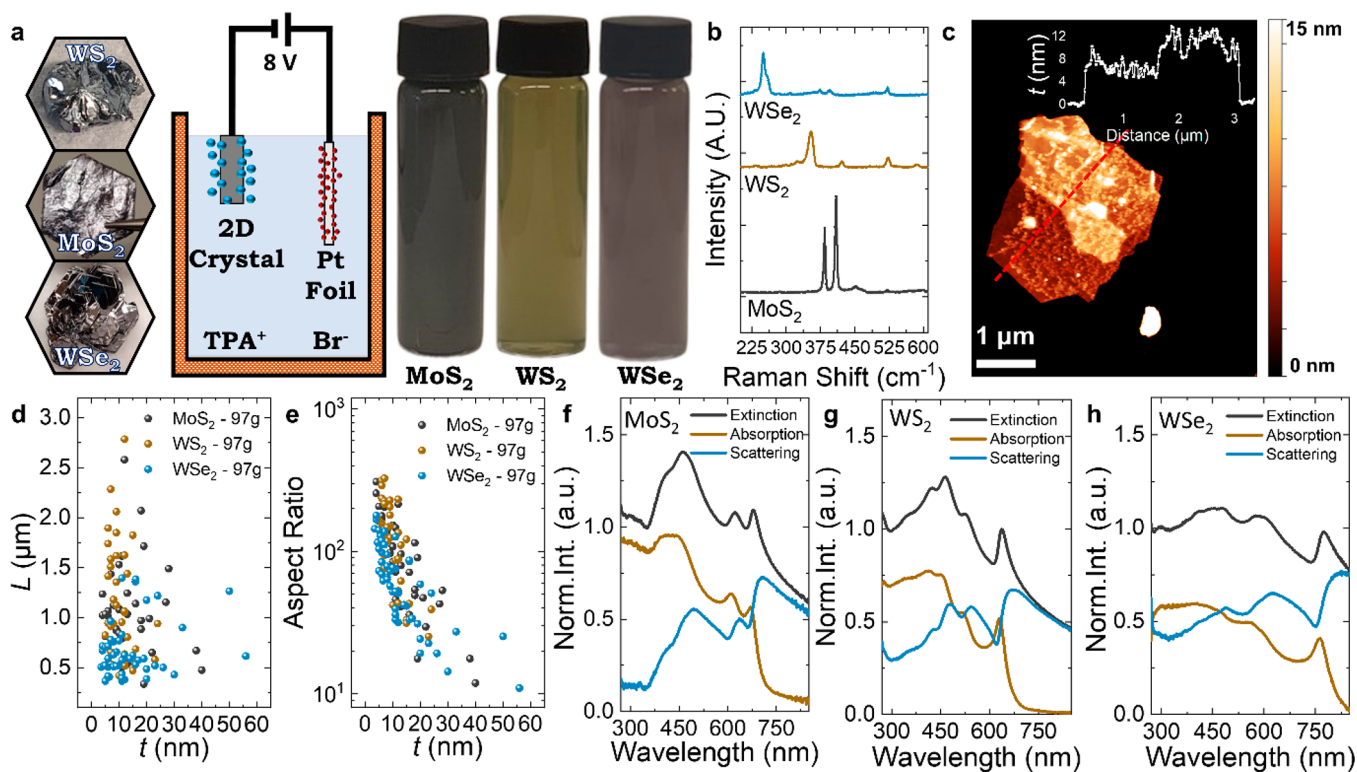


Figure 1. Electrochemical exfoliation of TMDs and their characterization. (a) Pictures of the bulk TMD crystals used for the electrochemical exfoliation, schematic of the intercalation with TPA^+ cations and the resulting semiconducting inks after centrifugation. (b) Chemical analysis by Raman spectroscopy of the TMD flakes after exfoliation. (c) Atomic force microscopy micrograph of a MoS_2 flake after centrifugation (97g). (d, e) Atomic force microscopy statistics of the flake AR and L and a function of the flake t . (f–h) Normalized optical characterization of the TMD inks by UV–vis showing the extinction, absorption, and scattering components as a function of wavelength shone through the ink.

hopping activation energies, $E_a > 300$ meV,¹¹ leading to low μ in the range $0.01\text{--}0.3$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$.^{10,12–14}

Electrochemical exfoliation (EE) with quaternary ammonium molecules has emerged as an alternative route toward large 2D flakes, $L > 1$ μm , with a low $t < 10$ nm, which permits conformal junctions,⁹ reducing junction resistance (i.e., the electrical resistance at the interface between flakes) and E_a (< 100 meV).^{3,11} To maximize network μ the flakes need to be conformal to each other and aligned (i.e. the network mesoposity should be minimized $< 5\%$).⁹ Deposition techniques which can help to align flakes, such as spin coating¹⁵ or Langmuir–Blodgett,¹⁶ have been used with EE MoS_2 flakes on rigid Si/SiO₂ to increase the transistor μ value to $1\text{--}8$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. However, in many cases, strategies such as acid treatment^{15,17,18} (e.g., bis(trifluoromethane)sulfonimide) or high-temperature annealing (> 200 °C)^{3,11,18,19} are required to remove flake stabilization agents such as poly(vinylpyrrolidone) (PVP) or remove unintentional doping.²⁰ Unfortunately, these strategies are typically incompatible with most flexible substrates, which require processing temperatures < 120 °C to avoid deformation.² The measurement of devices under vacuum ($< 10^{-6}$ mbar)^{10,13,17,21} or with passivation layers (e.g., aluminum oxide)²² has also been used to help reduce charge carrier scattering and thus ensure device $\mu > 0.1$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. However, vacuum processes can hinder applicability in a commercial environment, while passivation layers add additional complexity to the manufacturing process. Therefore, a protocol to yield high-mobility devices ($\mu > 1$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$) that is compatible with flexible substrates and

operational in ambient air without vacuum measurement, passivation layers, or acid treatments would be highly desirable. Furthermore, high- μ networks with TMDs have so far only been achievable with networks of MoS_2 flakes despite the abundance of TMDs available to explore. Moreover, high $\mu > 1$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ networks of 2D flakes that go beyond MoS_2 on a flexible substrate and in ambient air have not yet been achieved.

This work will utilize Langmuir–Schaefer deposition²³ to explore flake networks of EE, WS_2 and WSe_2 (and MoS_2 for comparison purposes), with minimal ink usage (< 20 μL). Due to the high flake alignment and high aspect ratio (> 100) the flakes have conformal junctions with minimal interflake junction resistance and therefore high μ on both Si/SiO₂ and flexible PET in ambient air and without acid treatments or high-temperature annealing (> 120 °C).

RESULTS AND DISCUSSION

TMD Ink Production and Characterization. We use EE to intercalate and expand 2D bulk crystals of MoS_2 , WS_2 , and WSe_2 as shown in Figure 1a. Next, the intercalated TMD crystal is ultrasonically treated with PVP in DMF, centrifuged at 97g, and then solvent-exchanged into IPA after washing (see Methods) to form our MoS_2 , WS_2 , and WSe_2 semiconducting inks (Figure 1a). The centrifugation washing is a key step to remove the residual PVP without annealing and ensure that the inks will be compatible with low processing temperatures of < 120 °C. Raman spectroscopy is utilized to monitor TMD flake quality after exfoliation. Figure 1b depicts the spectra of

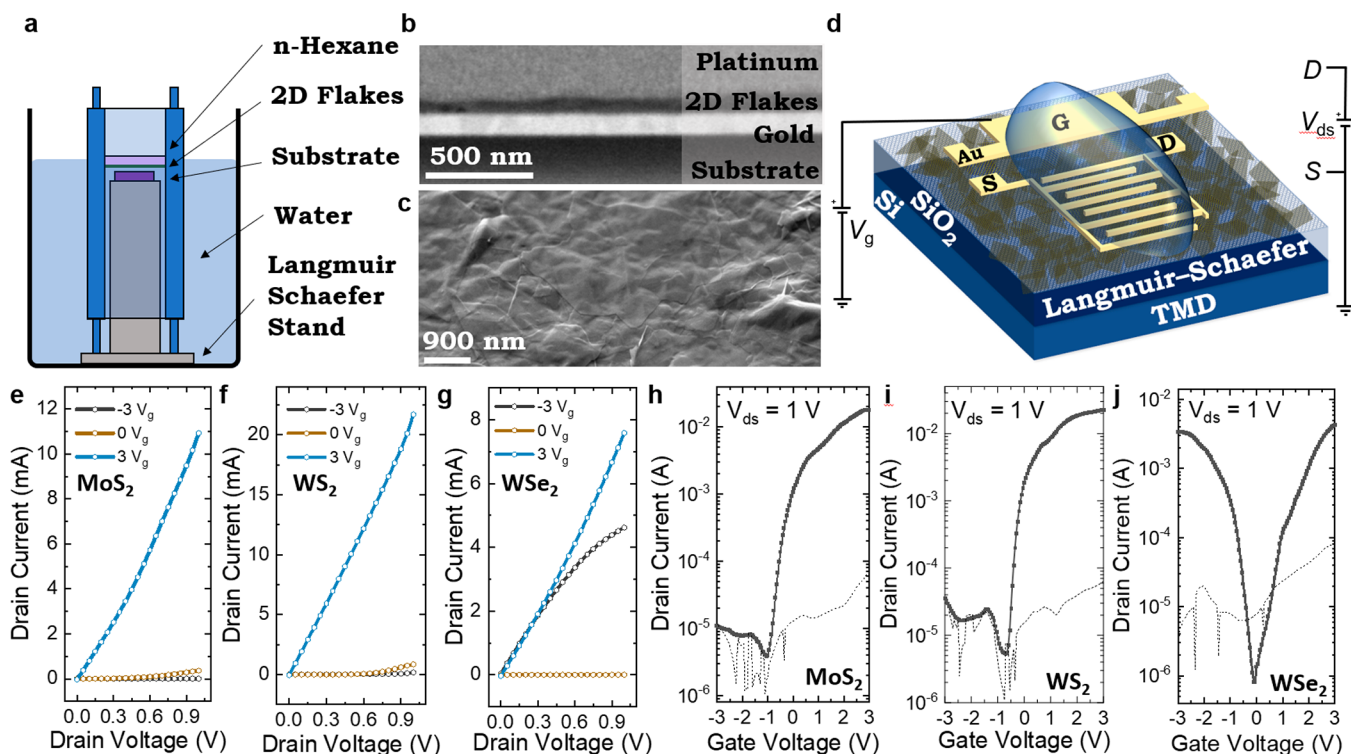


Figure 2. Experimental setup and electrical properties of the Langmuir–Schaefer electrochemical transistor on Si/SiO₂. (a) Schematic of the Langmuir–Schaefer deposition setup. (b) Cross-sectional SEM of a highly aligned LS network on quartz with $t_c \approx 60$ nm. (c) Scanning electron microscopy image of a LS-deposited MoS₂ network showing conformal junctions between flakes and folded MoS₂ flakes (top). Scale bar: 1 μ m. (d) Sketch of the Langmuir–Schaefer TMD electrochemical transistor where S is the source and D is the drain (bottom). Output curves of the (e) MoS₂ transistor, (f) WS₂ transistor, and (g) WSe₂ transistor where I_d is measured as a function of V_{ds} (using V_g ranging from -3 to 3 V with a step change of 3 V). Transfer curves of the (h) MoS₂, (i) WS₂, and (j) WSe₂ transistors where I_d is measured as a function of the applied V_g (black curve). For each set of devices, $V_{ds} = 1$ V is used. I_g is also measured as a function of the applied V_g (dashed black curve).

the MoS₂ (black), WS₂ (brown), and WSe₂ (blue) flakes and are consistent with previous reports of 2H semiconducting flakes since the J₂ and J₃ vibrational modes attributed to the metallic 1T phase are not observed (Supplementary Note 1 and Supplementary Figure 1a mark the absent peaks).^{24–26}

Atomic force microscopy (AFM) statistics are used to estimate the lateral flake size (L) and apparent flake thickness (t) of the MoS₂, WS₂ and WSe₂ flakes on Si/SiO₂ substrates. Figure 1c is an AFM micrograph of a MoS₂ flake with an associated cross section, while Figure 1d plots L versus t for individual flakes with no apparent correlation, which is unlike the case for LPE flakes (Supplementary Figure 1b).⁸ The average flake lengths, $\langle L \rangle$, were 1.0 ± 0.1 , 1.2 ± 0.1 , and 0.67 ± 0.05 μ m, while the average apparent flake thicknesses, $\langle t \rangle$, were 14 ± 1 , 10.5 ± 0.7 , and 14 ± 1 nm for MoS₂, WS₂, and WSe₂ flakes, respectively. Plotting the flake aspect ratio (AR, L/t) versus t in Figure 1e shows maximum AR values of 309, 326, and 177 for MoS₂, WS₂, and WSe₂ flakes, respectively, with means of 102, 132, and 70. These values are significantly higher than ARs achieved with LPE by ultrasonication (AR ≈ 10 –40),^{8,27} shear mixing (AR ≈ 4 –40, Supplementary Note 1), cyclic shear mixing (AR ≈ 60)²⁸ or microfluidization (AR ≈ 50).²⁹ AR > 40 is required to make conformal flake-to-flake junctions to minimize the junction resistance to improve the device performance.⁹ It is known that the ratio of the in-plane-tearing energy to the out-of-plane-peeling energy determines the aspect ratio of liquid exfoliated flakes, as the former parameter controls the lateral size while the latter controls the

nanosheet thickness.⁸ In electrochemical exfoliation, ion insertion is thought to reduce the peeling energy, thus increasing the aspect ratio.

In Figure 1f–h UV–visible optical absorption spectra of the MoS₂, WS₂, and WSe₂ inks are taken with an integrating sphere to isolate the extinction, absorption, and scattering components of the TMD inks.³⁰ The normalized spectra of the MoS₂, WS₂, and WSe₂ inks display excitonic transitions, around 679 and 623 nm for MoS₂,³¹ 638 and 526 nm for WS₂, and 775 and 579 nm for WSe₂, attributed to the A exciton and B exciton, respectively, consistent with previous reports of LPE and mechanically exfoliated flakes.^{30,32,33} The spectral profiles are consistent with size measurements by AFM (Supplementary Note 2).³⁴

Electrochemical Transistors with TMD Networks. We use Langmuir–Schaefer (LS) coating (Figure 2a) to fabricate TMD networks on Si/SiO₂ wafers with our MoS₂, WS₂, and WSe₂ inks. The interfacial tension at the hexane/deionized water interface creates highly aligned networks after solvent removal with minimal ink wastage of <20 μ L (see Methods). As shown in Figure 2b, we used a focused ion beam to cut and polish a cross-section of an MoS₂ network made by the LS deposition process, which was then imaged using SEM. The cross sections appear largely featureless, implying the film to be near-monolithic. An image analysis³⁵ showed this network to contain 2–5% mesopores (i.e., those larger than 5 nm in size—smaller pores are below the resolution of this measurement). This is significantly lower than for poorly aligned,

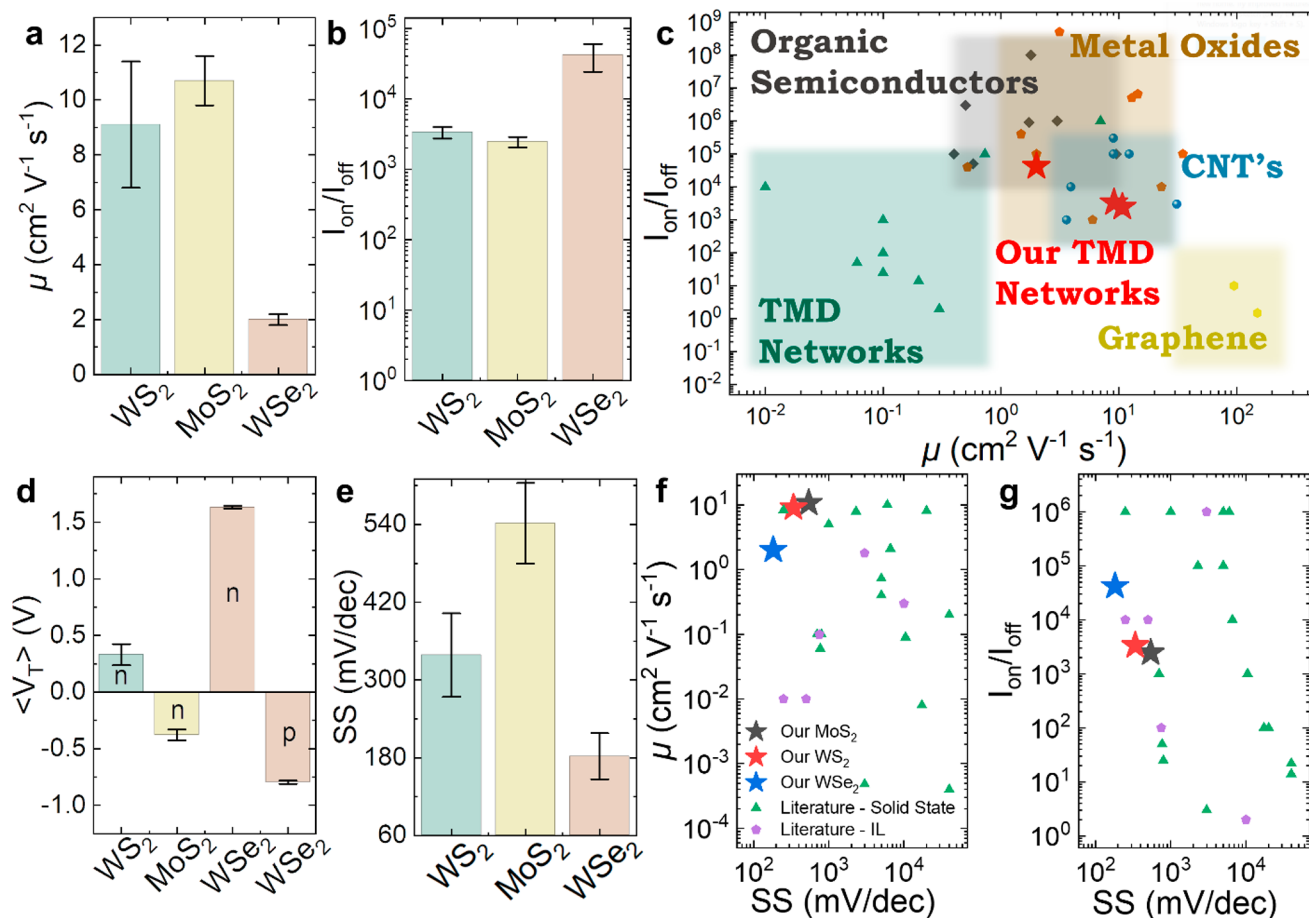


Figure 3. Device performance compared to previous scientific literature. (a) Our transistor μ values for WS_2 , MoS_2 , and WSe_2 . (b) Our $I_{\text{on}}/I_{\text{off}}$ ratios for WS_2 , MoS_2 , and WSe_2 . (c) Our μ values and $I_{\text{on}}/I_{\text{off}}$ ratios (red stars) compared to those of other TMD networks (green triangles), organic semiconductors (black squares), metal oxides (orange pentagons), carbon nanotubes (blue circles), and graphene networks (yellow hexagons). (d) The device $\langle V_T \rangle$ and (e) subthreshold slope for WS_2 , MoS_2 , and WSe_2 . (f) The μ and (g) $I_{\text{on}}/I_{\text{off}}$ ratio performance plotted as a function of the subthreshold slope for our electrochemical WS_2 , MoS_2 , and WSe_2 transistors and compared in more detail to TMD networks for solid-state (green triangles) and ionically gated (purple pentagons) devices. Error is calculated by SDOM in this figure.

spray-coated nanosheet networks ($P_{\text{net}} \approx 0.3\text{--}0.6$),^{10,35} implying LS-deposited films are compact and consist of basal-plane-aligned nanosheets with adjacent sheets lying conformal to each other.⁹ In Figure 2c top-surface SEM imaging of an MoS_2 network also shows excellent flake alignment in the plane of the film and conformal interflake junctions, implying a low junction resistance and E_a .^{9,11} We also observe folds and wrinkles in the MoS_2 flakes (also identified with TEM, Supplementary Note 3), implying high flake flexibility which we have previously linked to the formation of conformal junctions.⁹ Gold electrodes (~ 100 nm thick) are deposited by evaporation (Temescal FC-2000) through a stainless-steel mask, creating source and drain electrodes with width $W \approx 11$ nm and channel length $L_c \approx 50$ μm onto networks of MoS_2 , WS_2 , and WSe_2 . A side gate of ~ 1.5 mm \times 4 mm is also patterned ~ 1 mm from the source and drain electrodes (Supplementary Note 4). The devices were then annealed again at 120 $^\circ\text{C}$ for 1 h in an inert N_2 environment. AFM measurements (see Methods) reveal a network thickness (t_c) of $\sim 25\text{--}40$ nm (Supplementary Note 3) for our devices. To complete our electrochemical transistor, shown in Figure 2d (bottom), we add the drop-cast ionic liquid 1-ethyl-3-methylimidazolium bis-

(trifluoromethylsulfonyl)imide (EMIM TFSI) to allow gating of the semiconducting channel.³⁶

Next, we characterize the electrochemical transistors using a probe station at atmospheric pressure and temperature and in ambient air. For the MoS_2 , WS_2 , and WSe_2 (Figure 2e–g) devices, we measure the output characteristics at gate voltages of 3, 0, and -3 V. These curves are consistent with MoS_2 and WS_2 being n-type,^{3,13} as the devices switch on at positive V_g (as seen by a drop in drain current, I_d , to <0.1 mA). The WSe_2 transistor remains on at -3 V_g and 3 V_g and is only off ($I_d < 1$ μA) at $V_g \approx 0$ V, confirming ambipolar behavior as expected.¹⁴ Next, we measure the transfer characteristics using a gate voltage (V_g) window of -3 to 3 V and applying a drain source of $V_{\text{ds}} = 1$ V (Figure 2h–j for MoS_2 , WS_2 , and WSe_2 , respectively). We also observed gate leakage (I_g) for each device (dashed black line) attributed to the conductivity of the ionic liquid. The low I_g indicates the lack of electrochemical reactions with the electrodes. We calculate μ of the transistors from the equation $\mu = (L_c/W)(1/C_{\text{device}})(g_m/V_{\text{ds}})$, where $g_m = \partial I_d / \partial V_g$ is the transconductance (e.g., measured from the slope of the transfer characteristic from ~ 1 to -1 V_g for n-type MoS_2/WS_2 and ~ 0 to -1 V_g for n-type WSe_2) and C_{device} is the device capacitance estimated as ~ 3.1 $\mu\text{F cm}^{-2}$ from cyclic

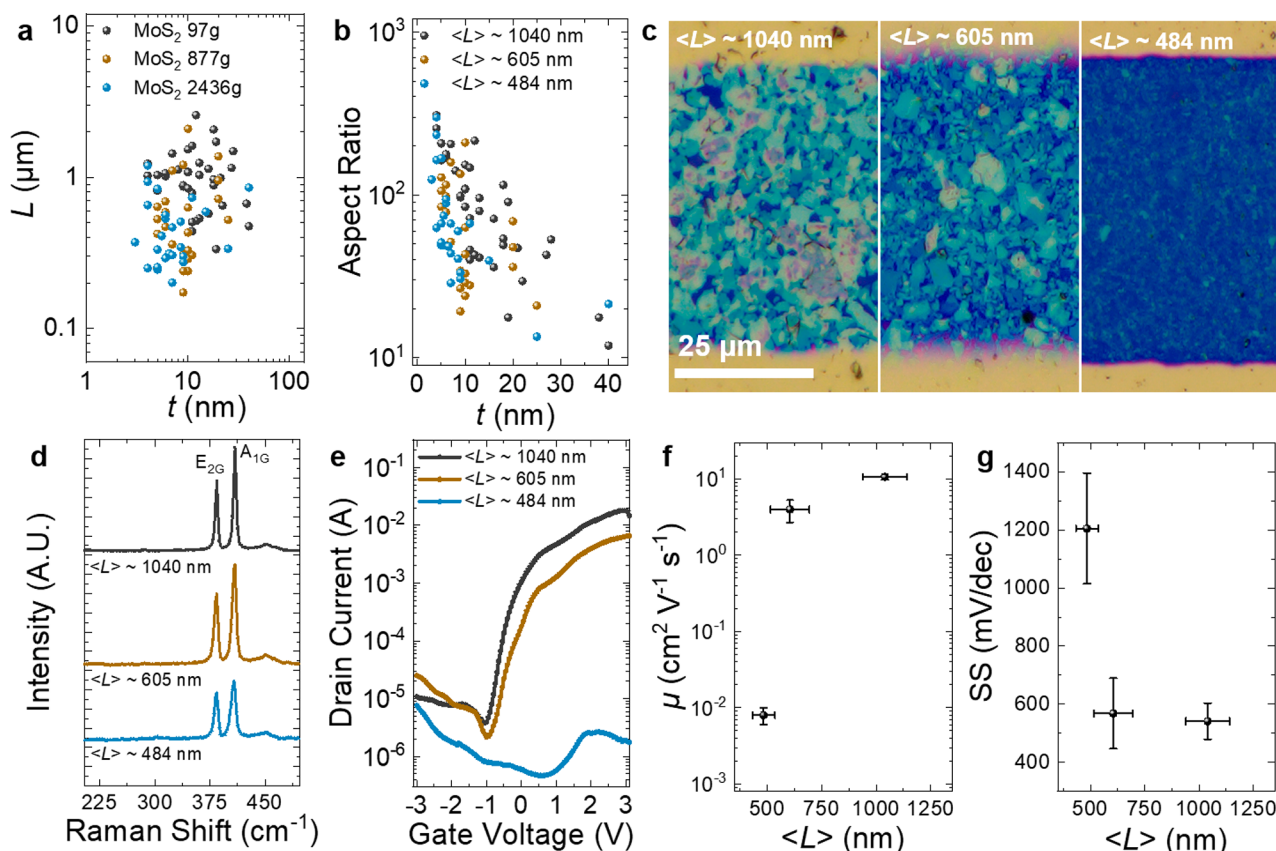


Figure 4. Examination of the effect of $\langle L \rangle$ on MoS₂ transistor performance. (a, b) Atomic force microscopy statistics of the MoS₂ flakes. (c) Optical microscopy of the transistor channels with $\langle L \rangle$ from 484 to 1040 nm. (d) Raman spectroscopy of MoS₂ to determine the defect density in the MoS₂ flakes. (e) Transfer characteristics of the MoS₂ flake networks as a function of $\langle L \rangle$. (f) Average μ and (g) average subthreshold slope of the MoS₂ transistors as a function of $\langle L \rangle$. Error is calculated by the standard deviation of the mean (SDOM) in each case.

voltammetry (see Methods and Supplementary Note 6). The average ambient μ values for MoS₂, WS₂, and WSe₂ are calculated to be $\mu_{\text{MoS}_2} \approx 10.7 \pm 0.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ($N = 9$), $\mu_{\text{WS}_2} \approx 9.1 \pm 2.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ($N = 6$), and $\mu_{\text{WSe}_2} \approx 2.0 \pm 0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ($N = 6$) (Figure 3a), with $I_{\text{on}}/I_{\text{off}} \approx (2.6 \pm 0.4) \times 10^3$, $(3.4 \pm 0.6) \times 10^3$, and $(4.2 \pm 1.8) \times 10^4$ for MoS₂, WS₂, and WSe₂ respectively (Figure 3b). The WSe₂ p-type μ was also notably high at $1.3 \pm 0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The best devices had $\mu_{\text{MoS}_2} \approx 15.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $\mu_{\text{WS}_2} \approx 16.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and $\mu_{\text{WSe}_2} \approx 2.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with $I_{\text{on}}/I_{\text{off}} \approx 1.9 \times 10^3$, 5×10^3 and 5×10^3 for MoS₂, WS₂, and WSe₂ respectively. We find that the electrical properties are consistent within the array and similar to vacuum-based measurements with no significant decrease in performance when measured in ambient air (Supplementary Note 5). The μ value is orders of magnitude greater than those in previous works on ionic gating of TMD networks ($\mu \approx 0.01\text{--}0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)^{10,12–14,21} and either greater than or comparable to those in previous literature ($\mu \approx 0.01\text{--}8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) for solid-state field-effect transistors (FETs).^{3,11,15–18,22,37} We attribute the high μ to both the removal of the residual stabilization agent by centrifugation washing and the use of electrochemical 2D TMDs: their high aspect ratio and LS-induced alignment lead to conformal junctions and thus reduced junction resistance and E_a .⁹ Our devices represent a significant improvement to state-of-the-art solution-processed 2D network literature devices. The transistors are comparable to competing solution-processable

technologies developed over the last few decades, such as organic polymers,^{38–40} semiconducting carbon nanotubes (CNTs),^{41–43} graphene²⁷ and metal oxides,^{44–46} as shown in Figure 3c. A more comprehensive table can be found in Supplementary Note 7. The n-type behavior of MoS₂ and WS₂ could complement the library of high- μ p-type organic polymer materials available for flexible digital electronics, as there is currently a lack of high- μ n-type semiconductors,⁴⁷ essential for CMOS circuits which require both similarly high- μ p-type and n-type transistors.³

Minimising the threshold voltage $\langle V_T \rangle$ is important to reduce the power supply voltage in transistor circuits.³ In Figure 3d our MoS₂ (yellow) and WS₂ (green) transistors have $\langle V_T \rangle = -0.38 \pm 0.05$ and 0.33 ± 0.09 V, respectively, demonstrating minimal variation in $\langle V_T \rangle$ between devices. The n-type $\langle V_T \rangle$ of the WSe₂ devices (orange, n) is 1.63 ± 0.01 V, and the p-type $\langle V_T \rangle$ is -0.80 ± 0.01 V (orange, p), which can likely be attributed to either W or Se vacancies.⁴⁸ In Figure 3e, we calculate the subthreshold slope (SS), defined as the change in gate voltage necessary to change the drain current by one decade. The SS should be minimized to reduce the switching power loss.⁴⁹ We find SS values of 542 ± 62 , 339 ± 64 and 182 ± 36 mV/dec for the MoS₂ (yellow), WS₂ (green), and WSe₂ (orange) transistors, respectively. Since $\text{SS} \propto 1/C_{\text{device}}$,⁵⁰ our SS is expected to be low (<600 mV/dec) since we use a high $C_{\text{device}} \approx 3.1 \text{ } \mu\text{F cm}^{-2}$, attributed to the ionic liquid EMIM TFSI. Assuming the semiconductor capacitance in our transistor channels is similar, and our C_{device} is constant

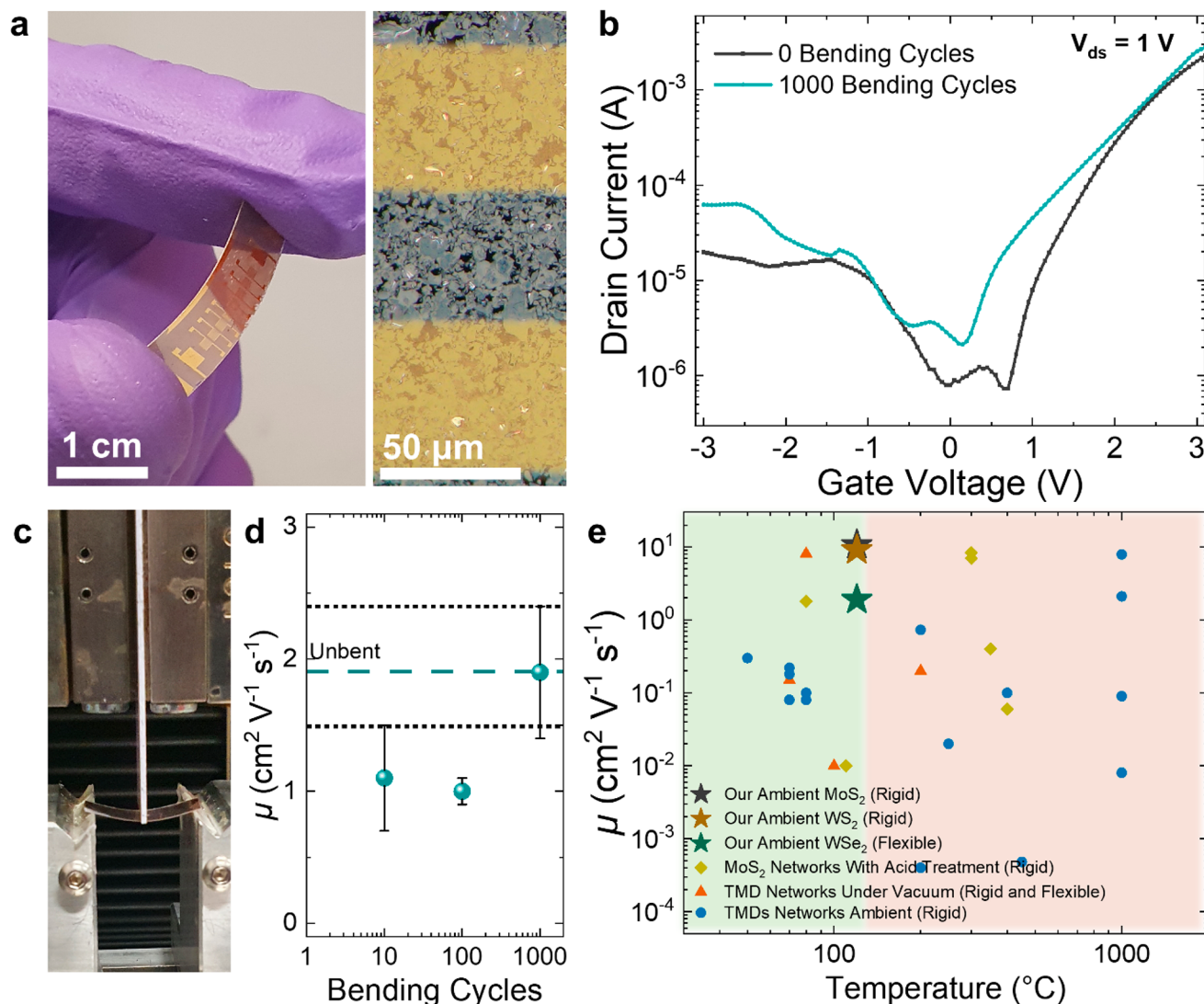


Figure 5. Flexible WSe₂ transistors on PET. (a) Digital image of the WSe₂ transistor array on a PET substrate (left) and optical microscopy image of the WSe₂ channel in bright field (right). (b) Transfer characteristic of the WSe₂ transistors when unbent (0 cycles) and after 1000 bending cycles using $V_{ds} = 1$ V. (c) Digital image of bending apparatus used for strain testing of devices. (d) Transistor μ as a function of the device bending cycles. The unbent device's μ is represented by the horizontal cyan dashed line, and the error is represented by the dashed black line. Error is calculated by SDOM. (e) Our flexible WSe₂ transistor (green star), rigid MoS₂ (black star) and WS₂ (brown star) transistors μ as a function of device processing temperature compared to literature values of other solution-processed TMD network transistors made on rigid or flexible substrates. The green box indicates temperatures compatible with flexible substrates, while the red box indicates temperatures incompatible with most flexible substrates (>120 °C).

between our electrochemical transistors, the increased MoS₂ SS (>200 mV/dec) compared to WS₂ and WSe₂ could potentially be explained by an increased interface trap capacitance. A higher interface trap density in the MoS₂ transistors could be attributed to sulfur vacancies or poor flake-to-flake interfaces in our network.⁵⁰ As a further investigation, we examine the dependence of $\langle L \rangle$ on the transistor μ and SS and find μ is maximized and SS is minimized when $\langle L \rangle > 1$ μm (Supplementary Note 7). Plotting the μ (Figure 3f) and I_{on}/I_{off} values (Figure 3g) as a function of SS, we find that the most optimal devices would be found in each plot's top left-hand corner. In our case, our MoS₂, WS₂, and WSe₂ transistors have some of the lowest SS and highest μ and I_{on}/I_{off} values recorded for TMD networks (Figure 3f,g), even when compared to other ionically gated networks. A comprehensive list can be found in Supplementary Note 7.

Optimization of Flake Lateral Size in Electrochemical Transistors.

As a further investigation, we examine the effect of $\langle L \rangle$ on the transistor performance by making three inks of MoS₂ of different $\langle L \rangle$ by cascade centrifugation at 97g, 877g and 2436g, respectively, followed by centrifugation washing to remove residual polymer (see Methods). In Figure 4a, AFM estimates $\langle L \rangle$ values of 1040 ± 101 , 605 ± 89 , and 484 ± 50 nm and $\langle t \rangle$ values of 14 ± 1 , 10 ± 1 , and 9 ± 2 nm for the 97g, 877g and 2436g MoS₂ inks, respectively. In each ink, the mean AR was above 70 with many flakes have a value >100 (Figure 4b). A single LS process is used to deposit the MoS₂ inks on a Si/SiO₂ substrate, and the previous protocol to pattern the transistors is used (see Methods). We use optical microscopy in the bright field (Figure 4c) to confirm that the TMD flakes cover the channel between the source and drain. The flakes appear to be highly aligned in all cases due to the LS method. As shown in Figure 4d, we use Raman spectroscopy to

investigate the defects in each MoS₂ ink. The Raman spectra look similar, showing the E_{2g} and A_{1g} peaks at 384 and 409 cm⁻¹ as the prominent feature.⁵¹ The intensity ratio of the E_{2g} and longitudinal (LA) mode ($I(\text{LA})/I(\text{E}_{2g})$) can be used to calculate the defect density in MoS₂.⁵¹ The absence of an LA mode peak at ~330 cm⁻¹ is indicative that the MoS₂ is pristine in the basal plane with a defect density of <0.05 nm⁻² for each of the three length-selected samples.⁵¹

In Figure 4e, we characterize the electrochemical MoS₂ transistors using a probe station at atmospheric pressure and in ambient air. The transfer characteristic ($V_{\text{ds}} = 1$ V) shows n-type behavior, which is typical of MoS₂ for the $\langle L \rangle \approx 1040$ nm and $\langle L \rangle \approx 605$ nm flake network consistent with previous reports,^{3,13,52} but ambipolar behavior for the $\langle L \rangle \approx 484$ nm flakes, possibly due to doping from residual polymer, solvent, or oxygen edge functional groups,⁵³ which has been observed previously in MoS₂ flakes.⁵⁴ The ambient μ values for each MoS₂ network (Figure 4f) are calculated to be $\mu_{1040} \approx 10.7 \pm 0.9$ cm² V⁻¹ s⁻¹ ($N = 9$), $\mu_{605} \approx 4.0 \pm 1.3$ cm² V⁻¹ s⁻¹ ($N = 3$) and $\mu_{484} \approx 0.008 \pm 0.002$ cm² V⁻¹ s⁻¹ ($N = 3$) with $I_{\text{on}}/I_{\text{off}} \approx (2.6 \pm 0.4) \times 10^3$, $(3.3 \pm 1.9) \times 10^3$, and 28 ± 12 for MoS₂ flakes of $\langle L \rangle \approx 1040$, 605, and 484 nm, respectively. The increase in μ with $\langle L \rangle$ suggests the networks to be at least partially junction-limited,⁹ implying further mobility increases are possible. In Figure 4g, we find that the SS decreases with increasing $\langle L \rangle$ from SS $\approx 1205 \pm 190$ mV/dec at $\langle L \rangle \approx 484$ nm to SS $\approx 542 \pm 62$ mV/dec at $\langle L \rangle \approx 1040$ nm. This would suggest a reduced trap capacitance at $\langle L \rangle \approx 1040$ nm (since C_{device} is constant and the semiconductor capacitance is negligible),⁵⁰ and therefore, we would expect more conformal junctions are being made when $\langle L \rangle \approx 1040$ nm. Based on these results, a larger $\langle L \rangle$ should be used when making transistors with TMDs to improve the junctions between flakes and maximize μ and $I_{\text{on}}/I_{\text{off}}$.

Flexible WSe₂ Transistor Arrays. To investigate our technology's applicability on a flexible substrate, we undertake a Langmuir–Schaefer deposition of the WSe₂ ink on PET. We chose WSe₂, as it had shown the highest $I_{\text{on}}/I_{\text{off}}$ in the rigid devices. Gold electrodes were evaporated following the protocol established for our previous Si/SiO₂ devices to make the WSe₂ transistor array shown in Figure 5a, left ($L_c = 50$ μm). A bright field optical microscopy image (Figure 5b, right) shows a uniform deposition of flakes between the source and drain electrodes. The devices are electrically characterized using a probe station in ambient air, and we observe the typical ambipolar behavior expected for WSe₂ (Figure 5b, black curve). We estimate electron $\mu \approx 1.9 \pm 0.4$ cm² V⁻¹ s⁻¹ with $I_{\text{on}}/I_{\text{off}} \approx 2.9 \times 10^3 \pm 0.9 \times 10^3$, which is similar to the μ_{WSe_2} value obtained for WSe₂ transistors on Si/SiO₂ ($\mu_{\text{WSe}_2} \approx 2.0 \pm 0.2$ cm² V⁻¹ s⁻¹, $N = 6$) indicating a successful transfer of the device properties to a flexible substrate despite the higher surface roughness of the PET ($S_q \approx 18$ nm) which would typically result in lower μ .²⁷ We then apply a 1% tensile strain to the transistors for 10, 100, and 1000 cycles using the cyclic tensile tester shown in Figure 5c (see Methods) and find that the μ value is maintained ($\mu \approx 1.9 \pm 0.5$ cm² V⁻¹ s⁻¹, $N = 6$) even after 1000 bending cycles (Figure 5b, cyan curve, and Figure 5d), demonstrating the flexibility of the transistors. In Figure 5e, we plot our transistor's first-cycle μ performance (green star) against the scientific literature on solution-processed 2D material networks, which are measured in ambient air (blue circles), measured under vacuum (orange

triangles), and measured after acid treatment (yellow squares). Most processing methods previously used in the literature are not compatible with flexible substrates, as they typically require annealing temperatures >200 °C or acid treatments and therefore use Si/SiO₂ or quartz substrates (Supplementary Note 7). Only one work by Kim et al. demonstrated a high-mobility TMD network (MoS₂) at a low annealing temperature of ~80 °C, achieving $\mu \approx 8.1$ cm² V⁻¹ s⁻¹ and $I_{\text{on}}/I_{\text{off}} \approx 10^2$ (or $\mu \approx 1.8$ cm² V⁻¹ s⁻¹ and $I_{\text{on}}/I_{\text{off}} \approx 10^6$ on acid treatment) but with a high SS ≈ 3000 mV/dec. However, it was not tested on a flexible substrate but was assembled on Si/SiO₂ and was measured under vacuum.¹⁷ To our knowledge, the only two other works that have demonstrated transistors made on PET from a network of WSe₂ flakes achieved $\mu \approx 0.1$ cm² V⁻¹ s⁻¹ and $I_{\text{on}}/I_{\text{off}} \approx 10^2$ – 10^3 and were both measured under vacuum rather than ambient air.^{10,14} Therefore, our WSe₂ transistors represent a 1 order of magnitude improvement in μ on flexible PET substrates while demonstrating that their performance can be maintained even after excessive straining (1000 cycles at 1% strain). We also note that, to our knowledge, our devices are the only example of flexible high-mobility ($\mu > 1$ cm² V⁻¹ s⁻¹) TMD networks without using acid treatments, high-temperature annealing, or measurement under vacuum/encapsulation. It is also likely that our MoS₂ (black star) and WS₂ (brown star) transistors would also work on a flexible substrate, given that WSe₂ was successfully transferred without a decrease in μ and the MoS₂ and WS₂ follow the same manufacturing and deposition protocol.

CONCLUSIONS

We discover that WS₂ and WSe₂ can achieve high- μ transistors with n-type and ambipolar behavior, respectively, to add to the library of high- μ 2D solution-processed materials which will be required in future devices and circuits that need materials with complementary behavior. We successfully utilized Langmuir–Schaefer deposition to minimize ink waste (<20 μL) and improve the network stacking and alignment, enabling ambient air electrochemical transistors with $\mu \approx 2$ – 16 cm² V⁻¹ s⁻¹, $I_{\text{on}}/I_{\text{off}} \approx 10^3$ – 10^4 , $\langle V_T \rangle \approx 0.3$ – 1.6 V, and SS ≈ 182 – 542 mV/dec representing a 1 order of magnitude increase in μ and SS for state-of-the-art electrochemical transistors with 2D WS₂ and WSe₂ flake networks. The performance was comparable to that of solution-processed solid-state 2D network FETs, CNTs, metal oxides, and organic polymers but without high-temperature annealing (>120 °C), acid treatments, and vacuum measurements, improving the commercialization potential of our solution-processed transistors. We also found that the transistor μ is maximized and SS is minimized when $\langle L \rangle > 1$ μm . As a final demonstration, we created flexible WSe₂ transistors on PET that did not degrade in performance for at least 1000 bending cycles at 1% strain, showing a 1 order of magnitude improvement in μ for solution processed 2D flakes on a flexible substrate.

METHODS

Electrochemical Exfoliation of 2D Crystals. An electrochemical cell with two electrodes is used to intercalate WS₂, WSe₂, and MoS₂ (HQ graphene) crystals. A thin piece (0.1 \times 1 \times 1 mm) of a crystal is used as the cathode, while a platinum foil (Alfa Aesar) is used as the anode. Copper crocodile clips are used to hold the electrodes in place. For the electrolyte, tetrapropylammonium (TPA) bromide (Sigma-Aldrich, 5 mg/mL) is added to propylene carbonate (~50 mL). A voltage of 8 V is applied for 30 min between the

electrodes to intercalate the 2D crystal with TPA⁺ cations. The 2D crystal expands in each case to greater than twice its original volume, indicating the successful intercalation of the crystal. After intercalation, the 2D crystal is emersed in IPA overnight to dissolve and remove any residual bromide ions (Br⁻) on the crystal.

Ink Formulation with 2D Crystals. The 2D crystal is then bath-sonicated (Fisherbrand 112xx series) in 1 mg/mL poly(vinylpyrrolidone) (PVP, molecular weight ~40000) in dimethylformamide (DMF) for 5 min followed by centrifugation (Hettich Mikro 220, 1195-A, radius 87 mm) at 500 rpm (24g) for 20 min to remove unexfoliated crystals. The dispersion is size-selected by centrifuging the supernatant (top 90%) at 1000 rpm (97g) for 1 h and collecting the sediment. Unfortunately, attempts to disperse the 2D crystal directly in DMF without PVP were unsuccessful, as the initial centrifugation step (24g) resulted in complete sedimentation of the unexfoliated and exfoliated crystals. Therefore, size selection and removal of bulk unexfoliated crystals would not be possible. To remove the PVP, the 97g sediment was diluted with 2 mL of DMF and centrifuged at 10k rpm (9744g) for 1 h. The process was repeated twice, and the sediment was collected each time. A third washing step was used to remove residual DMF, which involved diluting the sediment in IPA (0.5 mL) and subsequently centrifuging at 10k rpm (9744g) and collecting the sediment. The sediment is redispersed in IPA (~0.5 mL, concentration ~2.5 mg/mL) to make the 97g dispersion used in the study respectively for each 2D crystal. We use IPA, as it is a low-boiling-point solvent (~82.5 °C) that can evaporate quickly after Langmuir–Schaefer deposition. For the ⟨L⟩ study, the supernatant of the 1000 rpm (97g) MoS₂ dispersion is centrifuged at 3000 rpm (877g) and then 5000 rpm (2436g). The sediment of the 877g and 2436g MoS₂ dispersions follows the washing protocol previously described and is then redispersed in IPA to make the 877g MoS₂ ink and 2436g MoS₂ ink, respectively.

Network Formation by Langmuir–Schaefer and Transistor Electrode Fabrication. The Langmuir–Schaefer setup involves a Teflon stand (10 cm long) where a Si/SiO₂ chip (2 × 2 cm) is placed on top (root-mean-square roughness S_q ≈ 0.1 nm, 300 nm oxide thickness). The stand is placed in a beaker (about 100 mL) of deionized water. About 20 mL of distilled hexane is drop-cast onto the surface of the deionized water to create a water/hexane interface, under which the Si/SiO₂ chip is submerged. The MoS₂, WS₂, and WSe₂ inks are drop-cast (~140 μL) onto the surface of the hexane until no gaps in the interface could be seen. The Teflon stand and Si/SiO₂ are then carefully extruded through the 2D crystal layer to coat the surface of the Si/SiO₂ with the TMD network; ~20 μL of material is lost at the edges of the Si/SiO₂. The TMD networks are left in a fume hood to dry in ambient air for ~6 h. Next, we anneal the TMD networks at 120 °C for 1 h on a hot plate in an N₂ glovebox (Jacomex GP campus) to remove residual solvent and improve the adhesion of the 2D flakes to the Si/SiO₂ substrate. The process is repeated to build the second layer of the network. Two depositions are undertaken for the WS₂ and WSe₂ networks, while one deposition is used for MoS₂. Gold electrodes (~100 nm thick) are deposited by evaporation (FC-2000 Temescal Evaporator) through a stainless steel mask (50 μm thick) which is laser cut (Laser Micromachining ltd). The gold defines the channel dimensions of W = 11000 μm and L_c = 50 μm. The Au evaporation also defines our gate electrode, which is placed ~1 mm from the source and drain electrodes and is ~1.5 × 4 mm in size. The WS₂, WSe₂, and MoS₂ devices (each on individual chips) are then annealed on a hot plate at 120 °C for 1 h in an inert N₂ environment (Jacomex GP campus). The same protocol is used for our WSe₂ devices on a flexible substrate, replacing Si/SiO₂ with PET (Novel, Novacentrix).

Transmission Electron Microscopy. TEM is performed using a JEOL 2100 instrument. The TEM grids are prepared by LS deposition of the MoS₂ ink (1 layer, see Langmuir–Schaefer methods for protocol) on lacey-carbon grids followed by room-temperature drying for ~6 h. The TEM imaging is performed at an accelerating voltage of 200 kV using a beam current of 105 μA.

Scanning Electron Microscopy. SEM is performed with a Carl Zeiss Ultra SEM operating at 4 kV with a 30 μm aperture. Images are

acquired using the secondary electron detector, and the samples are not coated prior to imaging. The sample substrate is a 300 nm SiO₂/Si wafer.

FIB-SEM Cross-Section Imaging. FIB-SEM microscopy is carried out using a dual-beam Carl Zeiss Auriga focused ion beam system. Network cross sections are milled using a 30 kV:600 pA beam. All images are captured at a working distance of 5 mm with a 2 kV accelerating voltage and aperture size of 30 μm. The network porosity is measured by segmenting network cross sections into their pore and nanosheet contributions using trainable WEKA segmentation.⁵⁵ The porosity is calculated by dividing the number of pixels classified as “pore” by the numerical sum of the “pore” and “nanosheet” pixels in each cross-section. This technique can identify pores larger than 5 nm × 5 nm in cross-sectional area.

I–V Probe Station Measurements. To control the injection of ions into our semiconducting channel, we use the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM, Sigma-Aldrich). The ionic liquid is first heated under vacuum at 100 °C for 6 h to remove any absorbed water. A drop of EMIM is then pipetted onto the transistors so that the gate, source, and drain electrodes are covered with ionic liquid. The devices are left under vacuum (~1.6 × 10⁻⁴ mbar) in a Janis Probe Station overnight (12 h) to remove residual water further. Before undertaking measurements, the devices are brought back to atmospheric pressure. To undertake electrical characterization, devices are contacted using gold-coated probes connected to a Keithley 2612A dual-channel source measuring unit. A gate voltage window of -3 to 3 V is used for transfer characteristics with a scan rate of 50 mV/s and V_{ds} = 1 V for all devices.

Cyclic Voltammetry. A Gamry Reference 600 Potentiostat is used to undertake cyclic voltammetry measurements. The capacitance was extracted from area enclosed by the CV curves. We estimate the C_{device} value to be ~3.1 μF cm⁻² for our MoS₂ and WS₂ devices and ~4.9 μF cm⁻² for our WSe₂ devices. C_{device} is also estimated as ~1.2 μF cm⁻² for ⟨L⟩ ≈ 484 nm MoS₂ devices (see Supplementary Note 6 for further information).

Optical Microscopy. An optical microscope (Olympus DSX1000 digital microscope) is used to image deposited droplets in bright field mode. The images are acquired at a ×50 magnification. For the device's imaging, a single 70 × 70 μm image is not sufficient to observe the entire device. Therefore, an area of 7 × 7 images is sequentially taken and stitched together with a 10% overlap in live panorama mode.

Atomic Force Microscopy. A Bruker Multimode 8 microscope is used to undertake AFM and analyze the thickness and lateral size of the flakes. The WS₂, MoS₂, and WSe₂ inks are drop-cast onto Si/SiO₂ after dilution in IPA by a factor of 1:100. The samples are then annealed at 120 °C for 15 min to remove residual solvent. The samples are scanned using OLTESPA R3 cantilevers in ScanAsyst mode, and ~35–50 flakes are counted to determine the statistics. The lateral size is calculated as the square root of the flake length times the flake width.

Raman Spectroscopy. Inks of MoS₂, WS₂, and WSe₂ are drop-cast onto an Si/SiO₂ substrate and annealed at 120 °C. The Raman spectra of the drop cast networks are acquired with a Horiba Jobin Yvon Labram HR800 Raman system at 532 nm with a 10× objective and incident power of ~1 mW to minimize possible thermal damage.

Optical Absorption Spectroscopy. The extinction spectra are obtained using a PerkinElmer Lambda 1050 spectrometer at a step of 1 nm with a 10 mm optical length cuvette (quartz cuvette). The absorption spectra are obtained by using an integrating sphere. The slit width is 2 nm.

Transistor Three-Point-Flexural Tests. A zwickiLine (Zwick-Roell) three-point flexure testing system is used to conduct bending testing on the transistors. The strain applied (ϵ) to our transistor can be calculated using the equation $\epsilon = 6dD_f/L_s^2$, where d is the PET thickness (170 nm), L_s is the support span (16 mm), and D_f is the maximum deflection of the center of the beam. In all cases, we apply a strain of 1%. To obtain an average in our mobility estimate we use N

= 6, 7, 6, and 6 transistors for 0, 10, 100, and 1000 bending cycles, respectively.

ASSOCIATED CONTENT

Data Availability Statement

The authors declare that the data supporting the findings of this study are available within the paper and its [Supporting Information](#) files. Data are also available from the corresponding author upon reasonable request.

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsnano.2c11319>.

Aspect ratio comparison between shear mixing and electrochemical inks, UV–vis of the TMD flakes, imaging with SEM, TEM, and AFM of the flake-to-flake junctions in the networks, optical microscopy of the devices, electrical characteristics of the device arrays including examination of device gate leakage and hysteresis, cyclic voltammetry of the networks, and a literature review of TMD transistors with solution-processed networks (PDF)

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Author Contributions

T.C. and J.N.C. conceived and designed the experiments. T.C., did all electrical measurements, Raman spectroscopy, and optical microscopy on the devices. T.C. and O.C. manufactured the inks and undertook AFM. T.C. and K.S. did Langmuir–Schaefer deposition of TMD inks. S.L. and D.O. undertook gold evaporation on devices. S.L. took all UV–vis measurements. E.C., C.G., and A.G.K. did all SEM measurements. C.G. made laser-cut masks and carried out cross-sectional imaging. H.K. did all TEM imaging. J.G. and T.C. undertook strain testing of devices. T.C. undertook CV measurements with assistance from A.G.K., J.M., and J.N.C. The manuscript was written by T.C. in close consultation with other authors and edited by J.N.C.

Notes

The authors declare no competing financial interest.

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