Position Controlled Growth of Single Crystal Cu₃Si Nanostructures

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KEYWORDS

Cu₃Si, surface energy driven growth (SEDG), Eutectic, patterning

ABSTRACT

In this work we demonstrate the position controlled growth of single Cu₃Si nanostructures using a Ge-Cu bilayer film that contains a pattern of defects on a Si substrate with a thin oxide layer. The defects act as nucleation centres for growth whilst the presence of Ge within the bilayer is critical to insure effective surface diffusion rates and to eliminate spurious nucleation and growth. This behaviour presented is consistent with a surface energy driven growth mechanism. The defect mediated reaction between Cu and the underlying Si substrate insures that the grown nanostructures are in perfect registry with the substrate. The possible applications and alternative implementations of this technology are discussed.

INTRODUCTION

The precision placement of nanostructures is potentially important for a wide range of device and sensor technologies. Patterning of high conductivity metals is important for device interconnects applications; particularly the demand for reduced-dimension solder balls patterns in flip-chip technologies. Bottom-up strategies that exploit the transfer of nanoparticles from solution require complementary recognition chemistries patterned on the substrate surface.^{1, 2} This approach frequently leads to multiple particles aggregating on a single patterned site where the mechanical and electrical connectivity between the particle and substrates is typically unsuited for device applications. The alternative top-down strategy involves the use of electron beam lithography and lift-off.³ While this approach is capable of creating well-ordered arrays of nanostructures with good mechanical adhesion and electrical properties, the patterned structures are typically polycrystalline with no preferred orientation with respect to the substrate. Both approaches involve significant processing steps that are not easily integration into device fabrication.⁴

Here, we consider the growth of patterned arrays of Cu_3Si nanostructures. Silicide structures are important electronic materials with established roles as interconnect and contact materials, respectively.⁵⁻⁷ Conversely, the well-established inter diffusion of Si and Cu greatly affects the material properties close to the interface and can potentially affect device performance. Substantial effort has already focused on the precise synthesis and positioning of copper silicide building blocks on substrates.⁸⁻¹¹ We demonstrate here that by simply heating silicon substrates that contain patterned voids in a deposited Ge-Cu bilayer film it is possible to create arrays of Cu_3Si pyramidal nanostructures. This is an example of a surface energy driven growth (SEDG) process in which differences in the surface energies of the components within a bilayer and the growth substrate facilitates low temperature surface diffusion, nucleation and ultimately the production of high-

quality single crystal materials.¹²⁻¹⁵ Growth is followed in real time using SEM and post growth TEM demonstrates that the nanostructures are not only single crystals but are aligned with the Si substrate lattice. Using this approach arrays of Cu₃Si building blocks that range in size from 200 nm to 1 μ m were fabricated with pitches of 500 nm to 8 μ m. Since the SEDG method involves reaction between the bilayer components and/or the substrate, it does not require the addition of gas phase growth precursors. Thus is easily integrated into established microelectronics fabrication processes and applications.

EXPERIMENT

The multilayer samples in this work were fabricated using Si(100) substrates (2 inch diameter, 275 $\pm$ 25 μ m thick, N-type As-doped wafers, purchased from Semiconductor Wafer, Inc.) capped with a 20-30 nm thermal oxide layer. Controlled thicknesses of polycrystalline Cu followed by amorphous Ge films¹⁶ were deposited on the substrate by varying the sputter-deposition time using a magnetron sputter-coater (Cressington 208 HR). Thickness was monitored in real time using a quartz crystal microbalance. Cu (10 nm) and Ge (2 nm) bilayer film were investigated. To facilitate position controlled growth a focused ion beam (FIB)(Zeiss, Auriga) lithography was used to mill an array pattern of holes into the Cu-Ge bilayer. The nominal diameter and depth of the holes are 100 ~ 150 nm respectively, the latter being sufficient to penetrate beneath the Cu-Ge multilayer and to create voids in the oxide layer on top of the Si substrate (see Fig. S1 of SI). Once transferred into an SEM chamber (SEM, Zeiss, Ultra) these samples were heated *in-situ* from room temperature to 650 $^{\circ}$ C using a heating stage (Kammrath and Weiss Jumbo dTron 304) that is water cooled to reduce outgassing. These temperature conditions were chosen because the Cu-Ge eutectic comprised of 36.0 at. % Ge melts at 640 $^{\circ}$ C.¹⁷ A typical temperature ramp rate of 1 $^{\circ}$ C per second was used and the chamber pressure was kept at below 2×10^{-5} Torr in all cases. At the end

of the temperature ramp the sample was maintained at 650 °C and the reaction was directly monitored by SEM until completion. Experiments with different heating ramp rates were also carried out. At the ramping speed of 0.1 to 10 °C per second range, we could not find any difference in the shape and composition of final structure. After the reaction was completed, the products were characterized by high resolution transmission electron microscope (TEM, FEI Titan) and energy dispersive analysis (EDX). Cross section of samples after growth were prepared using Focused Ion Beam (FIB, Zeiss, Auriga) to investigate the crystal structure and to confirm the registry of the nanostructures with the substrate.

RESULTS AND DISCUSSION

Figure. 1 (a) Phase diagram of Cu-Ge binary alloy system.¹⁸ (b) Schematic diagram of a FIB pattern on top of Cu 10 nm and Ge 2 nm multilayer. The holes are milled through the deposited Ge and Cu layers into the Si substrate with a nominal depth of 50 ~ 100 nm.

Previously, we demonstrated that the 2~10 nm Cu film on a Si substrate results in the formation of wedge-shaped nanostructures during annealing at 650 °C.¹² However, when Ge is used as a catalyst layer single crystal Cu₃Si nanowires were grown on the Si substrate by a mechanism that is consistent with SEDG method.¹² The Ge–Cu binary system has a eutectic temperature of 644 °C

(Fig. 1(a)).¹⁸ Upon heating above the eutectic temperature, 650 °C, the Cu-Ge bilayer melts to form a eutectic alloy containing 36.0 atom % Ge. During annealing, the bilayer film becomes unstable and de-wets the underlying SiO₂ substrate. Eutectic droplets begin to form due to the dissolution of Cu and Ge atoms by surface diffusion. Beneath these growing eutectic droplets, the SiO₂ substrate decomposes to form Cu₃Si, driven by the enhanced local concentration of Cu and the tendency of Cu to rapidly diffuse through SiO₂ to form the silicide. In this sense the eutectic ball acts as the catalyst for decomposition of SiO₂ and silicide formation.^{9, 19-22} The etched Si is known to be released into the liquid Cu/Ge eutectic ball and forms Cu₃(Si_{1-x}Ge_x).²³ Due to the larger heat of formation for Cu₃Si compared to that of the Cu₃Ge, Ge is segregated out of the Cu₃(Si_{1-x}Ge_x) and a high purity single crystal of Cu₃Si is formed in the eutectic ball.²³ A Cu₃Si nanowire grows from this seed as the annealing process continues, and its size is limited by diffusion and the finite supply of Cu from the original bilayer film. The quality of single crystal Cu₃Si nano wire was proven by SEM, TEM and EDX measurement.¹²

Here in this paper we address the question of how one can control the position and the size of the nanostructures over large areas so that the nanocrystals produced can be grown directly onto the device without the complication of any kind of transfer process. In developing a strategy to create arrays of Cu₃Si nanostructures there are three important observations. First, the extensive literature that exists on Cu₃Si growth points to the critical role of substrate defects. Li et al. demonstrates that Cu₃Si growth following Cu deposition on SiO₂/Si substrate is initially due to voids at the SiO₂/Si interface produced by a slow thermal decomposition reaction: $\text{Si} + \text{SiO}_2 \rightarrow \text{SiO}$. These voids facilitate the direction reaction between Cu and Si to form Cu₃Si nanostructures.⁹ This void reaction mechanism was further emphasized by Wen et al.²⁴ using artificially created voids less than 100 nm in size by He-implantation in silicon. In that study, a copper nitrate solution

was used to decorate all the open-volume defects in the single crystal resulting in local Cu_3Si precipitation. Second, we noted in our earlier work that the thermal instability of any bilayer film is greatest at defect sites in the film or at the edges of the substrate.¹³ The SiO_2 passivation layer has much lower surface energy than the components of the bilayer and critical fluctuations at these defect sites initiate dewetting and drive bilayer instabilities that promote diffusion and reaction. Finally, the presence of Ge in the bilayer has been shown to be effective at enhancing diffusion rates on a substrate and to facilitate transport in diffusion limited reactions. In this work we combined all three effects by exploiting the use of focused ion beam (FIB) milling to create a pattern of artificial voids within the Cu-Ge bilayer and the underlying SiO_2/Si interface which upon annealing result in the formation of an array of aligned Cu_3Si nanostructures (Fig. 1(b)).

Figure 2. Time/temperature evolution series of SEM images showing growth of Cu_3Si nanostructure. (a) An array of four FIB milled holes in the Ge/Cu/ SiO_2 /Si substrate 25 second after starting annealing. (b) With annealing white dots of Cu-silicied begin to form. (c) Precipitation of Cu in the milled holes. (d) and (e) Cu precipitate in the milled holes increases in size. (f)-(i) Rectangular features are formed and increases in size. The time after annealing and the temperature are written in each figure. The scale bar is 1 μm . (j) Cu_3Si structures grown from a FIB patterned array revealing individual nanostructures grow only in FIB milled dots.

Exploiting our capability to perform real time observation of Cu_3Si growth, we can directly observe that the growth of the Cu_3Si nanostructure as described in Fig. 2. Figure 2(a) shows an SEM image of the original pattern of voids on the Cu-Ge bilayer. The Ge and Cu layers are 2 nm

and 10 nm thick, respectively, while the voids have diameters of 120 nm and are 50~100 nm deep (see Fig. S1 of SI). Note the void depth is sufficient to penetrate beyond the bilayer film and into the SiO₂/Si interface beneath. We begin by optimising the growth condition to directly observe Cu₃Si formation in real time SEM during in-situ annealing. We found an optimized annealing speed of 1 °C per sec enables us to ramp the temperature slowly to the desired level (650 °C) and then to follow the nanostructure growth with minimal thermal drift in the SEM image. When the temperature reached 182 °C, the surface is comprised of small droplet-shaped islands, with average dimensions of ~ 50 nm. At this stage the positions of the droplets are randomly distributed and looks similar to that previously report.^{24, 25} This random distribution of droplets can be clearly seen in Fig 2(b). Increasing the temperature to 325 °C, the number density of these small islands is reduced and instead much larger nanostructures (later shown to be Cu₃Si) begin to form at the locations of the FIB voids as seen in Fig.2(c). At higher temperatures of 513 °C, the nanostructures become bigger and appear as square-shaped crystallites (Fig. 2(d) - (f)). The initial temperature of crystalizing is lower than the original bulk eutectic temperature since the latter is known to decrease markedly with decreasing the particle size.²⁶⁻²⁹ We note that the orientation of these square crystallites is the same across the substrate, indicating an epitaxial relationship with the underlying single crystal Si substrate. Since the final nanostructures are larger than the patterned voids the growth of Cu₃Si likely generates new defects at the SiO₂/Si interface consistent with the extra volume expansion associated with the formation of Cu₃Si.³⁰ This is consistent with the known ability of Cu₃Si to catalyze the further decomposition of surrounding SiO₂ leading to void formation and continued Cu₃Si growth.^{2, 15}

Figure 3. (a) Cross-section TEM images of Cu_3Si nanostructures which is rooted in Si substrate. (b) HRTEM images of the nanostructure. Inset FFT pattern of the same area, viewed along the $[0001]\eta''$. (c) The enlarged TEM image of blue square box of (a) to show the interface.

HRTEM analysis of the Cu_3Si nano structure reveals a single crystal as shown in Figure 3(a). After the Cu_3Si crystal was grown from the patterned hole, a cross section of nano structure was prepared using FIB. As shown in Figure 3(a), the root of Cu_3Si crystal is embedded in the Si crystal and covered by Pt that was used as a protection layer. We note the appearance of parallel Moiré fringes (indicated by red circle) due to the presence of long-period antiphase domains (LPAPD), which have been reported previously for epitaxial Cu_3Si thin films grown on silicon.² The LPAPD pattern

is continuous along the entire nanostructures indicating that the nanostructure is a single crystal. The root of the crystal is comprised of a V-shaped groove with a sharp border consistent with a highly anisotropic reaction. The angle between border of the groove shows (111) direction at an angle of 54.7° from the (100) surface. Because Si (111) planes have the highest surface atomic density of all silicon planes, the reaction takes place along Si<111> directions kinetically. The growth along Si<111> likely occurs via the diffusion of Cu atoms from the surface at high temperatures. This reaction with the Si substrate is self-limiting due to the limited local availability of materials (Cu, Si). However, the lateral growth of these nanostructures, which is evident from Fig 2, reflects the availability of SiO₂ surrounding the initial patterned growth locations and the ability of Cu₃Si to catalyze the formation of void defects that facilitate the direct reaction of Cu atoms with the silicon substrate.^{2, 15}

The HRTEM image of the grown nanostructure in Figure 3(b) shows a single crystal Cu₃Si [0001] η'' pattern with a 0.35 nm d spacing, which is in good agreement with previously reported measurements.²⁴ Based on the HRTEM (Figure 3(b)) and EDX data (see Fig. S2(d) of SI), the structural composition of this nanostructure is unambiguously identified as Cu₃Si. Figure 3(c) shows the enlarged TEM image of the blue squared area of Fig. 3(a) at the interface between the nanostructure and the Si-SiO₂ interface. The average thickness of oxide layer on top of Si surface is 20 ~ 30 nm. After nanostructure growth, the oxide layer next to the nanostructure becomes thinner the bubble-like structures inside the nanostructure were observed (see Fig. S2(a) of SI). These bubble-like structures have an amorphous structure (see red arrows in Fig. S2(c) of SI), with a silicon and oxygen composition and are consistent with structures previously reported.¹² It is already established that the Cu₃Si precipitates at the oxide/silicon interface and catalyzes the reaction between silicon and SiO₂.⁹ This is believed to involve the rupture of Si-Si bonds in silicon

and Si-O bonds in SiO₂ via catalytic action of Cu₃Si,⁹ which leads to the formation and desorption of SiO and consistent with the presence of bubble-like void at the interface.

Figure 4. SEM images after annealing FIB patterned samples with (a), (c) Cu 10 nm / Ge 10 nm multilayers and (b),(d) Cu 10 nm single layer. Hole depth is around 50 nm with dot separation of 1 μ m for (a) & (b) and 0.5 μ m separation for (c) & (d). The sample which grown from Cu-Ge bilayer film shows pyramidal nanostructures and imaged as 30°-tilted view to give better understanding whereas the random shaped structure of (b) and (d) grown from the Cu single layer has no height so that they presented as plan view.

To illustrate the critical role of Ge in the Cu₃Si nanostructure growth process we compared the behaviour of the Cu-Ge (10 nm / 10 nm) bilayer film (Fig. 4(a) and (c)) to that of a 10 nm Cu single layer film (Fig. 4(b) and (d)) following an anneal to 650 °C. As shown in Figure 4, well-oriented nanostructures were only grown on the Cu-Ge bilayer sample. Regular shaped features are observed at fixed separations corresponding to the original void pattern. Occasionally we observe a pointed nanowire-like growth on top of these pyramidal nanostructures. However, the

fraction of the nanostructure containing nanowires is less than 0.1%, which is significantly less than was observed following a non-patterned bilayer growth study.¹² This is likely a result of the FIB milled holes acting as a rapid sink for Cu atoms via direct reaction with the Si substrate and thus reducing the supply available for wire growth. Under these conditions nanostructure growth with pitches that range from 500 nm, 1 μm , 5 μm and 8 μm were successfully grown (see Fig. S3 of SI). The diffusion length of Cu atoms facilitated by the presence of Ge is sufficient to deplete the entire bilayer leading to a tight distribution of nanostructure sizes.

In contrast, when a FIB patterned single layer Cu film with 0.5 μm separation is annealed (Fig.4 (b)), the majority of the material becomes precipitated around the patterned voids without any regular shaped nanostructure or nanowire growth. When the separation between the patterned voids is increased to 1 μm (Fig. 4(d)), some of material becomes aggregate around the void and increases the size of the voids, however most of the material has dewet the surface without any registry. Figure 4 conclusively shows that SEDG method using the Cu-Ge bilayer is necessary to facilitate controlled nanostructure growth at the pre-determined locations.

CONCLUSION

In summary, we have shown that an artificial pattern of voids created by FIB facilitates the growth of an array of single crystal Cu_3Si nanostructure. While the mechanism relies on the formation of voids that promote the silicide formation reaction the presence of Ge in the bilayer is essential to facilitate surface diffusion and the elimination of spurious nanostructure growth. Whilst the approach reported here involves the use of FIB it is likely that an imprint lithography approach would also be effective in generating patterns of defects which would in turn greatly facilitate its implementation in electronic device applications.

ASSOCIATED CONTENT

Supporting Information. Cross sectional SEM image of FIB milled hole, Cross sectional TEM image and EDX data of Cu₃Si nanostructure and SEM images of patterned Cu₃Si nano structures with various pitches This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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The position controlled growth of single Cu_3Si nanostructures using a Ge-Cu bilayer film that contains a pattern of defects on a Si substrate with a thin oxide layer was presented.

Supporting information

Position Controlled Growth of Single Crystal Cu₃Si Nanostructures

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Figure S1. Cross sectional SEM image of FIB milled hole: The diameter and depth of the hole are 120 nm and 50 nm. The depth is sufficient enough to penetrate the Cu-Ge multilayer and to create voids in the oxide layer on top of the Si substrate.

Figure S2. Cross sectional TEM image of Cu₃Si nanostructure. (a) The bubble-like structures inside the nanostructure are marked with red arrows. (b) The thickness of the oxide layer is marked with red line. The oxide layers next to the nanostructure become thinner than the original oxide layer. (c) Bubble-like amorphous O-containing region near the silicide/Si interface. (d) The EDX analysis of the nanostructure within the better than 1 at.% detection sensitivity of EDX. The wire is comprised 25 % of Si and 75 % of Cu, which is Cu₃Si phase according to the Cu-Si binary phase diagram. A trace amount of Ge and O was detected on the surface area.

Figure S3. SEM images of patterned Cu_3Si nano structures with various pitches of (a) 500 nm (b) 1 μm (c) 5 μm and (d) 8 μm .

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