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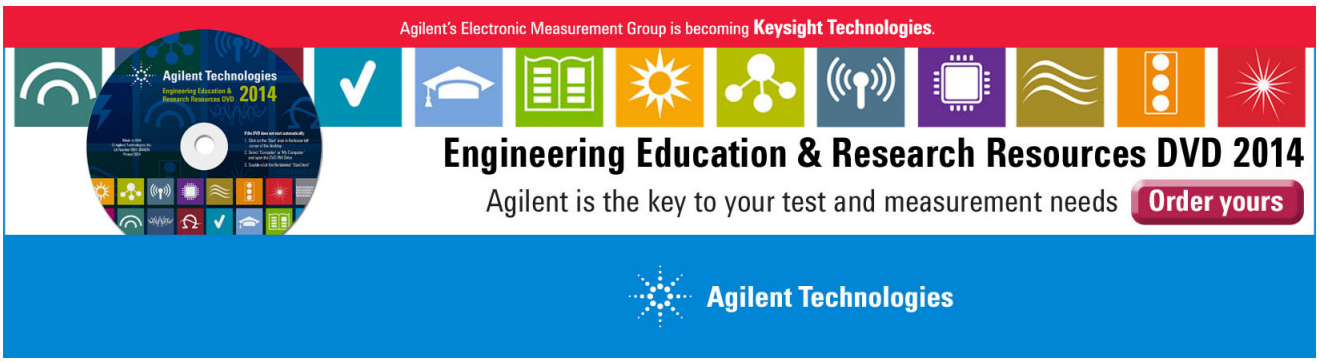

Single-crystal silicon/silicon dioxide multilayer heterostructures based on nanomembrane transfer

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A method to fabricate single-crystal Si/SiO_2 multilayer heterostructures is presented. Heterostructures are fabricated by repeated transfer of single crystal silicon nanomembranes alternating with deposition of spin-on-glass. Nanomembrane transfer produces multilayers with low surface roughness and smooth interfaces. To demonstrate interface quality, the specular reflectivities of one-, two-, and three-membrane heterostructures are measured. Comparison of the measured reflectivity with theoretical calculations shows good agreement. Nanomembrane stacking allows for the preprocessing of individual membranes with a high thermal budget before the low thermal budget assembly of the stack, suggesting a new avenue for the three dimensional integration of integrated circuits. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2734367]

Si/SiO_2 heterostructures offer the prospect of large band offsets from layer to layer, and thus are of great interest for many potential applications. These range from electronic devices such as double- and triple-barrier resonant tunneling diodes,[1] to light emitting materials such as superlattices,[2] to photonics.[3] In general, Si/SiO_2 heterostructures are an enabling step towards three-dimensional integration of electronic and photonic systems. Polycrystalline-Si/amorphous-SiO_2 heterostructures can be fabricated using growth techniques by alternating deposition of Si and SiO_2. However, the presence of grain boundaries in the polycrystalline film is detrimental to many applications. Further, growth of polycrystalline Si on amorphous materials leads to roughening that increases as the number of layers in the structure increases. Thus, methods to create crystalline-Si/amorphous-insulator structures are desirable.

Silicon on insulator (SOI) is a cornerstone of modern micro- and nanoelectronics because it combines a thin single-crystal Si layer on top of SiO_2.[4] Its advantages include the excellent electronic properties provided by single-crystal Si and the effective isolation from the substrate provided by the oxide insulating layer. Recent advances in SOI substrates include ultrathin SOI, offering a solution to the problem of the short-channel effect, and strained SOI (sSOI), which enables tuning of both the electronic band structure and carrier mobility.[5,6] The ability to stack SOI layers or even sSOI layers vertically may lead to higher device densities and potentially to three-dimensional (3D) process integration for optics, mechanics (e.g., in microelectromechanical systems), and electronics.

The Smart Cut™ (Ref. 7) and silicon implanted oxide processes are the most common ways to produce single-layer SOI wafers. The extension of single-layer Smart Cut™ to multiple layers has been reported by Maleville *et al.*[8] to create multilayer heterostructures of single-crystal Si on top of amorphous SiO_2. The required multiple H implantations and successive high temperature annealing steps necessary to restore the crystal structure place strong limits on the degree of integration that is possible.

The concepts of epitaxial lift-off[9] or nanomembrane transfer[10,11] offer a simpler approach to the fabrication of single-crystal Si and amorphous-SiO_2 multilayer heterostructures, one with potential advantages. The flexibility offered by nanoscale thin crystalline membranes enables robust bonding at low temperatures. Membranes with finished devices can be transferred and stacked without high temperature treatment and thus little degradation occurs during stacking. Low temperature processing is also important for applications such as flexible electronics, in which host substrates are not able to sustain annealing at high temperatures.[12] Further, bonding to curved substrates is possible, something that is practically impossible for thick wafer bonding. The freedom to vary the membrane size also leads to the possibility of laterally localized heterostructures. Such local reconfiguration of substrates is already used in the fabrication of commercial field-effect transistors with local strain for improved mobility. The process described here enables such reconfiguration in the vertical direction as well. Importantly, low surface roughness is achieved for each added Si layer, in contrast to the dramatic increase in surface roughness that occurs when polycrystalline/amorphous-material heterostructures are fabricated by growth techniques.

The nanomembranes we use here are formed from SOI.[13] Although single-layer SOI is a convenient starting point for membrane transfer, there are other options. Songmuang *et al.*[14] have demonstrated the possibility to prepare by growth substrates with single-crystal Si on a sacrificial layer such as Ge. Recent work[15,16] has shown that a series of etching steps can generate large quantities of Si nanoribbons from bulk Si, offering a low-cost method to obtain crystalline-Si membranes. In this work we pattern into SOI an array of square holes, for rapid underetching and release, using photolithography followed by SF_6 reactive ion etching. Following patterning, the membranes are released by immersing the SOI chip in a solution of 10% HF. After the underlying oxide is removed, agitation of the solution causes the membrane to rise to the surface, at which point it can be transferred to de-ionized water for rinsing and removed by lifting it out of the water with the desired final substrate. After the water evaporates, the membrane adheres to the sub-

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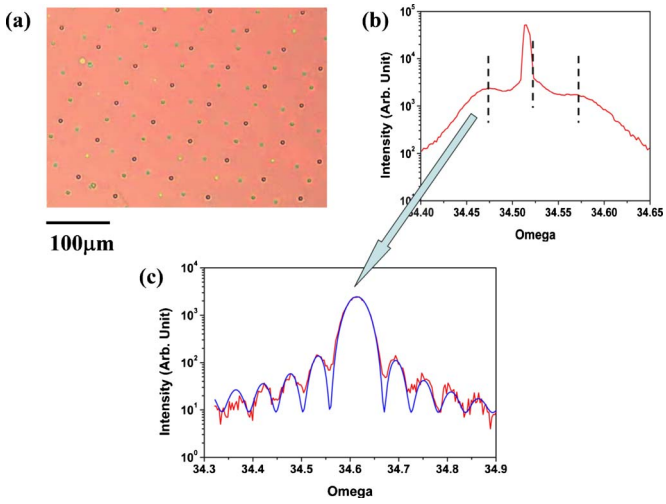

FIG. 1. (Color online) (a) Optical image of three stacked membranes with a SOG layer in between each membrane. Visible are the three sets of holes with slightly different orientations and offset from each other. (b) and (c) show x-ray diffraction data for the same sample. (b) ω scan showing three broad membrane peaks as well as the sharp substrate peak. (c) $\omega/2\omega$ scan corresponding to the left peak in (b). The blue line is a simulation using a best fit silicon layer thickness of 96 nm. Similar $\omega/2\omega$ scans can be obtained for the other two-membrane peaks.

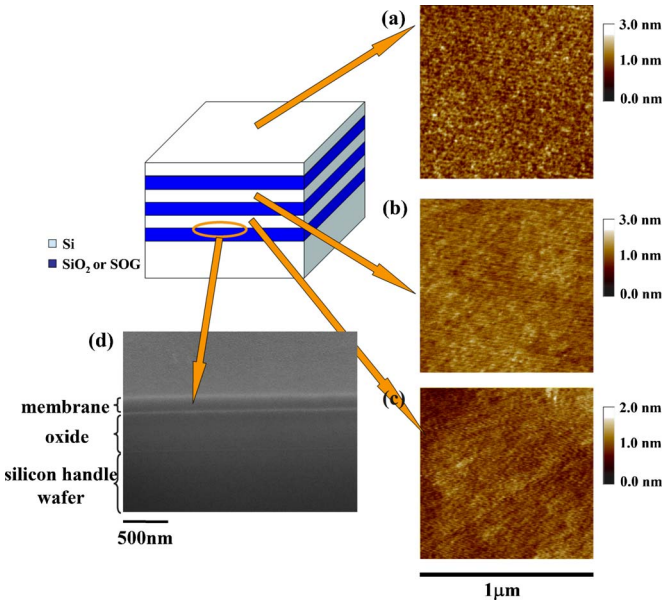

FIG. 2. (Color online) [(a)–(c)] AFM images of the top Si layer from three different samples with different numbers of layers. Sample (a) has three Si layers (with intervening SOG) and its rms surface roughness is 0.25 nm; sample (b) has two layers, and its rms roughness is 0.15 nm; sample (c) is a single transferred membrane on SOG, and it has 0.17 nm rms roughness. (d) Tilted SEM image of a membrane cross section. FIB was used to cut the cross section.

strate. Annealing at 500 °C enhances the bonding of the membrane to the substrate, enabling subsequent wet-processing steps.

We use spin on glass (SOG) to form a dielectric between the single-crystal Si membranes. Upon annealing at 900 °C, SOG forms silicates with a refractive index $n=1.46$, comparable to silicon dioxide, and thus suitable for optical devices. For electronic applications, use of thermal oxidation would provide superior properties. By repeated membrane transfer and deposition of SOG, this stacking technique results in single-crystal semiconductor/amorphous-insulator heterostructures [Fig. 1(a)]. Additional fabrication details can be found in Ref. 17.

For many applications, both surface and interface roughness will affect device performance. For optical applications, increased roughness will decrease the reflectivity and increase scattering. To examine the surface and the membrane-substrate interface we use atomic force microscopy (AFM) and focused ion beam (FIB) plus scanning electron microscopy (SEM). The surface morphologies of the top Si layers from three different samples with different numbers of Si layers are shown in Fig. 2. The surface roughness remains small for all Si layers, in the range from 0.15 to 0.25 nm, comparable to that of prime SOI wafers. Variation in rms values are not correlated with the increasing numbers of layers, i.e., no overall increase in surface roughness with increasing numbers of Si layers is observed.

The fact that upper layers can be as smooth or smoother than lower layers emphasizes that membrane transfer can in fact act as a smoothing process, exactly opposite to the case of growth. Further, it is important to note that the surface of the substrate to which the membrane is transferred is usually rougher than the membrane itself. We find that the rms roughness of the SOG surface exceeds 1 nm. Thus, while the flexibility of the membranes enables them to "drape" over micron size particles, the stiffness of a 100 nm thick membrane acts to reduce short-range roughness. The decrease in roughness due to stiffness may indicate the presence of nanovoids at the underlying Si and SiO_2 interface. Even though such voids must be very small, they may affect the ultimate bonding strength and are a possible trade-off to the smoothing effects of membranes. Nonetheless, a major advantage of the approach of stacking Si membranes is to maintain low surface roughness as additional Si layers are added. In contrast, growth techniques increase roughness with more overlayers.[3] Figure 2(d) shows the interface between a silicon membrane and the underlying oxide along a FIB cross section.

Figure 1(b) shows the rocking curve x-ray diffraction data for a three-layer single-crystal Si/SiO_2 multilayer heterostructure fabricated by nanomembrane transfer. The three broad peaks correspond to the three Si layers, while the sharp peak overlapping the middle broad peak is the substrate peak. From these x-ray data it is clear that the misalignment in ω of different layers from stacking is similar to the value for commercial SOI, of order 0.1°. Aligning to one of the three peaks corresponding to a membrane layer and performing a $\omega/2\omega$ scan produces a central peak with clear, symmetric fringes. The intensity oscillations on either side of the center peak are further evidence that both the surface and the interface with the substrate are sharp and flat. Such measurements provide a method to extract the thickness of each layer, 96 nm for the layer in question.

Photonic applications of Si/SiO_2 heterostructures are motivated by the high index contrast between the silicon index of refraction ($n=3.5$) and that of its thermal oxide ($n=1.45$). One example is Si-based dielectric mirrors, offering high reflectivity and a broad bandwidth with omnidirectional properties. As a quality test of the fabrication method reported here, we measured the reflectivity of heterostructures fabricated by membrane transfer using Fourier transform infrared (FTIR) reflectometry. We took data on samples consisting of a Si substrate and one, two, and three Si membranes, with intervening SOG layers. We used a gold film as

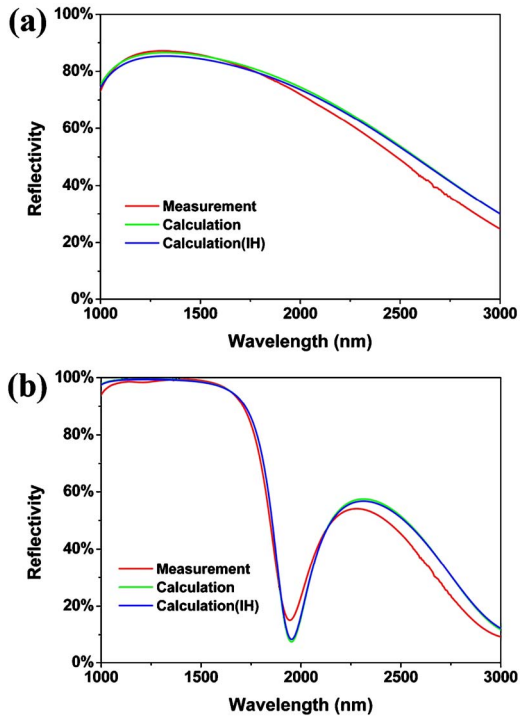

FIG. 3. (Color online) Specular reflectivity of Bragg reflectors for *s*-polarized radiation and an incident angle of 35° from the normal. The detailed layer thicknesses are as follows: (a) 104 nm Si/225 nm SOG/Si substrate, (b) 108 nm Si/167 nm SOG/108 nm Si/166 nm SOG/108 nm Si/180 nm SOG/Si substrate. Calculations are performed using a matrix formulation. The green curves ignore the presence of holes in the membranes. The blue curves include the effect of holes. The holes decrease the reflectivity by ~2% for a single membrane. This effect decreases for heterostructures with more than one membrane and is less than 0.1% for three membranes.

a reference, as it is highly reflective (above 98%) for the telecommunication wavelength range (1–2 μm) reported here. The reflectivity of the gold film is calculated using the n and k data listed in Ref. 18.

Figure 3 shows experimental and calculated reflectivities for specular reflection of *s*-polarized infrared radiation with an incidence angle of 35° from the surface normal. For a single transferred membrane (Si/SOG/Si substrate), the reflectivity is a slowly varying function of wavelength, peaking at 86% [Fig. 3(a)]. As expected, when additional periods of the heterostructure are added, the reflectivity increases, reaching a peak of more than 99% for three membranes [Fig. 3(b)]. The addition of membranes causes the reflectivity as a function of wavelength to take on the classic plateau-shape characteristic of Bragg reflectors. Simulations of the reflectivity (the matrix formulation[19]) match the experimental data, indicating that the optical properties of the Si/SOG heterostructure match the expectations based on bulk indices of refraction.

Holes are intentionally introduced into the membranes to decrease the time required for complete release of large membranes, but in principle they can be avoided using a back side etch. In practice, we have released membranes as large as 400 μm on a side without holes and without a back side etch. Perhaps surprisingly, for applications such as Bragg reflectors that make use of the entire membrane, the presence of small holes has a negligible effect. In total, the holes in one single-membrane account for approximately 2% of the total area. Simulations show that, as expected, the reflectivity is reduced by ~2% for the single-membrane sample. However, the effect decreases with the increasing numbers of membrane layers and is only 0.1% for three membranes. This reduction is due to the low likelihood of holes aligning between layers. Light incident on any given hole, e.g., in the top layer, is reflected by the combined effect of the remaining layers, when multiple membranes are present.

In summary, using a membrane transfer technique, we have fabricated single-crystal-Si/amorphous-SiO_2 multilayer heterostructures with smooth surfaces and no increase in rms roughness with repeated transfer and stacking. The approach relies on bonding, but it is a very different type of bonding than wafer bonding of thick substrates. It is observed in our experiments that pillars about tens microns wide and hundreds of nanometers tall made on a supporting substrate lead to voids about two times wider than the perturbation when a nanomembrane is transferred, whereas they can create centimeter size voids in wafer bonding.[20] Further, it is a common modern microelectronics approach to engineer local regions on substrates, e.g., with strain for high-speed transistors. Membrane transfer offers the prospect of local, high-quality heterostructures integrated with regions of very different materials, including different strains, different numbers of layers, and even different crystalline orientations or compositions.

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